SY21275

High-Performance Boost Regulator for UHD TV Display

General Description

The SY21275 high-efficiency, current-mode-control boost regulator operates over a wide input voltage range of 8.6V to 15.9V and integrates a low-$R_{DS(ON)}$ N-channel MOSFET. It employs a fixed 500kHz switching frequency that provides high efficiency and fast transient response, and features an externally programmable soft-start time to minimize the inrush current at start-up.

The SY21275 is highly integrated, so only the input and output capacitors, inductor, soft-start capacitor, and resistor-divider need to be selected for the targeted application specifications.

SY21275 is available in a compact DFN3×3-10 package.

Features

- Wide 8.6V–15.9V Input Voltage Range
- Low $R_{DS(ON)}$ for N-channel MOSFET: 75mΩ (typical)
- 95% Typical Efficiency
- Feedback Reference Voltage: 1.25V ±1.5%
- 500kHz Fixed Switching Frequency
- Pulse Skipping Mode at Light Load
- Adjustable Soft-Start Limits Inrush Current
- EN ON/OFF Control
- Overvoltage Protection
- Cycle-by-Cycle Current-Limiting Protection
- Input UVLO
- Thermal Shutdown with Automatic Recovery
- Compact DFN3×3-10 Package

Applications

- TFT LCD Panels AVDD

Typical Application

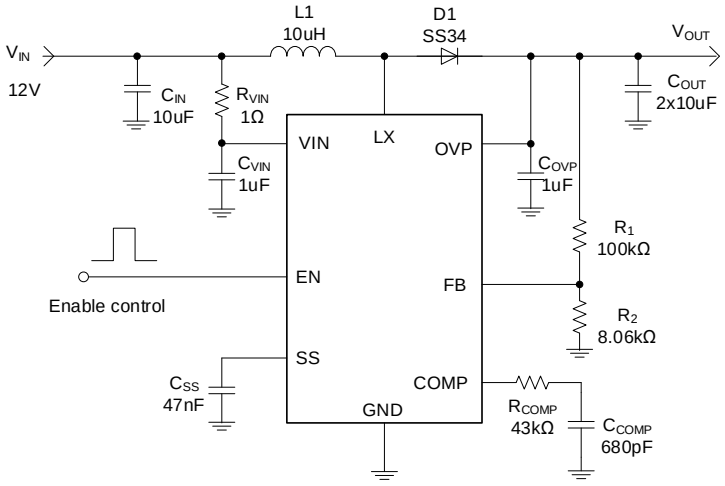


Figure 1. Schematic Diagram

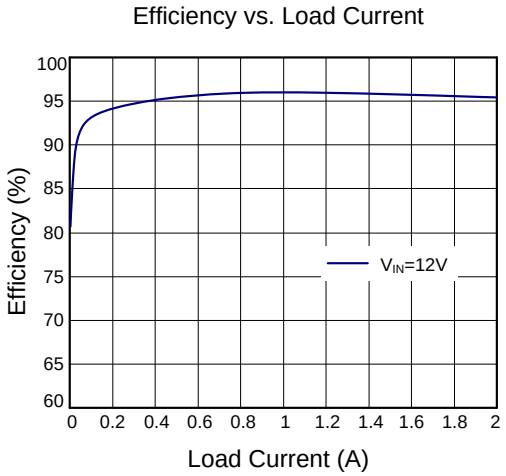


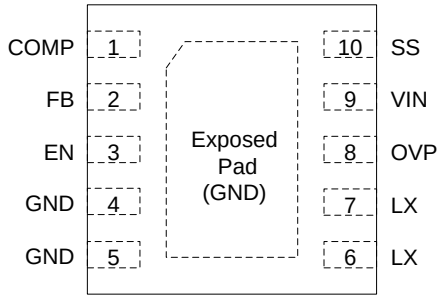
Figure2. Efficiency vs. Load Current

Ordering Information

Ordering Part Number	Package Type	Top Mark
SY21275DBC	DFN3×3-10 RoHS Compliant and Halogen Free	**BAM*xyz***

x = year code, y = week code, z = lot number code

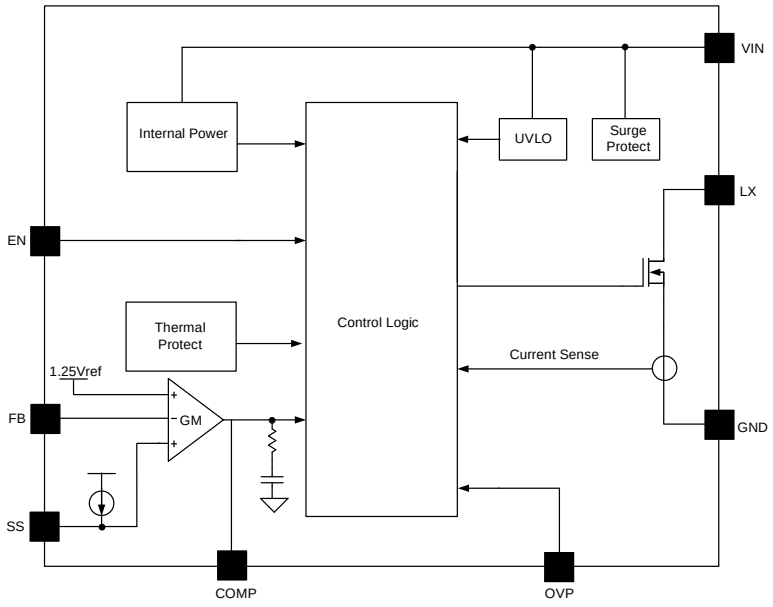
Pinout (top view)



Pin Description

Pin Name	Pin Number	Pin Description
COMP	1	Loop compensation pin. Connect a RC network between this pin and ground to stabilize the control loop.
FB	2	Output voltage feedback. Connect to the center of a resistive voltage divider between the main output and the ground.
EN	3	Enable control pin. Pull high to enable the regulator; pull low to disable the regulator. Do not leave floating.
GND	4,5	Ground pin.
LX	6,7	Inductor pin. Connect this pin to the switching node of the inductor.
OVP	8	Boost-regulator overvoltage-protection input pin. Decouple this pin from the GND pin with a minimum 10µF ceramic capacitor.
VIN	9	Supply input pin. Decouple this pin from the GND pin with a minimum 10µF ceramic capacitor.
SS	10	Soft-start control pin. Connect a capacitor between this pin and GND to program the soft-start time. A 5µA pullup current source is connected to this pin.
EP	–	Exposed pad. Connect to ground plane for better thermal performance.

Block Diagram



Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
V_{IN}	-0.3	22	V
EN, LX, OVP, COMP, SS	-0.3	28	
FB	-0.3	4	
Lead Temperature (Soldering, 10s)		260	°C
Junction Temperature, Operating	-40	150	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	38	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	8	
P_D Power Dissipation T_A = 25°C	2.6	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
VIN, EN	8.6	15.9	V
Junction Temperature, Operating	-40	125	°C
Ambient Temperature	-40	85	

Electrical Characteristics

(V_{IN} = 12V, TA = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		8.6		15.9	V
Input UVLO Threshold	$V_{UVLO,RISING}$	V_{IN} rising threshold voltage, V_{FB} > 300mV, V_{OVP} > 6V	8.0	8.3	8.6	V
Input UVLO Hysteresis	$V_{UVLO,HYS}$		0.6	0.8	1.0	V
Shutdown Current	I_{SHUT}	EN = 0	5		15	μA
Quiescent Current	I_Q	EN = high, V_{FB} = 1.3V	90	120	150	μA
Enable Logic High Threshold	V_{EN_HIGH}	Rising	1.5			V
Enable Logic Low Threshold	V_{EN_LOW}	Falling			0.4	V
Switching Frequency Program Range	F_{OSC}		450	500	550	kHz
Feedback Reference Voltage	V_{REF}		1.2312	1.25	1.2688	V
Peak Current Limit	$I_{LIM, PEAK}$	Duty = 15%	4.5		6.5	A
N-FET R_{ON}	$R_{DS(ON)}$		50	75	100	mΩ
Soft-Start Delay Time	t_{DLY}		1.5	2.5	3.5	ms
Minimum On Time	$t_{ON,MIN}$	Note 5	20		80	ns
Soft-Start Charging Current	I_{SS}		3.5	5	6.5	μA
Overvoltage Threshold		OVP Rising	18		20	V
Thermal Shutdown Temperature	T_{SD}	Note 5	140	155	170	°C
Thermal Shutdown hysteresis	T_{HYS}	Note 5	5	12	20	°C

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at TA = 25°C on a high effective 4-layer thermal conductivity test board of JEDEC 1-7 thermal measurement standard. The paddle of DFN3x3 packages is the case position for θ_{JC} measurement.

Note 3: The device is not guaranteed to function outside its operating conditions.

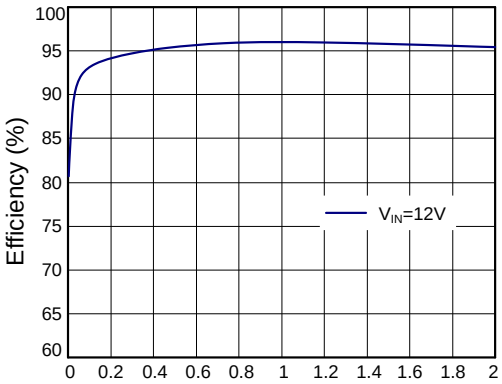
Note 4: Recommended output voltage: V_{OUT} > 1.052 × V_{IN}.

Note 5: Guaranteed by design. Not fully tested in production.

Typical Performance Characteristics

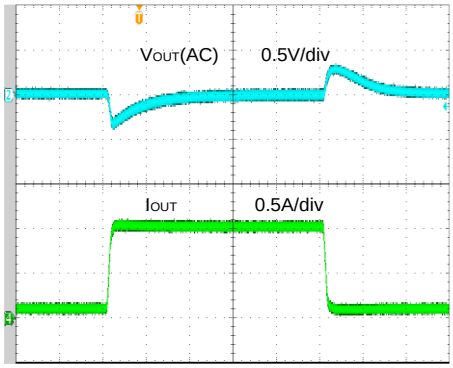
(T_A= 25℃, V_{IN}=12V, V_{OUT} = 16.6V, L = 10μH, C_{OUT}= 20μF, unless otherwise specified.)

Efficiency vs. Load Current



Load Transient

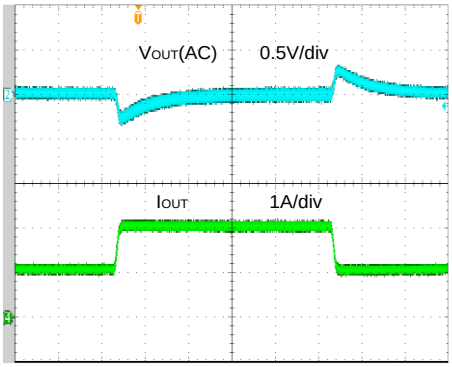
(V_{IN}=12V, V_{OUT}=16.6V, I_{OUT}=50mA~1A)



Time (200μs/div)

Load Transient

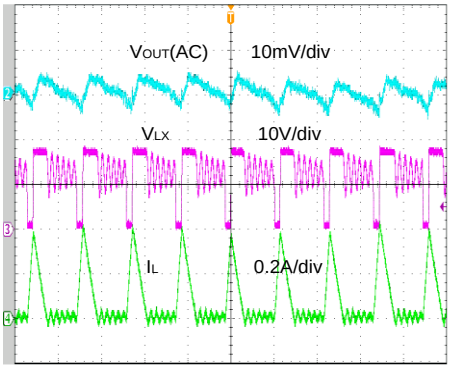
(V_{IN}=12V, V_{OUT}=16.6V, I_{OUT}=1A~2A)



Time (200μs/div)

Output Ripple

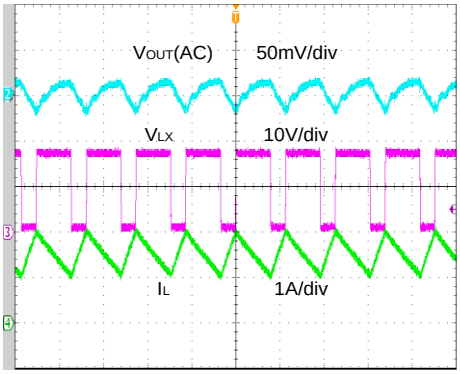
(V_{IN}=12V, V_{OUT}=16.6V, I_{OUT}=50mA)



Time (2μs/div)

Output Ripple

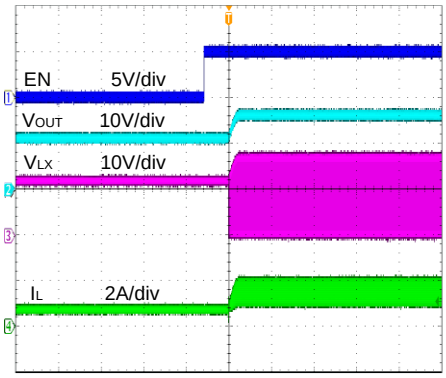
(V_{IN}=12V, V_{OUT}=16.6V, I_{OUT}=1A)



Time (2μs/div)

Startup from Enable

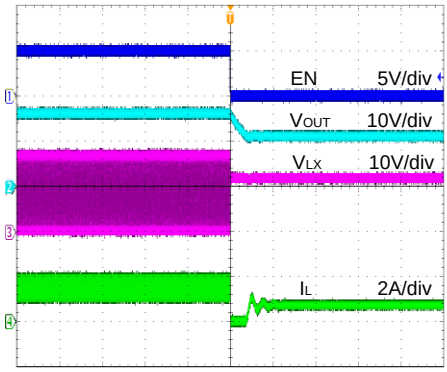
(V_{IN}=12V, V_{OUT}=16.6V, I_{OUT}=1A)



Time (20ms/div)

Shutdown from Enable

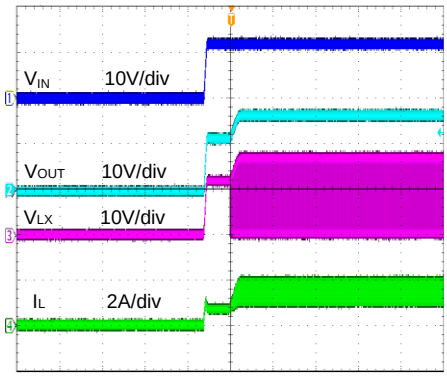
(V_{IN}=12V, V_{OUT}=16.6V, I_{OUT}=1A)



Time (400μs/div)

Startup from V_{IN}

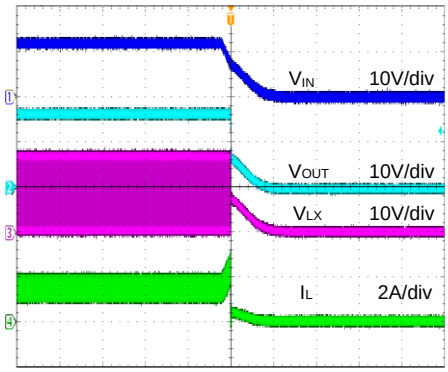
(V_{IN}=12V, V_{OUT}=16.6V, I_{OUT}=1A)



Time (20ms/div)

Shutdown from V_{IN}

(V_{IN}=12V, V_{OUT}=16.6V, I_{OUT}=1A)



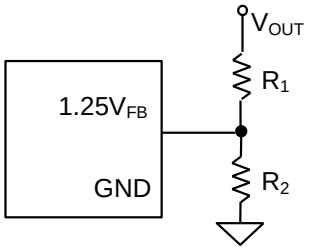
Time (20ms/div)

Application Information

The SY21275 is highly integrated, so only the following components need to be selected for the targeted application specifications: input capacitor C_{IN}, output capacitor C_{OUT}, output inductor L, soft-start capacitor C_{SS}, and feedback resistor-divider R1 and R2.

Feedback Resistor-Divider R1 and R2:
Choose R1 and R2 to program the proper output voltage. To minimize the power consumption under light loads, choose large resistance values (between 10k and 1M) for both resistors. For example, if R1 = 200k, then R2 can be calculated as:

$$R2 = \frac{R1 \times 1.25V}{V_{OUT} - 1.25V}$$



Input Capacitor C_{IN}:
For the best performance, select a typical X5R or better grade ceramic capacitor with a 10V rating, and greater than 10μF capacitance. The component should be placed as close as possible to the module, while also minimizing the loop area formed by C_{IN} and the IN/GND pins. When selecting an input capacitor, ensure that its voltage rating is at least 20% greater than the maximum voltage of the input supply. X5R or X7R dielectric types are the most often selected due to their small size, low cost, surge current capability, and high RMS current rating over a wide temperature and voltage range.

In situations where the input rail is supplied through long wires, it is recommended to add some bulk capacitance like electrolytic, tantalum or polymer type capacitors to reduce the overshoot and ringing caused by the added parasitic inductance.
Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

The ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2\sqrt{3} \times L\, f_{SW} \times V_{OUT}}$$

Output Capacitor C_{OUT}:
Select the output capacitor C_{OUT} to handle the output ripple requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting the component. For the best performance, use an X5R or better grade ceramic capacitor with a 25V rating, and capacitance greater than 10μF.

For applications where the design must meet stringent ripple requirements, the following considerations must be followed:

The output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔI_L) on the output capacitor's ESR (ESR ripple), as well as the stored charge (capacitive ripple). When calculating total ripple, both should be considered.

$$V_{RIPPLE,ESR1} = I_{LREAK} \times ESR$$
$$V_{RIPPLE,ESR2} = I_{LVALLEY} \times ESR$$
$$V_{RIPPLE,CAP} = \frac{I_{OUT} \times (1 - D)}{C_{OUT} \times f_{SW}}$$

The capacitive ripple might be higher because the effective capacitance for ceramic capacitors decreases with the voltage across the terminals. The voltage derating is usually included as a chart in the capacitor datasheet, and the ripple can be recalculated after taking the target output voltage into account.

Boost Inductor L:
There are several considerations in choosing this inductor:

1) Choose the inductance to provide a ripple current that is approximately 40% of the maximum output current. The recommended inductance is calculated as:

$$L = \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \times \frac{V_{OUT} - V_{IN}}{f_{sw} \times I_{OUT,MAX} \times 0.4}$$

where f_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY21275 regulator is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting performance.

2) The selected saturation current rating of the inductor must be greater than the peak inductor current under full-load conditions:

$$I_{SAT,MIN} > \frac{V_{OUT}}{V_{IN}} \times I_{OUT,MAX} + \frac{V_{IN}(V_{OUT} - V_{IN})}{2 \times f_{SW} \times L \times V_{OUT}}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency. It is recommended to choose an inductor with DCR less than 50mΩ to achieve high overall efficiency.

Enable Operation

Pulling the EN pin low (EN < 0.4V) will shut down the device. During shutdown mode, driving the EN pin high (EN > 2.0V) will switch the device on again.

Soft-Start

Connect a capacitor across the SS pin and SGND to program the soft-start time, as follows:

$$t_{SS} = \frac{C_{SS} \times 1.25V}{5\mu A}$$

Diode Selection

A Schottky diode is a good choice for high-efficiency operation because of its low forward-voltage drop and fast reverse recovery. The current rating of the diode must meet the following requirement:

$$I_D(RMS) \approx \sqrt{I_{OUT} \times I_{PEAK}}$$

The Schottky diode reverse-breakdown voltage should be larger than the output voltage.

Loop Compensation

The SY21275 employs a constant-off-time current-mode control scheme. The current-mode control scheme has two feedback loops:

- The inner loop (current loop) does not require any external compensation component.
- The outer loop (voltage loop) is compensated with external components.

In most applications, a Type 2 or Type 2a compensation network, as shown in Figure 3, can be used to stabilize the voltage loop. Type 2 is most widely used, and it works fine for power stages lagging down to -90˚ and where the boost brought by the output capacitor ESR must be canceled. Type 2a is used where the output capacitor ESR effect can be neglected. SY21275 uses a Type 2a compensation network.

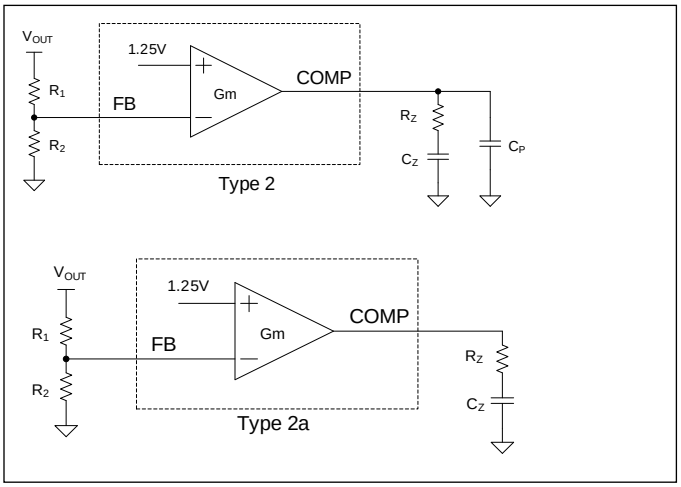


Figure 3. Compensation networks

Follow the steps below to calculate the value of external components for voltage loop compensation:

1. Select the crossover frequency f_C of the closed loop. For the tradeoff of stability and transient response of the system, the recommended crossover frequency is the minimum value of 1/5 of the right-half-plane zero (f_{RHPZ}) and 1/10 of the switching frequency. The system has faster response at higher crossover frequency.

$$f_{RHPZ} = \frac{(1 - D_{MAX})^2 \times V_{OUT}}{2\pi \times L \times I_{OUT}}$$

2. Select an R_Z value of the R-C series combination connected to the COMP pin:

$$R_Z = \frac{V_{OUT}}{g_M \times G_{fc} \times V_{REF}}$$

where g_m is the error amplifier transconductance, which is typically 50μS; G_{fc} is the gain of the power stage at crossover frequency.

$$G_{fc} = \frac{1 - D_{MAX}}{2\pi \times f_c \times C_{OUT} \times R_i}$$

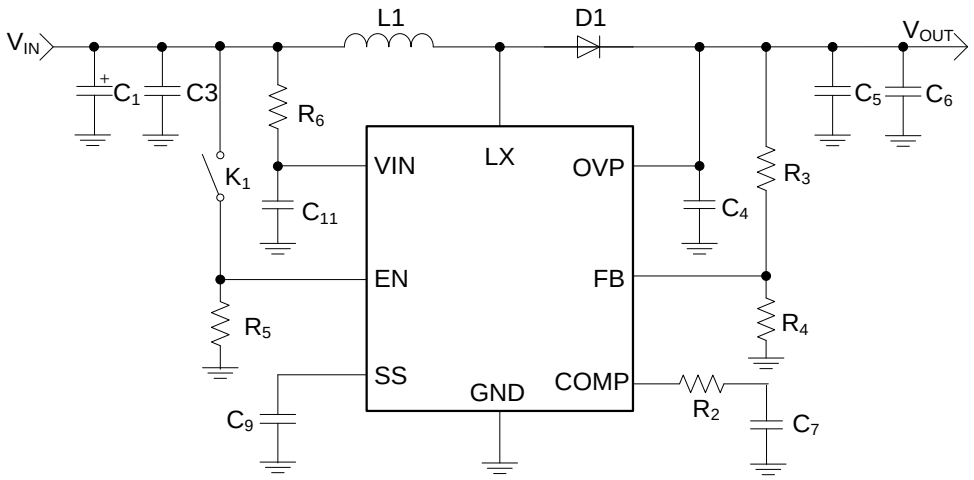
where R_i is the current-sense resistance, which is typically 170mΩ.

3. Select a C_Z value of the R-C series combination connected to the COMP pin. The compensation zero decides the phase margin at the crossover frequency.

Place a compensation zero at or before the dominant pole of R_L and C_O. R_L is the load resistance, which equals V_{OUT}/I_{OUT}.

$$C_Z = \frac{V_{OUT} \times C_{OUT}}{I_{OUT} \times R_Z}$$

Application Schematic



Design Specifications

Input Voltage (V)	Output Voltage (V)	Input Current Limit (A)
8.6-15.9	16.6	3

BOM List

Reference Designator	Description	Part Number	Manufacturer
C1	47μF/50V, Electrolytic Capacitor		
C3	10μF/25V,1206	C3216X5R1E106M	TDK
C4, C11	1μF/50V,0603	C1608X5R1H105K	TDK
C5, C6	10μF/25V,1206	C3216X5R1E106M	TDK
C7	680pF/50V,0603	C1608C0G1H681J	TDK
C9	47nF/50V,0603	C1608X7R1H473K	TDK
R2	44.2kΩ, 0603	RC0603FR-0744K2L	YAGEO
R3	100kΩ,0603	RC0603FR-07100KL	YAGEO
R4	8.06 kΩ,0603	RC0603FR-078K06L	YAGEO
R5	1MΩ,0603	RC0603FR-071ML	YAGEO
R6	5.1Ω,0603	RC0603FR-075R1L	YAGEO
D1	3A/40V	SS34	
L1	10μH	CDRH8D43NP-100NC	Sumida

Recommended Components for Typical Applications

V_{OUT}(V)	R_H(kΩ)	R_L(kΩ)	L(μH)	C_{OUT}
16.6	100	8.06	10	2×10μF/25V/X7R,1206

Layout Design

For optimal design, follow these PCB layout considerations:

- For minimum noise and maximum efficiency, place the following components close to the IC: C_{IN}, L1, R1, and R2.
- To achieve the best thermal and noise performance, maximize the PCB copper area connecting to the GND pin. A ground plane is highly recommended if board space allows.
- C_{IN} must be close to pins IN and GND. Minimize the loop area formed by C_{IN}, V_{IN}, and GND.
- To reduce potential noise:
  - Minimize the PCB copper area connected to the LX pin.
  - R1, R2, and the trace connected to the FB pin must **not** be adjacent to the LX net on the PCB layout.
- If the system chip interfacing with the EN pin has a high impedance state during shutdown mode, and the IN pin is connected directly to a power source such as a Li-ion battery, add a 1MΩ pulldown resistor between the EN and GND pins to prevent noise from falsely triggering the regulator during shutdown mode.

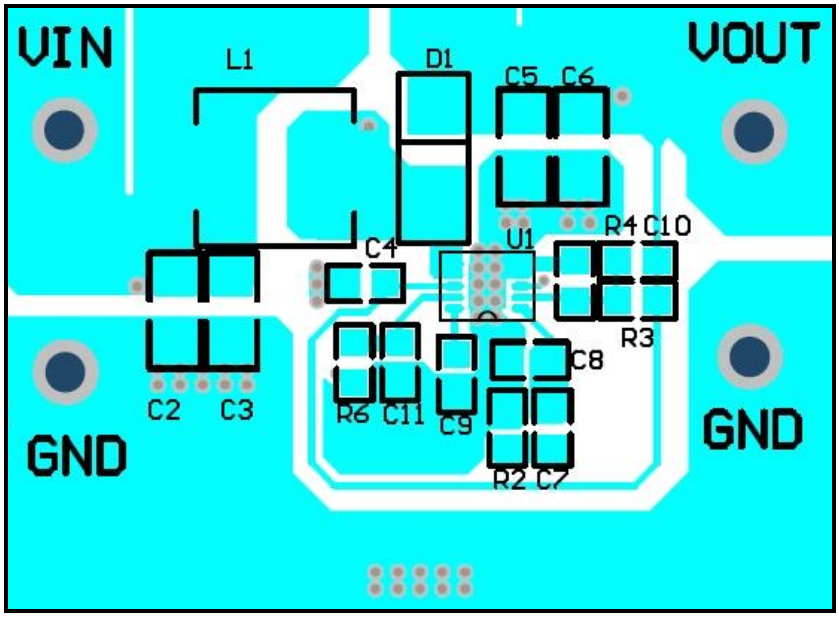
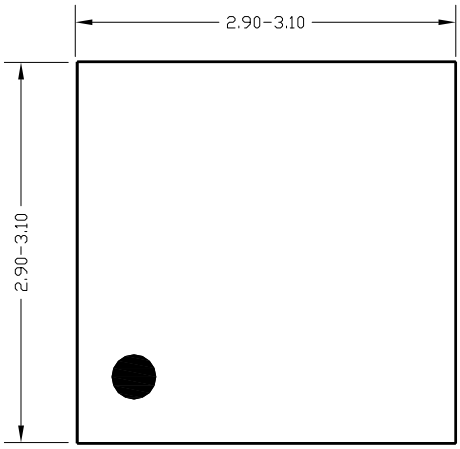
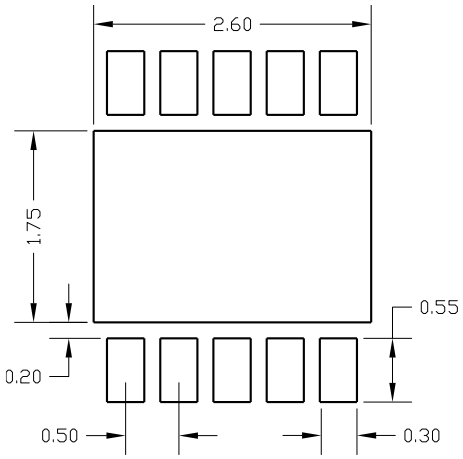


Figure 4. Recommended PCB Layout

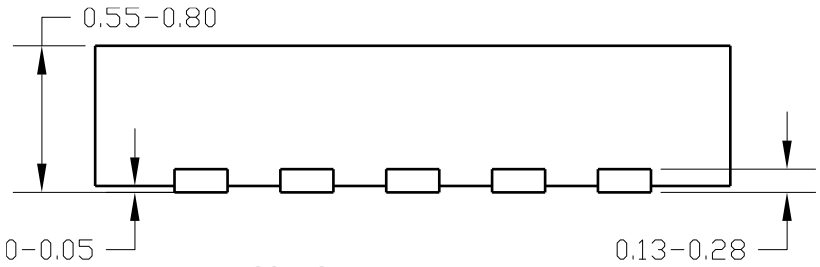
DFN3x3-10 Package outline



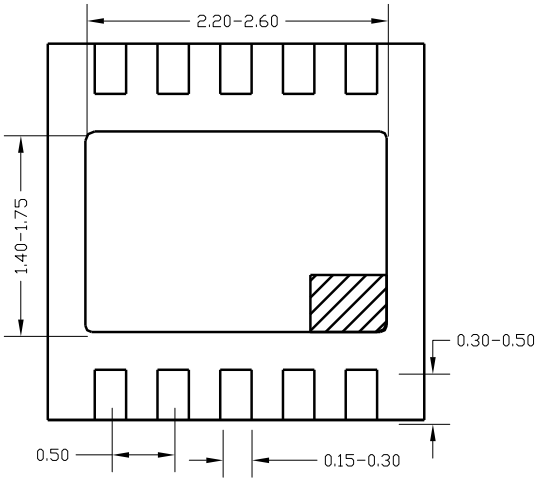
Top View

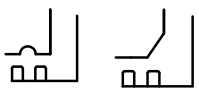


PCB layout (recommended)



Side View





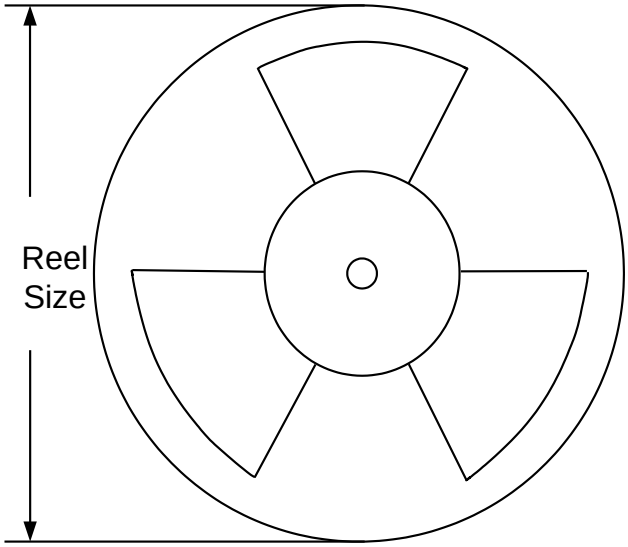
Detail A
Pin1 identifier: two options

Bottom View

Note: *All dimensions are in millimeters and exclude mold flash and metal burr.*

Taping and Reel Specification

Carrier Tape and Reel Specification for Packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel (pcs)
DFN3x3	12	8	13"	400	400	5000

Others: NA

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change
Apr.20, 2023	Revision 1.0	Production Release
Sep.10, 2015	Revision 0.9	Initial Release

IMPORTANT NOTICE

1. **Right to make changes.** Silergy and its subsidiaries (hereafter Silergy) reserve the right to change any information published in this document, including but not limited to circuitry, specification and/or product design, manufacturing or descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to Silergy's standard terms and conditions of sale.

2. Applications. Application examples that are described herein for any of these products are for illustrative purposes only. Silergy makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Buyers are responsible for the design and operation of their applications and products using Silergy products. Silergy or its subsidiaries assume no liability for any application assistance or designs of customer products. It is customer's sole responsibility to determine whether the Silergy product is suitable and fit for the customer's applications and products planned. To minimize the risks associated with customer's products and applications, customer should provide adequate design and operating safeguards. Customer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Silergy assumes no liability related to any default, damage, costs or problem in the customer's applications or products, or the application or use by customer's third-party buyers. Customer will fully indemnify Silergy, its subsidiaries, and their representatives against any damages arising out of the use of any Silergy components in safety-critical applications. It is also buyers' sole responsibility to warrant and guarantee that any intellectual property rights of a third party are not infringed upon when integrating Silergy products into any application. Silergy assumes no responsibility for any said applications or for any use of any circuitry other than circuitry entirely embodied in a Silergy product.

3. **Limited warranty and liability.** Information furnished by Silergy in this document is believed to be accurate and reliable. However, Silergy makes no representation or warranty, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. In no event shall Silergy be liable for any indirect, incidental, punitive, special or consequential damages, including but not limited to lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges, whether or not such damages are based on tort or negligence, warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, Silergy' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Standard Terms and Conditions of Sale of Silergy.

4. **Suitability for use.** Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Silergy components in its applications, notwithstanding any applications-related information or support that may be provided by Silergy. Silergy products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an Silergy product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Silergy assumes no liability for inclusion and/or use of Silergy products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

5. **Terms and conditions of commercial sale**. Silergy products are sold subject to the standard terms and conditions of commercial sale, as published at http://www.silergy.com/stdterms, unless otherwise agreed in a valid written individual agreement specifically agreed to in writing by an authorized officer of Silergy. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Silergy hereby expressly objects to and denies the application of any customer's general terms and conditions with regard to the purchase of Silergy products by the customer.

6. **No offer to sell or license**. Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights. Silergy makes no representation or warranty that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right. Information published by Silergy regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from Silergy under the patents or other intellectual property of Silergy.

For more information, please visit: www.silergy.com