SY205211AMC

Low Capacitance TVS Protection

General Description

SY205211AMC is a bi-directional, low-capacitance electrostatic discharge (ESD) and surge protector designed to provide ESD protection for high-speed data interfaces. SY205211AMC is designed to protect against over-voltage and over-current transient events. It complies with IEC 61000-4-2 (ESD), (±30kV air, ±30kV contact discharge), IEC 61000-4-5 (surge) (25A, 8/20μs).

The combined features of ultra-low capacitance and high ESD robustness make SY205211AMC ideal for applications where arrays are not practical. The low clamping voltage of the SY205211AMC guarantees a minimum stress on the protected IC.

The SY205211AMC is available in a compact SOD-323 package.

Features

- Transient Protection for High-Speed Data Lines
  - IEC61000-4-2 (ESD) ±30kV (Air) ±30kV (Contact)
  - IEC61000-4-5 (Surge) 25A (8/20μs)
- Low Leakage Current: 0.01μA @ V_{RWM} (Typical)
- Working Voltages: 3.3V
- Ultra-Low Capacitance: 0.6pF (Typical)
- Low Clamping Voltage

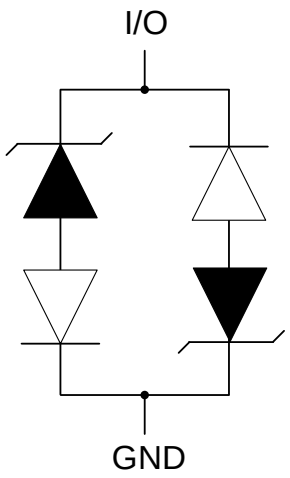
Applications

- Ethernet - 10/100/1000 Base-T
- Desktops, Servers, and Notebooks
- Mobile Phones
- Portable Instruments
- Analog Inputs
- USB Interface

Mechanical Characteristics

- SOD-323 Package
- Marking: Device Code, Date Code
- Packaging: Tape and Reel

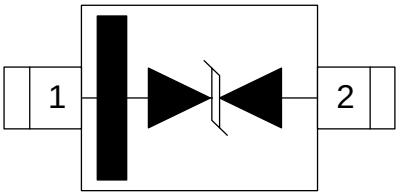
Circuit Diagram



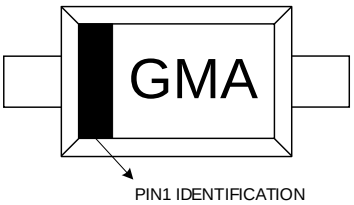
Ordering Information

Part Number	Package Type	Top Mark
SY205211AMC	SOD-323 RoHS Compliant and Halogen Free	GMA

Pinout (Top View)



Marking Codes



Note 1: "G" is device code, fixed.

Note 2: "MA" is date code.

Absolute Maximum Rating				
Parameter	**Symbol**	**Min**	**Max**	**Unit**
Maximum Peak Pulse Current (8/20μs)	I_{PP}		25	A
Maximum Peak Pulse Power (8/20μs)	P_{PK}		155	W
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	-30	30	kV
Operating Temperature	T_{OPT}	-40	+125	℃
Storage Temperature	T_{STG}	-55	+150	°C

Electrical Characteristics T_A = 25℃						
Parameter	**Symbol**	**Test Condition**	**Min**	**Typ**	**Max**	**Unit**
Nominal Reverse Working Voltage	V_{RWM}		-3.3		3.3	V
Reverse Leakage Current @ V_{RWM}	I_R	V_{RWM} = 3.3V, T_A = 25°C Between I/O and GND		0.01	0.1	μA
Reverse Breakdown Voltage @ I_T	V_{t1}	I_T = 1mA Between I/O and GND	3.7			V
Clamping Voltage @ I_{PP}	V_C (1)	I_{PP} = 1A, t_p = 8/20μs Between I/O and GND		8.0		V
Clamping Voltage @ I_{PP}	V_C (1)	I_{PP} = 25A, t_p = 8/20μs Between I/O and GND		13.0		V
Clamping Voltage @ I_{PP}	V_C (1)	I_{PP} = 16A, t_p = 10/100ns Between I/O and GND		9.0		V
Dynamic Resistance	R_{DYN} (1,2)	t_p = 10/100ns Between I/O and GND		0.25		Ω
Parasitic Capacitance	C_{ESD} (1)	V_R = 3.3V, f = 1MHz Between I/O and GND		0.6		pF

Note 1: The device is not guaranteed to function outside its operating conditions.

Note 2: R_{DYN} calculated based on I_{PP}=8A to I_{PP}=16A, t_p = 10/100ns.

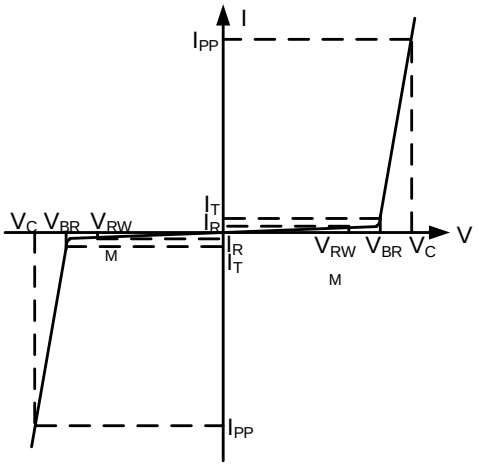
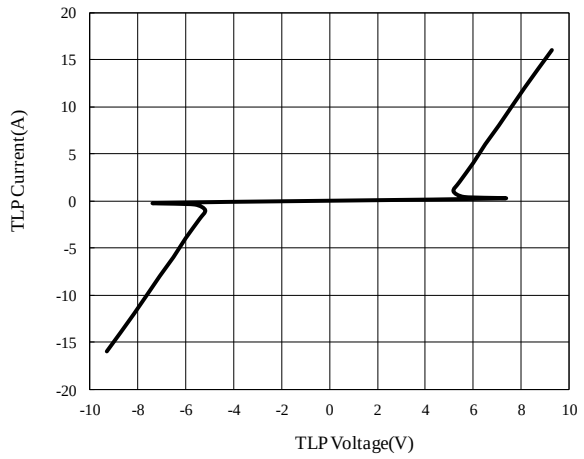


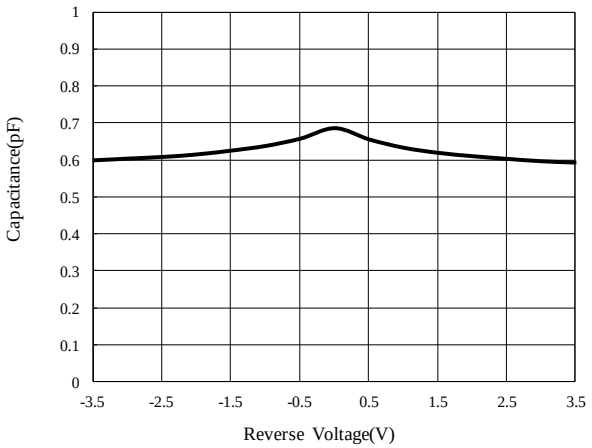
Figure 1. Bi-Directional TVS

Typical Characteristics

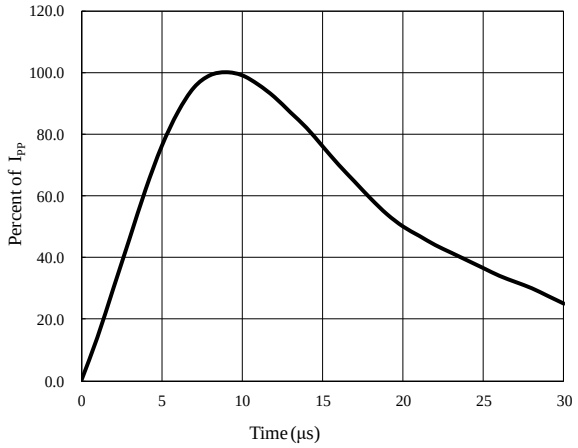
TLP Testing of I/O to GND



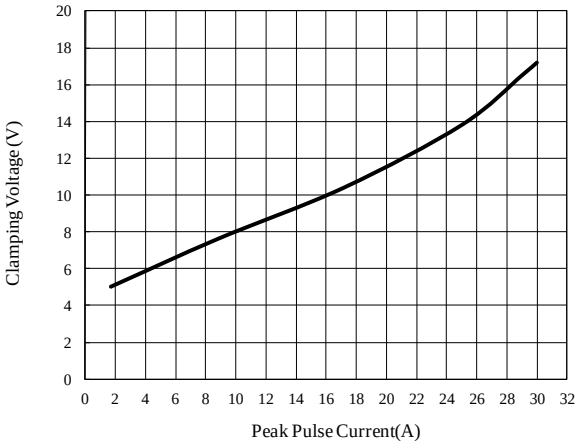
Capacitance vs. Voltage of I/O to GND



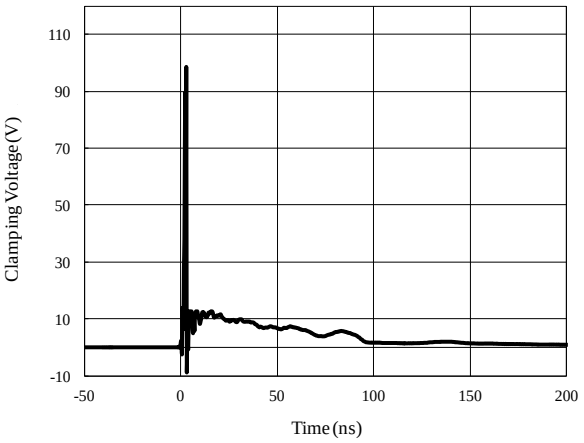
Pulse Waveform



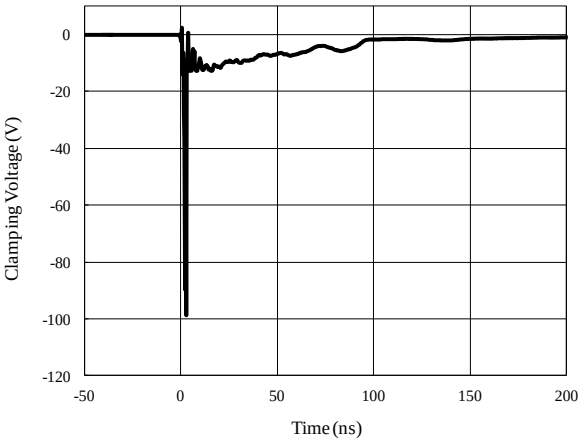
Clamping Voltage vs. Peak Pulse Current(8/20µs)



ESD Clamping of I/O to GND (+8kV Contact per IEC 61000-4-2)



ESD Clamping of I/O to GND (-8kV Contact per IEC 61000-4-2)



Application Information

Ethernet ESD Protection

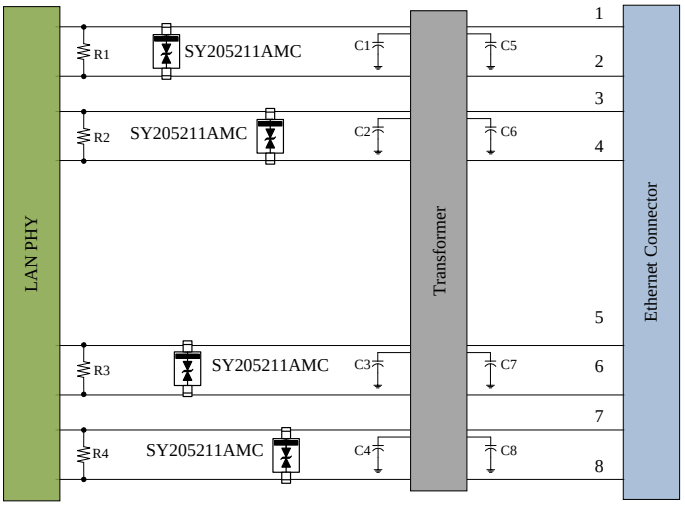


Figure 2. Typical ESD Protection for USB 2.0

In a typical Ethernet system, each interface port contains a twisted line pair through which differential signals flow. These wires are susceptible to damage caused by transient events including ESD, electrical fast transient (EFT), and lighting strikes. Placing a SY205211AMC device after each transformer can protect against transient damage.

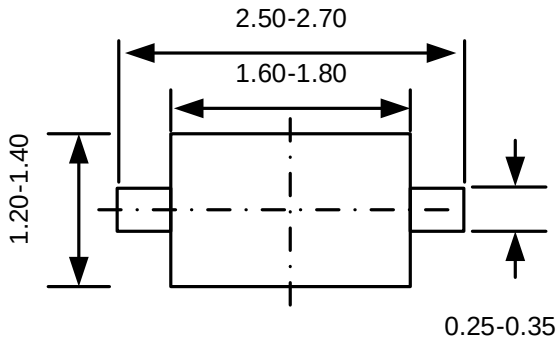
For example, RX- and RX+ are connected to Pin1 and Pin2 respectively. When there is a transient from RX- to RX+, the transient current will be discharged from Pin1 to Pin2 with low impedance. If the transient occurs from RX+ to RX-, the discharged transient current will flow from Pin2 to Pin1. Using SY205211AMC can protect against system damage.

PCB Layout Guidelines

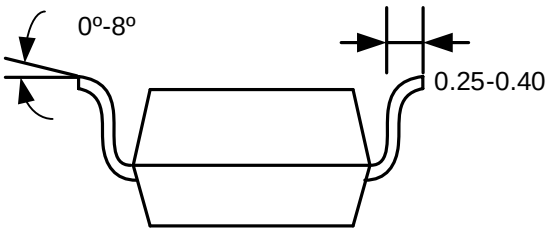
For optimum ESD protection and circuit performance, the following PCB layout guidelines are recommended:

- Place SY205211AMC as close to the connector or terminal ports as possible.
- The distance between the SY205211AMC ground pin and the GND reference path should be as short as possible.
- Use a large via to connect the SY205211AMC pins to the ground.
- Avoid running signals near board edges.
- The SY205211AMC should be placed near the protected lines.

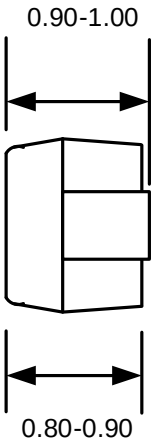
SOD-323 Package Outline



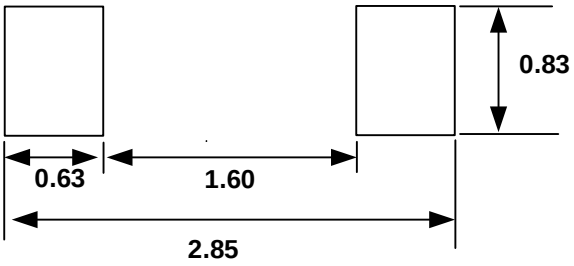
Top View



Side View



Side View

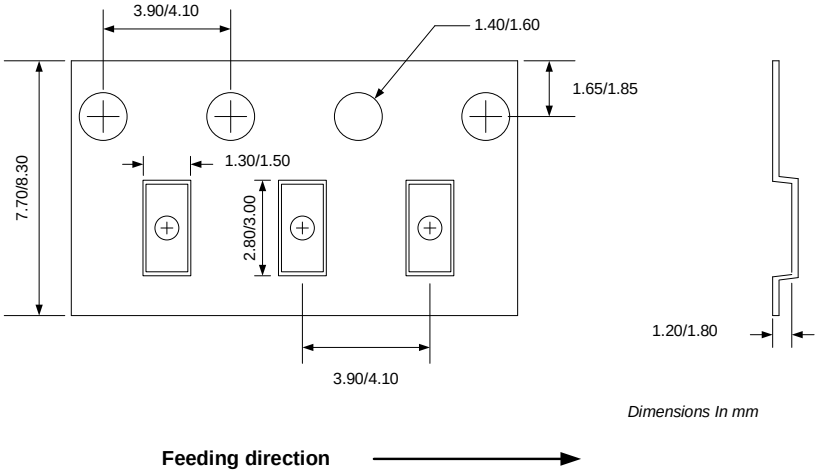


Recommended PCB Layout (Reference only)

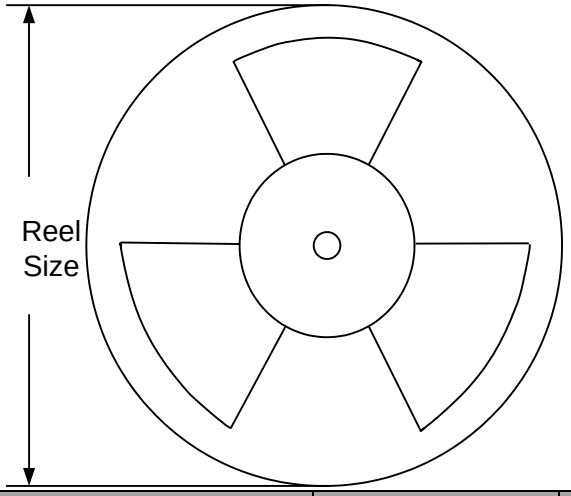
Note: *All dimensions are in millimeters and exclude mold flash and metal burr.*

Tape and Reel Specification

SOD-323 Taping Orientation



Carrier Tape & Reel Specification for Packages



Package Types	Tape Width (mm)	Pocket Pitch(mm)	Reel Size (Inch)	Qty per Reel (pcs)
SOD-323	8	4	7"	3000

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Revision Number	Revision Date	Description	Pages changed
0.9	05/10/2016	Initial Release	
1.0	05/10/2017	Production Release	

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