SY20741

High Efficiency, 2.5A, Multi-Cell Li-Ion Battery Charger

General Description

The SY20741 is a multi-cell Li-Ion battery step-down charger designed for a 4-14V input range, capable of delivering a charge current of up to 2.5A. The charge current can be adjusted using an external resistor, offering flexibility for various portable applications.

The charger features programmable charge timeout and adaptive input power limit functions, enhancing the safety of battery charging operations. The device includes 16V rated power switching and reverse blocking MOSFETs with extremely low ON resistance, ensuring high charge efficiency and simple peripheral circuit design.

Short-circuit, Charge Timeout and temperature protection are provided for reliable operation.

The open-drain STAT output can be used to indicate the battery state of charge.

The SY20741 is available in a compact QFN3×3 package.

Features

- Adaptive Input Power Limit for 4-14V Input Voltage Range
- 4.2V and 4.35V Selectable Cell Termination Voltage
- Integrated Synchronous Buck and Reverse Blocking MOSFET with 16V Rating
- Maximum 2.5A Programmable Charge Current
- +/-0.5% Cell Voltage Accuracy
- Supports Single-Cell or Two-Cell Battery Packs
- External Shutdown Function
- Input Voltage UVLO and OVP
- Thermal Fold-Back Protection
- Overtemperature Protection
- Battery Short-Circuit Protection
- Programmable Charge Timeout
- Charge Status Indication
- Low Profile QFN3×3 Package for Portable Applications

Applications

- Power Banks
- Mobile phones, PDAs, MP3 Players, MP4 Players
- PSP Game Players, NDS Game Players
- Notebooks

Typical Application

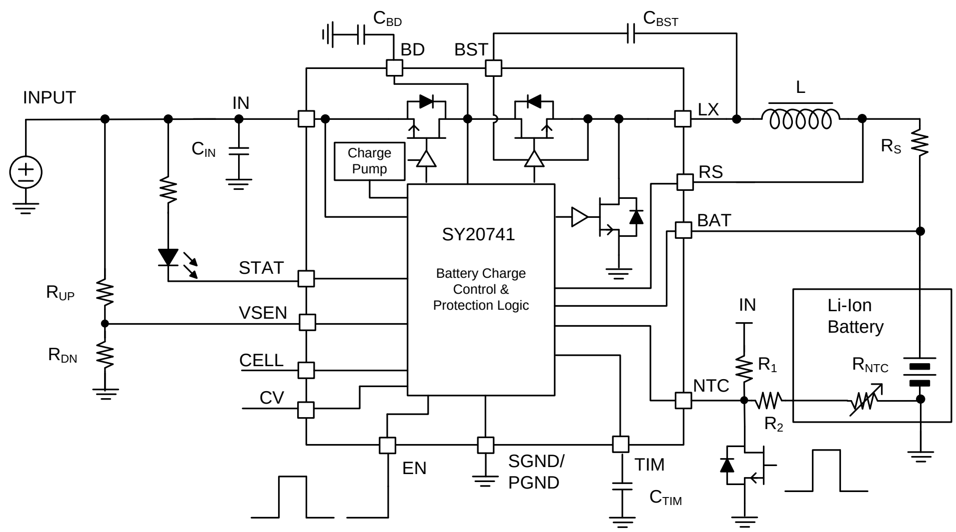


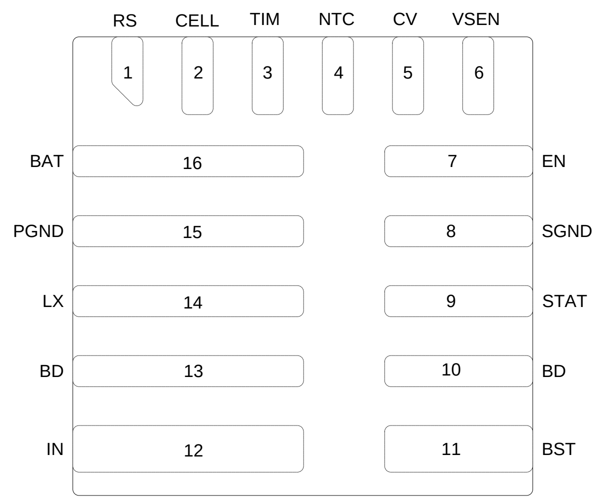
Figure 1. Schematic Diagram

Ordering Information

SY20741 □(□ □)□
└ Temperature Code
Package Code
Optional Spec Code

Ordering Number	Package Type	Top Mark
SY20741QDC	QFN3×3-16	**Ynxyz**

Device code: Yn
x=year code, y=week code, z= lot number code



(QFN3×3-16)

Figure 2 Package Pinout

Pinout (Top View)

Pin Name	Pin Number	Description
RS	1	Charge current sense resistor positive pin. The sensed voltage drop between RS and BAT is used for charge current regulation and charge termination detection.
CELL	2	Battery voltage selection pin. Leave floating for two-cell batteries. Connect to GND for single-cell batteries. The pin can't be pulled high to any bias voltage higher than 3.3V.
TIM	3	Charge timeout programming pin. Connect this pin with a capacitor to the ground to program the timeout protection threshold. The internal current source charges the capacitor for TC mode and fast charge (CC&CV) mode to program the charge time limit. TC charge time limit is about 1/9 of the fast charge time.
NTC	4	Battery thermal sense pin. The voltage on the NTC pin is sensed for battery thermal protection. The UTP threshold is typically 76% of V_{IN}, and the OTP threshold is typically 45% of V_{IN}. The NTC pin can also be used for the adaptive input power limit reference refresh. The adaptive input power limit threshold will be refreshed when NTC is pulled low for more than 100ms. The SY20741 sets the charge current to the trickle value; the device will refresh the adaptive input power limit threshold according to the input voltage. For inputs higher than 6V, the device will clamp the input voltage at V_{IN}-0.6V by regulating the duty cycle of the buck converter. For inputs lower than 6V, the clamped input voltage is set by the VSEN pin.
CV	5	Battery CV voltage selection pin.
VSEN	6	Input voltage sense pin for adaptive input power limit. If the voltage drops to the internal 1.19V reference voltage, V_{IN} will be clamped to the setting value, and the input current will be limited.
EN	7	Enable control pin. Drive to logic high to enable and low logic to disable.

SGND	8	Signal ground pin.

STAT	9	Charge status indication pin. Open drain output. Pull high to IN through a LED to indicate the charge is in progress. When the charge is complete, the LED turns off.
BD	10, 13	Connected to the drain of internal blocking MOSFET. Bypass with at least a 10µF ceramic cap to GND.
BST	11	Bootstrap pin. Supply for the MOSFET's gate driver. Decouple this pin to LX with a 0.1µF ceramic cap.
IN	12	DC power input pin. Connect a MLCC from this pin to the ground to decouple high frequency noise. This pin has OVP and UVLO functions to ensure the charger operates within a safe input voltage range.
LX	14	Switch node pin. Connect to external inductor.
PGND	15	Power ground pin.
BAT	16	Battery voltage sense pin.

Absolute Maximum Ratings (Note 1)

IN, BAT, LX, NTC, STAT, BD, EN, CV, VSEN -- 18V
TIM, CELL-- 4V
BST-LX Voltage -- 4V
RS --- BAT-0.3~BAT+0.3V
LX Pin Current Continuous --- 5A
Power Dissipation, P_D @ T_A = 25°C, QFN3×3-- 2.1W
Package Thermal Resistance (Note 2)
θ_{JA} -- 48 °C/W
θ_{JC} -- 4 °C/W
Junction Temperature Range -- -40°C to 125°C
Lead Temperature (Soldering, 10 sec.) --- 260°C
Storage Temperature Range --- -65°C to 150°C

Recommended Operating Conditions (Note 3)

IN --- 4V to 14V
BAT, LX, NTC, STAT, BD, EN, CV, VSEN---0V to16V
TIM, CELL--- 0V to 3.3V
BST-LX Voltage -- 0V to 3.3V
RS --- BAT-0.25~BAT+0.25V
LX Pin Current Continuous -- 4.5A
Junction Temperature Range --- -40°C to 100°C
Ambient Temperature Range -- -40°C to 85°C

Electrical Characteristics

(T_A=25°C, V_{IN}=5V, GND=0V, C_{IN}=10µF, L=2.2µH, R_S=10mΩ, C_{TIM}=330nF, unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Bias Supply (V_{IN})						
Supply Voltage Operation Range	V_{IN}		4		14	V
Input Voltage Lockout Threshold	V_{UVLO}	V_{IN} rising and measured from IN to ground			4	V
Input Voltage Lockout Hysteresis	ΔV_{UVLO}	Measured from IN to ground		0.2		V
Input Over Voltage Protection	V_{IN_OVP}	V_{IN} rising and measured from IN to ground	13.5			V
Input Over Voltage Protection Hysteresis	ΔV_{OVP}	Measured from IN to ground		0.5		V
Quiescent Current						
Battery Discharge Current	I_{BAT}	V_{IN} absent or EN=Low		5	10	µA
Input Quiescent Current	I_{IN}	Disable charge		0.8	1.1	mA
Oscillator and PWM						
Switching Frequency	f_{SW}			500		kHz
Power MOSFET						
$R_{DS(ON)}$ of Main N-FET	R_{NFET_M}			30		mΩ
$R_{DS(ON)}$ of Rectified N-FET	R_{NFET_R}			55		mΩ
$R_{DS(ON)}$ of Blocking N-FET	R_{NFET_B}			45		mΩ
Voltage Regulation						
Battery Charge Voltage	V_{BAT_REG}	1-cell battery, V_{CV}<0.4V	4.179	4.2	4.221	V
		1-cell battery, V_{CV}>1.5V	4.328	4.35	4.371	
		2-cell battery, V_{CV}<0.4V	8.358	8.4	8.442	
		2-cell battery, V_{CV}>1.5V	8.656	8.7	8.744	
Recharge Threshold Refer to V_{BAT_REG}	ΔV_{RCH}	1-cell battery	50	100	150	mV
		2-cell battery	100	200	300	
Trickle Charge Rising Edge Threshold	V_{TRK}	1-cell battery	2.7	2.8	2.9	V
		2-cell battery	5.4	5.6	5.8	
Adaptive Input Current REF Modify						
NTC Voltage Threshold for Adaptive Input Current Reference Refresh	V_{NTC}	NTC falling edge	0.4			V
NTC Low Time to Enable the Adaptive Input Current Refresh	t_{DET}	Low pulse width		100		ms
Charge Current						
Charge Current Accuracy for Constant Current Mode	I_{CC}	I_{CC}=25mV/R_S	-10%		10%	
Charge Current Accuracy for Trickle Current Mode	I_{TC}	I_{TC}=2.5mV/R_S	-50%		50%	
Termination Current	I_{TERM}	I_{TERM}=2.5mV/R_S	-50%		50%	
Output Voltage OVP						
Output Voltage OVP Threshold	V_{O_OVP}		105%	110%	115%	V_{BAT_REG}
Adaptive Input Power Limit Reference						
Reference for Adaptive Input Power Limit	V_{SEN}		1.16	1.19	1.22	V
The Adaptive Input Power Limit Reference is V_{IN}-ΔV_{AICL}	ΔV_{AICL}	NTC pulls lower than 100ms, and V_{IN} is higher than 6V		600		mV

Timer						
Trickle Current Charge Timeout	t_{TC}		0.36	0.5	0.64	hour
Constant Current Charge Timeout	t_{CC}		3.5	4.5	5.5	hour
Charge Mode Change Delay Time	t_{MC}			30		ms
Termination Delay Time	t_{TERM}			30		ms
Recharge Time Delay	t_{RCHG}			30		ms
Short Circuit Protection						
Output Short Protection Threshold, Falling Edge	V_{SHORT}		1.7	2.00	2.3	V
Auto Shut Down						
Auto Shutdown Voltage Threshold	V_{ASD}	V_{IN} falls, measured from IN to BAT	40	110	180	mV
Auto Shutdown Voltage Threshold Hysteresis	ΔV_{ASD}	V_{IN} rises, measured from IN to BAT		65		
Logical Control						
High Level Logic for Enable Control	V_{ENH}		1.5			V
Low Level Logic for Enable Control	V_{ENL}				0.4	V
High Level Logic for CV	V_{CVH}		1.5			V
Low Level Logic for CV	V_{CVL}				0.4	V
Battery Thermal Protection NTC						
Under Temperature Protection	V_{NTC_UTP}		75%	76%	77%	V_{IN}
Under Temperature Protection Hysteresis	$V_{NTC\_UTP\_HYS}$	Falling edge		5%		
Over Temperature Protection	V_{NTC_OTP}		44%	45%	46%	
Over Temperature Protection Hysteresis	$V_{NTC\_OTP\_HYS}$	Rising edge		1.5%		
Thermal Fold-back and Thermal Shutdown						
Thermal Fold-back Threshold	T_{Fold}			120		ºC
Thermal Fold-back Hysteresis Falling Edge	$T_{FoldHYS}$			20		ºC
Thermal Fold-back Ratio	I_{Fold}			0.25		I_{CC}
Thermal Shutdown Temperature	T_{SD}	Rising threshold		160		ºC
Thermal Shutdown Temperature Hysteresis	T_{SDHYS}			30		ºC

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

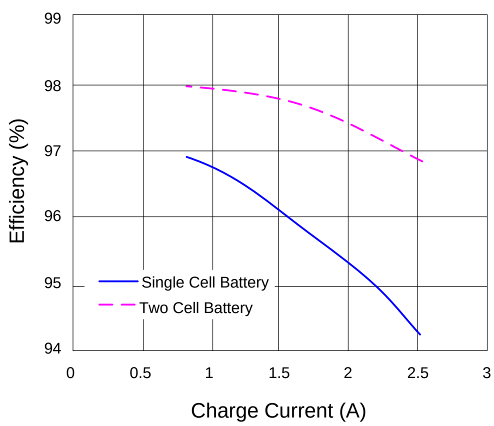
Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective four-layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions.

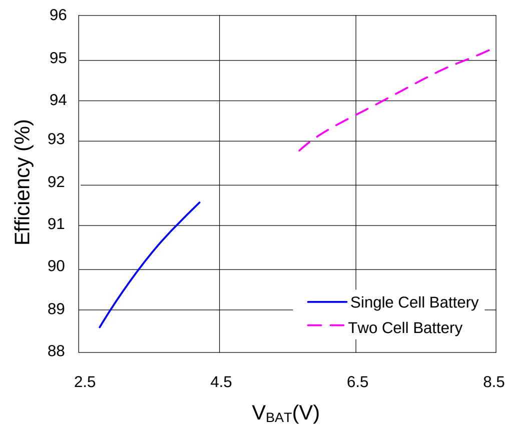
Typical Performance Characteristics

(T_A=25°C, V_{IN}=5V, V_{BAT}=3.6V for single-cell battery applications. V_{IN}=9V, V_{BAT}=7.6V for two-cell battery applications. R_S=10mΩ, C_{TIM}=330nf, unless otherwise specified.)

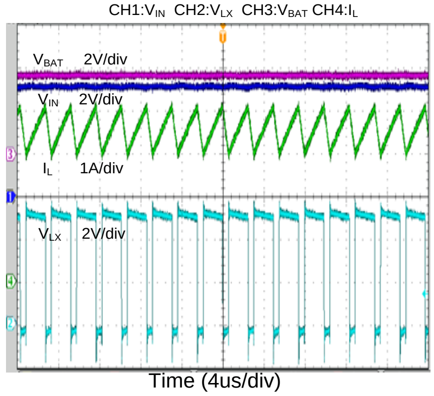
Efficiency vs. Load Current



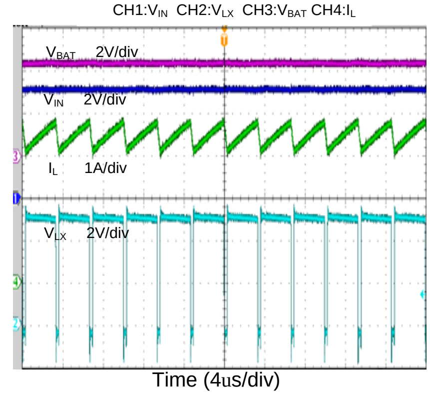
Efficiency vs. Load Current



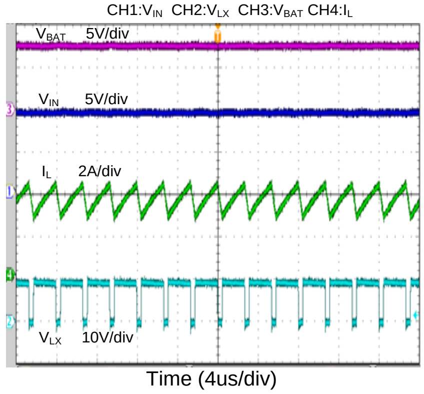
Steady Waveforms
(singl cell battery, CC Mode)
CH1:V_{IN} CH2:V_{LX} CH3:V_{BAT} CH4:I_L



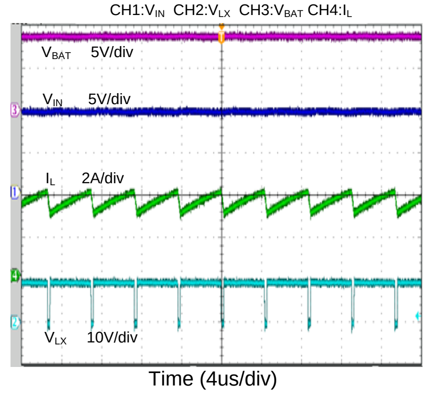
Steady Waveforms
(singl cell battery, CV Mode)
CH1:V_{IN} CH2:V_{LX} CH3:V_{BAT} CH4:I_L



Steady Waveforms
(Two cells battery, CC Mode)
CH1:V_{IN} CH2:V_{LX} CH3:V_{BAT} CH4:I_L



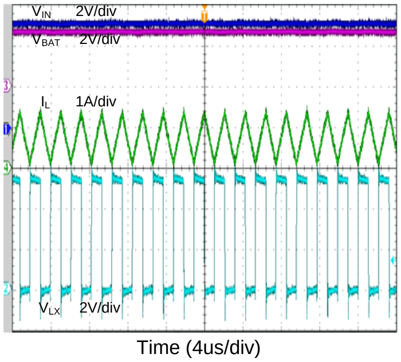
Steady Waveforms
(Two cells battery, CV Mode)
CH1:V_{IN} CH2:V_{LX} CH3:V_{BAT} CH4:I_L



Steady Waveforms

(TC Mode)

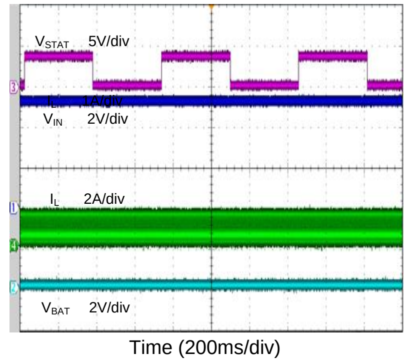
CH1:V_{IN} CH2:V_{LX} CH3:V_{BAT} CH4:I_L



Steady Waveforms

(Short Mode)

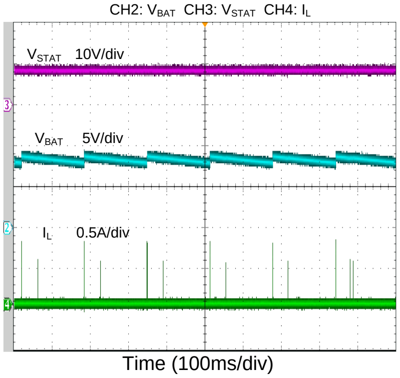
CH1:V_{IN} CH2:V_{BAT} CH3:V_{STAT} CH4:I_L



Steady Waveform When No Battery

(NTC=50% V_{IN}, No battery)

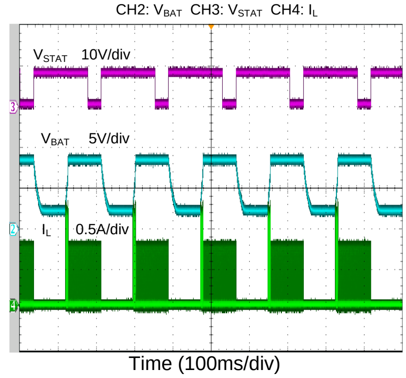
CH2: V_{BAT} CH3: V_{STAT} CH4: I_L



Steady Waveform

(NTC=50% V_{IN},100mA load to BAT,V_{BAT}=3V)

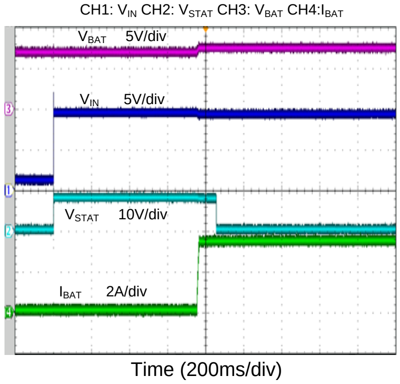
CH2: V_{BAT} CH3: V_{STAT} CH4: I_L



Power On

(Two Cell Battery)

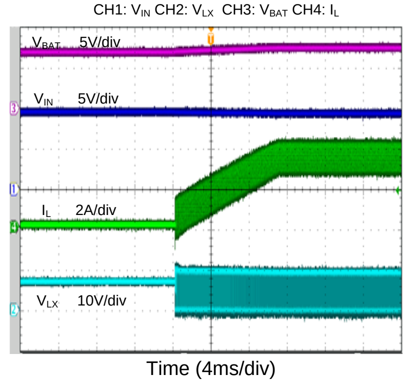
CH1: V_{IN} CH2: V_{STAT} CH3: V_{BAT} CH4:I_{BAT}



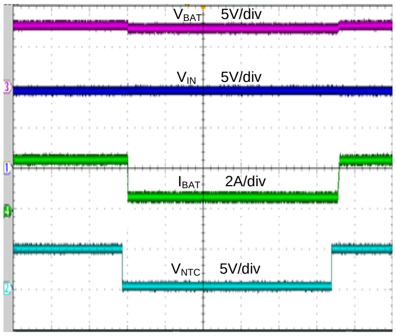
Soft Start

(Two Cell Battery)

CH1: V_{IN} CH2: V_{LX} CH3: V_{BAT} CH4: I_L

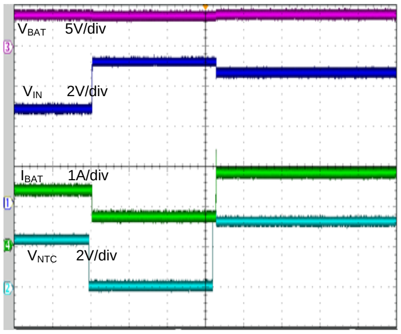


Low Pulse On NTC Pin
(V_{IN}=9V V_{BAT}=7.6V)
CH1: V_{IN} CH2: V_{NTC} CH3: V_{BAT} CH4:I_{BAT}



Time (200ms/div)

Adaptive Input Power Limit Reference Refresh
(Input Adapter changes to 7V/1A V_{BAT}=3.6V)
CH1: V_{IN} CH2:V_{NTC} CH3: V_{BAT} CH4:I_{BAT}



Time (400ms/div)

Application Information

The SY20741 is a multi-cell Li-Ion battery step-down charger designed for a 4-14V input range, and delivers a charge current of up to 2.5A. The charge current can be adjusted using an external resistor, offering flexibility for various portable applications.

The charger features programmable charge timeout and adaptive input power limit functions, enhancing the safety of battery charging.

The device includes 16V rated power switching and reverse blocking MOSFETs with extremely low ON resistance, ensuring high charge efficiency and simple peripheral circuit design.

Charging Status Indication Description:

STAT operates as an open-drain output, requiring a pull-up resistor for charging status indication. To implement this, connect an LED in series with a current limiting resistor from the IN net to the STAT pin. An illuminated LED signifies "Charge-in-Process," an unlit LED indicates "Charge Done" and a flashing LED with a frequency of 1.3Hz means "Fault Mode."

1. **Charge-in-Process:**
   - STAT pin is pulled low.
2. **Charge Done:**
   - STAT pin is high impedance.
3. **Fault Mode:**
   - In Fault Mode, the LED alternates between high and low voltage at a frequency of 1.3Hz.
   - Faults leading to Fault Mode include input OVP, BAT OVP, BAT short, BAT UTP, BAT OTP, timeout, and thermal shutdown.

Buck Charger Switching Mode Operation

Switching Mode Control Strategy:

The SY20741 utilizes quasi-fixed frequency control to simplify the internal close-loop compensation design. The frequency is quasi-fixed at 500kHz, allowing for minimized peripheral circuit design for size optimization. Additionally, during light load operation, the OFF time of the main switch is extended to achieve frequency fold back for improved efficiency.

Operation Principle:

When connected to an adapter, the SY20741 functions as a synchronous buck mode battery charger.

The charger control loops adapt to various charging modes based on battery state, including constant current charge mode, constant voltage charge mode, trickle charge mode as well as battery faults including battery short. The charge curve graph below illustrates the corresponding charge currents for each mode.

In the constant voltage mode, the charger halts charging if the current falls below the termination current. It resumes when the battery voltage decreases below the recharge voltage threshold.

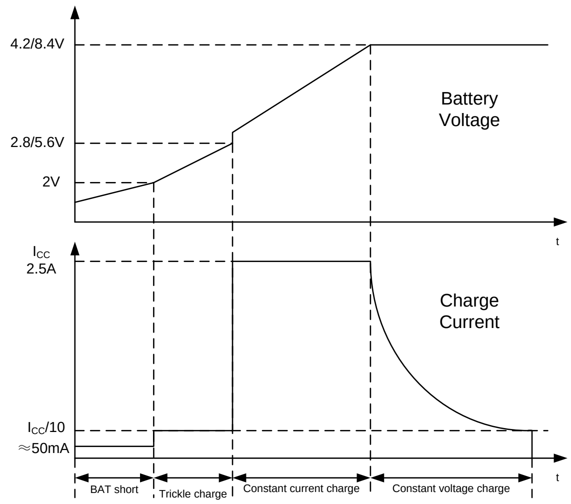


Figure 3. Battery Charge Modes

Adaptive Input Power Limit:

The SY20741 offers adaptive input power limiting by adjusting the current based on the input voltage. The charger automatically reduces the charge current when the IN voltage drops to the adaptive input power limit reference V_{REF}.

For a standard 5V adapter, V_{REF} is determined by the V_{SEN} pin and is calculated as follows:

$$V_{REF} = 1.19 \times \frac{R_{UP} + R_{DN}}{R_{DN}}$$

If the IN voltage is higher than 6V, V_{REF} is calculated using the equation:

$$V_{REF} = V_{IN} - \Delta V_{AICL}$$

Where:

- ΔV_{AICL} has a typical value of 0.6V.
- V_{IN} is the input voltage when the adapter is inserted.
- V_{REF} is resampled following a low pulse on the NTC pin lasting more than 100ms, provided that

the adapter is consistently present.

When the NTC pin is pulled low continuously, the charge current is set to the trickle value; battery thermal protection and adaptive input power limit functions are disabled.

Charger Protection Features:

In charge mode, the SY20741 has the following device and battery protection features:

Input Overvoltage Protection: SY20741 offers IN overvoltage protection. It will turn off the switching charger when an input OVP occurs. The device will resume normal operation when the fault is removed.

BAT Overvoltage Protection: SY20741 will stop charging when a BAT OVP event occurs. The device will resume normal operation when the fault is removed.

Timeout Protection: The charger is designed to detect a faulty battery. If the charger operates beyond the safety time determined by C_{TIM}, it will stop charging and enter a latched-off state. Recycling the input voltage is necessary to release this fault.

Battery Thermal Protection: The converter will halt switching if the NTC voltage falls below the OTP threshold while remaining above 0.4V or exceeds the UTP threshold. The device will automatically recover once the fault is resolved.

Thermal Shutdown Protection: The device will stop operation when the junction temperature is higher than T_{SD} (160°C typ.). The device will resume normal operation when the die temperature drops below T_{SD}-T_{SDHYS}.

Design Procedure

The following paragraphs provide information on the selection process for the input capacitor (C_{IN}), BD pin decoupling (C_{BD}), output capacitor (C_{OUT}), inductor (L), NTC resistors (R1 and R2) charging current sense resistor (Rs), and the timer capacitor (C_{TIM}) based on the target application specifications.

NTC Resistor:

The SY20741 monitors battery temperature by measuring the input voltage and NTC voltage. The controller triggers the UTP or OTP when the rate K ($K = V_{NTC}/V_{IN}$) reaches the threshold for UTP (K_{UT}) or OTP (K_{OT}). The temperature sensing network is shown below:

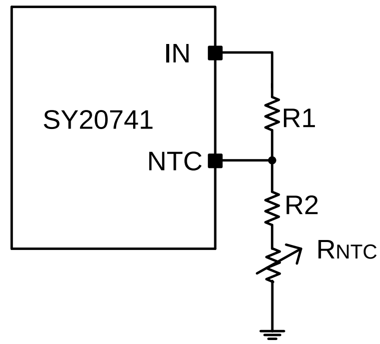


Figure 4. UTP /OTP configuration using R1 and R2

The calculation steps are:

1. Define K_{UT}; K_{UT} =75~77%
2. Define K_{OT}; K_{OT} =44~46%
3. Assume the resistance of the battery NTC thermistor is R_{UT} at the UTP threshold and R_{OT} at the OTP threshold.
4. Calculate R2:

$$R2=\frac{K_{OT}(1-K_{UT})R_{UT}-K_{UT}(1-K_{OT})R_{OT}}{K_{UT}-K_{OT}}$$

5. Calculate R1:

$$R1=(1/K_{OT}-1)(R2+R_{OT})$$

When typical values (K_{UT} =76% and K_{OT}=45%) are chosen, then:

$$R2=0.348R_{UT}-1.348R_{OT}$$
$$R1=1.222(R2+R_{OT})$$

The SY20741 accepts various NTC divider circuits. For the method below, R_1 and R_2 can be calculated by using the following equations:

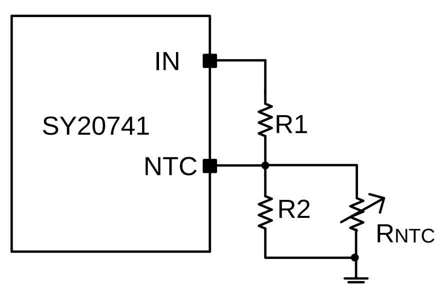


Figure 5. Alternate UTP /OTP configuration

$$R2=\frac{R_{OT}\times R_{UT}\times(K_{UT}-K_{OT})}{K_{OT}\times K_{UT}\times(R_{OT}-R_{UT})+R_{UT}\times K_{OT}-R_{OT}\times K_{UT}}$$

$$R1=\frac{R2\times R_{UT}\times(1-K_{UT})}{K_{UT}\times(R2+R_{UT})}$$

When typical values (K_{UT} =76% and K_{OT}=45%) are chosen, then:

$$R2=\frac{0.31R_{UT}\times R_{OT}}{0.108\times R_{UT}-0.418\times R_{OT}}$$

$$R1=\frac{0.316R2\times R_{UT}}{R_{UT}+R2}$$

Charging Current Sense Resistor Rs:

The charging current sense resistor R_S is calculated as follows:

$$R_S=\frac{25mV}{I_{CC}}$$

Where:

- The I_{CC} is the battery's constant charging current, unit: A.
- Units are in mΩ

Timer Capacitor C_{TIM}:

The charger provides a programmable safety charging timer. The charging time is programmed by the capacitor connected between the TIM pin and GND. The capacitance is calculated as follows:

$$C_{TIM}=2\times10^{-11}\ S\times T_{CC}$$

Where:

- T_{CC} is the permitted fast charging time, unit: s.
- Units are in F.

Input Capacitor C_{IN}

The ripple current through the input capacitor can be estimated using the following equation:

$$I_{C_{BD}\_MIN}=I_{CC}\sqrt{D(1-D)}$$

To minimize system noise, place a typical X7R or a better-grade ceramic capacitor close to the IN and GND pins. Minimize the loop area formed by C_{IN} and the IN/GND pins. The capacitor should be selected based on the ability to handle the ripple current. Paralleling capacitors can be used to meet the ripple requirements. A value of 10 µF is sufficient for most applications.

BD Pin Decoupling C_{BD}:

Place a typical X7R or a better-grade ceramic capacitor close to the BD and GND pins. Minimize the loop area formed by C_{BD} and the BD/GND pins. A value of 10 µF is recommended for most applications.

Output Capacitor C_{OUT}:

The output capacitor is selected to handle the output ripple noise requirements. Both steady-state ripple and transient requirements must be considered when selecting this capacitor. For the best performance, it is recommended to use an X7R or a better-grade ceramic capacitor with at least 10µF capacitance.

Output Inductor L:

When selecting the inductor, consider the following factors:

1. Choose the inductance to achieve the desired ripple current. It is suggested that the ripple current be approximately 40% of the average input current.
2. The minimum inductance is calculated as follows:

$$L=\frac{V_{OUT}\times(1-V_{OUT}/V_{IN,MAX})}{F_{SW}\times I_{OUT,MAX}\times 40\%}$$

Where:

- F_{SW} is the switching frequency.
- $I_{OUT,\ MAX}$ is the maximum load current.

The SY20741 is tolerant to different ripple current amplitudes. Therefore, the final inductance selection can deviate slightly from the calculated value without significantly affecting performance.

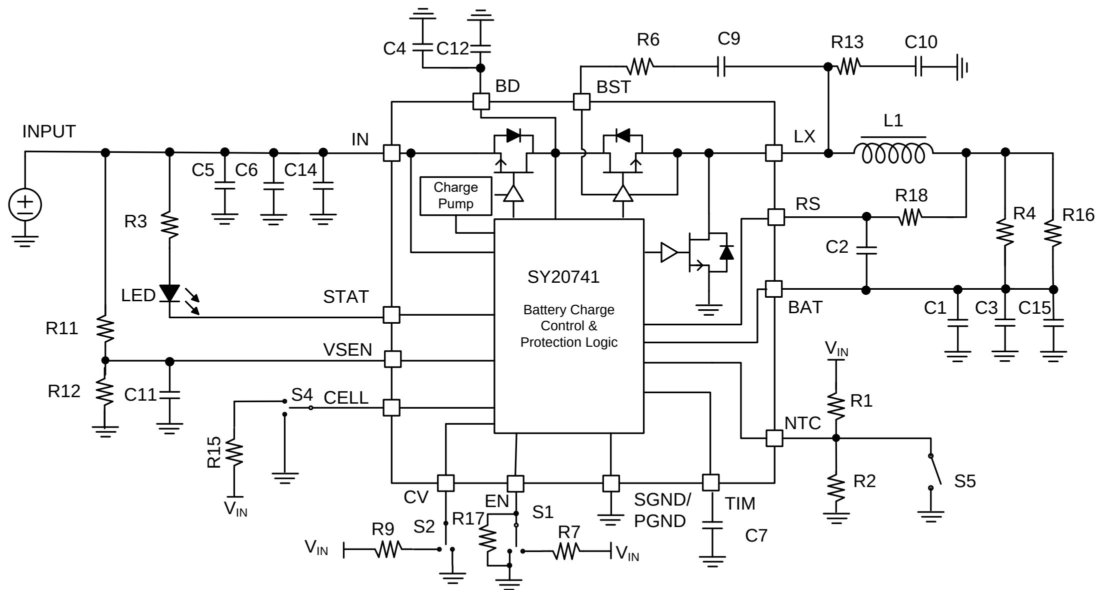
3. The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN}>I_{OUT,MAX}+\frac{V_{OUT}\times(1-V_{OUT}/V_{IN,\ MAX})}{2\times F_{SW}\times L}$$

4. The DC resistance (DCR) of the inductor and the core loss at the switching frequency should be sufficiently low to meet the desired efficiency requirements. It is recommended to select an inductor with DCR < 20mΩ.

The SY20741 includes internal compensation circuits that influence the choice of the inductor. It is advised to avoid inductors outside the range of 0.68µH to 3.3µH. A 2.2µH inductor is well-suited for typical applications and covers most use cases.

Schematic



BOM List

Designator	Description	Part Number	Manufacturer
U1	High Efficiency, 2.5A, Multi-Cell Li-Ion Battery Charger	SY20741QDC	Silergy
L1	INDUCTOR 2.2uH	SPM6530T-2R2M	TDK
C1,C3	16V/22µF,1206,X5R	C3216X5R1C226M160AB	TDK
C4,C5,	16V/10µF,1206,X7R	C3216X7R1C106K160AC	TDK
C7	330nF	C1608X7R1E334K080AC	TDK
C9	25V/47nF	C1608X7R1E473K080AA	TDK
LED	LED Chip 0603		
R1,R17,R9,R12	10kΩ, 0603, 1%		
R2	15kΩ, 0603, 1%		
R3	5.1kΩ, 0603, 1%		
R4	10mΩ, 1206, 1%		
R6, R18	0Ω, 0603, 1%		
R7	22kΩ, 0603, 1%		
R11	27.5kΩ,, 0603, 1%		
C2,C6,C10,C11, C12,C14,C15, R13,R15,R16	NA		
S1,S2,S4	Switch		
S5	Key		

*Note: The resistor R2 on the EVB set the NTC pin's voltage equals 60%V_{IN}, thus can make the IC enter Charger mode. In real Battery application circuit, please replace it with a negative thermal resistor to ground to achieve OTP and UTP protection.

PCB Layout Guide:

For best performance of the SY20741, the following guidelines must be followed:

1. Enhance thermal and noise performance by maximizing the PCB copper area connected to the GND pin.
2. Place C_{BD} and L close to the device to minimize noise problems and improve efficiency.
3. Place C_{BD} close to the BD and GND pins. The loop area formed by C_{BD} and GND must be minimized. Refer to Figure 2 below for the recommended C_{BD} layout design.
4. Minimize the PCB copper area associated with the LX pin to reduce EMI.
5. The capacitor (C_{TIM}) and the trace connecting to the TIM pin must not be adjacent to the LX net on the PCB layout to avoid noise problems.
6. Place the current sense resistor adjacent to the junction of the inductor and output capacitor. The traces from the sense connection points on the sense resistor to the device pins should be close to each other to minimize the loop area. Do not route the sense nets across high current paths. Refer to Figure 2 below for the recommended PCB layout design.

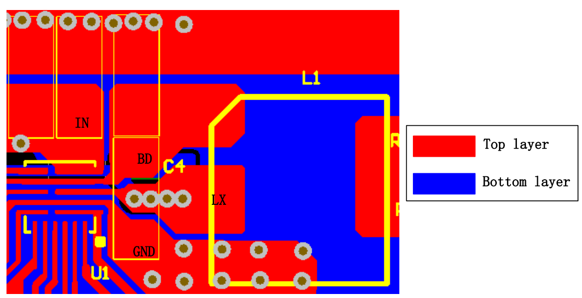


Figure 2. C_{BD} Layout Suggestion

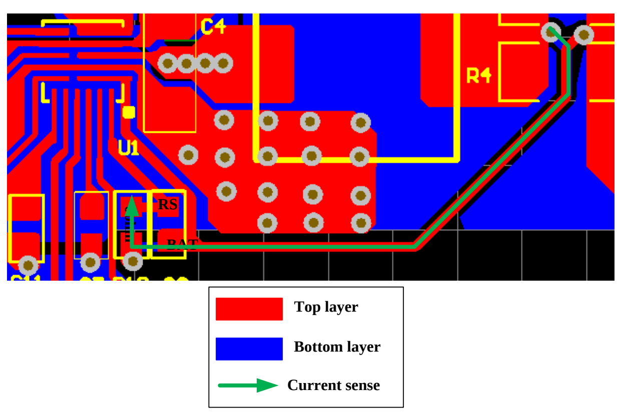
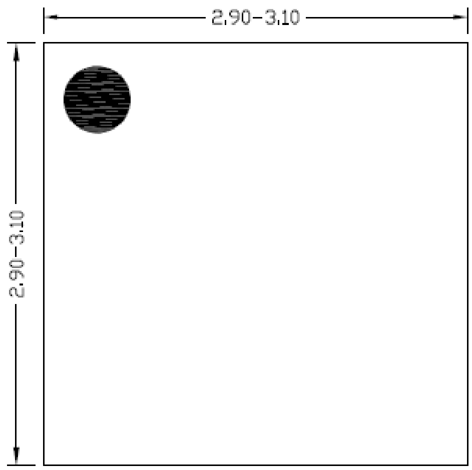
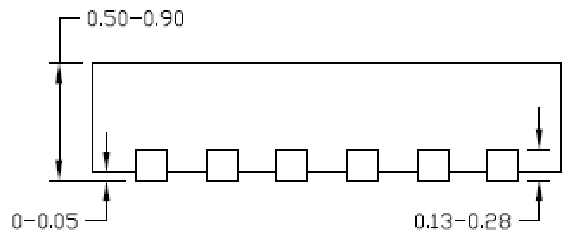


Figure 3. PCB Layout Suggestion

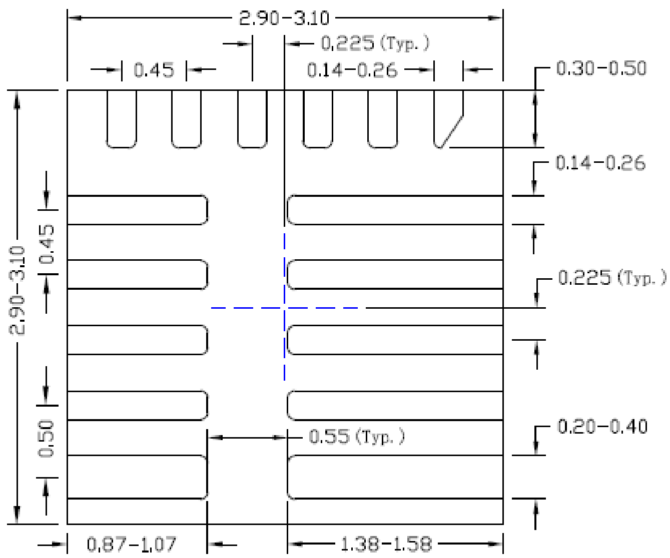
QFN3×3-16 Package Outline Drawing



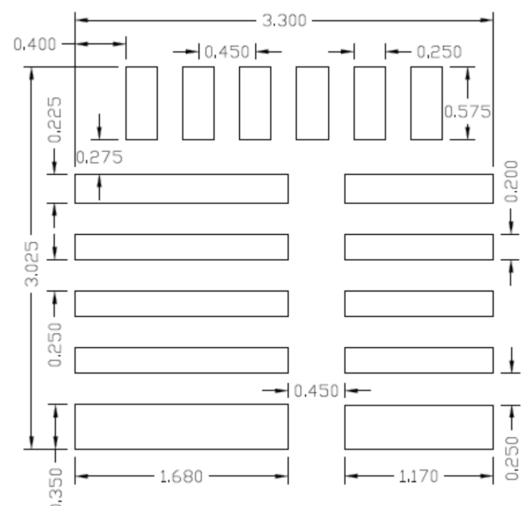
Top View



Side View



Bottom View

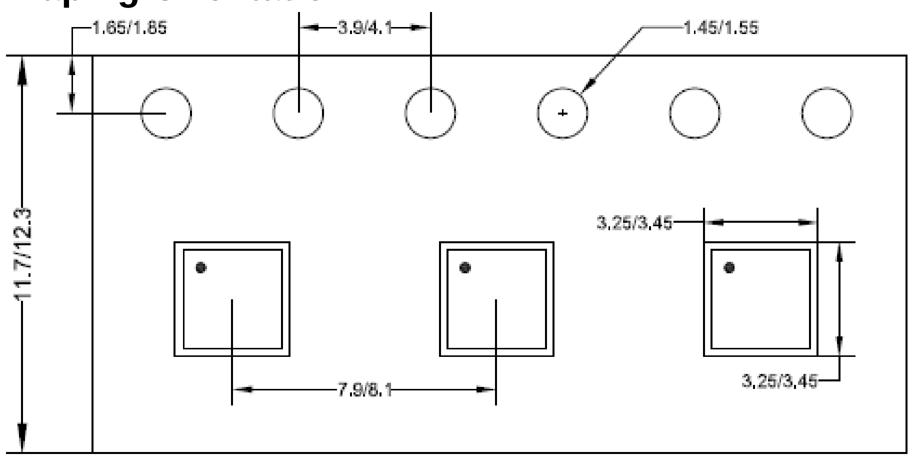


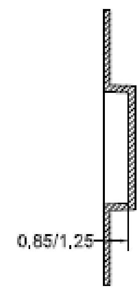
Recommended PCB Layout (Reference Only)

Note: All dimensions are in millimeters and exclude mold flash and metal burr.

Taping & Reel Specification

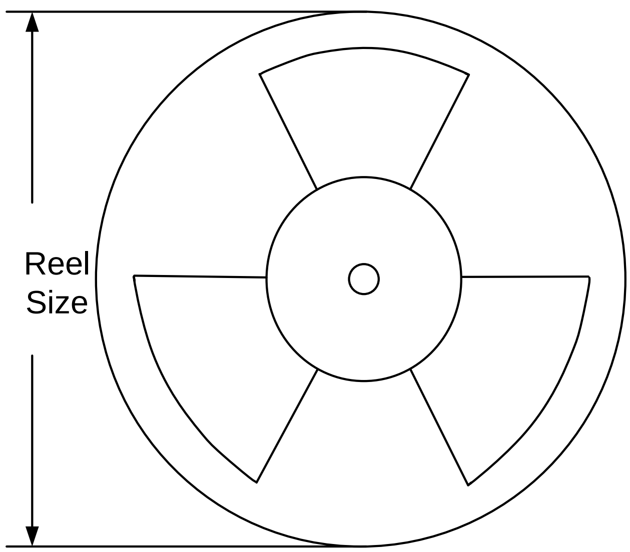
QFN3x3 Taping Orientation





Feeding direction →

Carrier Tape & Reel Specification for Packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN3x3	12	8	13"	400	400	5000

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change
Mar.26, 2020	Revision 0.9B	Change "V_{NTC_UTP}" min value from 74% to 75%, typical value from 75% to 76% , max value from 76% to 77%
Nov.16, 2017	Revision 0.9A	1. Change "V_{NTC_UTP}" min value from 70% to 74%, max value from 80% to 76%. 2. Change "V_{NTC_OTP}" min value from 43% to 44%, max value from 47% to 46%. 3. In Page 10, Change from "Define KUT, KUT =70~80%" to "Define KUT, KUT =74~76%", change from "Define KOT, KOT =43~47%" to "Define KOT, KOT =44~46%". 4. In page 10, chage the formula from $R_S = \frac{25}{I_{CC}}$ $R_S = \frac{25mV}{I_{CC}}$ 5. In page 11, change the formula from "CTIM=2×10-11TCC" to "CTIM=2×10-11S×TCC".
Aug. 9, 2017	Revision 0.9	Initial Release

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