

# SY205206DXC Low Capacitance TVS Protection

### **General Description**

SY205206DXC is a low-capacitance transient voltage suppressor (TVS) designed to provide electrostatic discharge (ESD) protection for high-speed data interfaces. With a typical capacitance of 2pF, SY205206DXC is designed to protect against overvoltage and over-current transient events. It complies with IEC61000-4-2 (ESD) (±30kV air, ±30kV contact discharge), IEC61000-4-5 (surge) (10A, 8/20µs).

Each SY205206DXC device can protect one data line. The SY205206DXC is available in a compact DFN0.6×0.3-2 package.

#### Features

- Transient Protection for High-Speed Data Lines
  - IEC61000-4-2 (ESD) ±30kV (air) ±30kV (contact)
    IEC61000-4-5 (surge) 10A (8/20µs)
- For Operating Voltage of 5V and Below
- Protects One Data Line
- Low Capacitance: 2pF
- Low Leakage Current: 0.01µA @ V<sub>RWM</sub> (typical)
- Low Clamping Voltage
- Each I/O pin withstands over 1000 ESD strikes for ±8kV contact discharge.

### Applications

- USB 2.0
- Portable Electronics
- Desktops, Servers, and Notebooks
- Mobile Phones
- Digital Camera Ports

### **Mechanical Characteristics**

- DFN0.6×0.3-2 Package
- Marking: Device Code, Date Code
- Packaging: Tape and Reel

### **Circuit Diagram**





# SY205206DXC

# **Ordering Information**

Part Number	Package Type	Top Mark
SY205206DXC	DFN0.6×0.3-2 RoHS Compliant and Halogen Free	W

# **Marking Codes**

Note 1: "W" is device code, fixed.

Absolute Maximum Rating					
Parameter	Symbol	Min	Мах	Unit	
Maximum Peak Pulse Current (8/20µs)	PP		10	Α	
Maximum Peak Pulse Power (8/20µs)	Ррк		100	W	
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	VESD	-30	30	kV	
Operating Temperature	T <sub>OPT</sub>	-40	+85	°C	
Storage Temperature	Tstg	-55	+150	°C	

Electrical Characteristics T <sub>A</sub> = 25°C						
Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Nominal Reverse Working Voltage	V <sub>RWM</sub>		-5		5	V
Reverse Leakage Current @ V <sub>RWM</sub>	I <sub>R</sub>	$V_{R} = 5V, T_{A} = 25^{\circ}C$		0.01	0.1	μA
Reverse Breakdown Voltage @ IT	V <sub>t1</sub>	I <sub>T</sub> = 1mA	5.6			V
Clamping Voltage @ IPP	V <sub>C</sub> (1)	$I_{PP} = 16A, t_p = 10/100ns$		9		V
Clamping Voltage @ IPP	V <sub>c</sub> (1)	I <sub>PP</sub> = 10A, t <sub>p</sub> = 8/20µs		9.5		V
Dynamic Resistance	R <sub>DYN</sub> (1,2)	t <sub>p</sub> = 10/100ns		0.17		Ω
Parasitic Capacitance	C <sub>ESD</sub> (1)	$V_R = 0V, f = 1MHz$		2	3	pF

Note 1: The device is not guaranteed to function outside its operating conditions.

Note 2:  $R_{DYN}$  calculated based on IPP=8A to IPP=16A,  $t_p = 10/100$ ns.

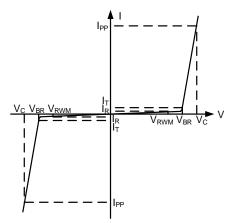
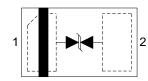


Figure 1. Bi-Directional TVS

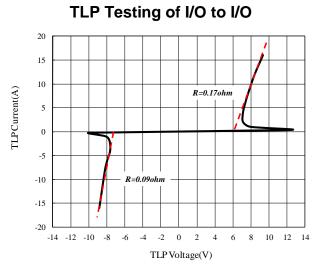
art Number	Package Type	Top Mark			
7205206DXC	DFN0.6×0.3-2 RoHS Compliant and Halogen	W			

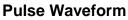
# Pinout (Top View)

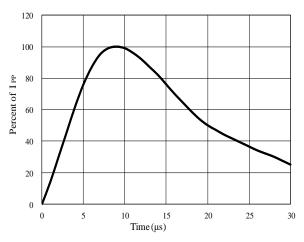




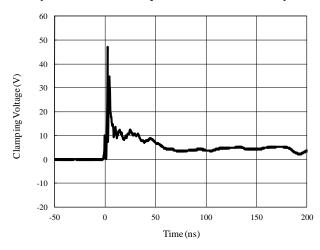
# **Typical Characteristics**



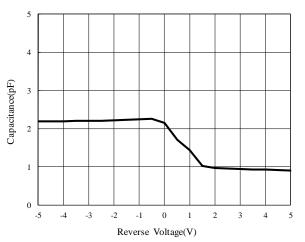




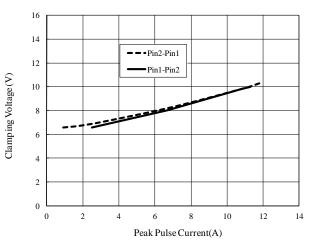
ESD Clamping of I/O to I/O (+8kV Contact per IEC 61000-4-2)



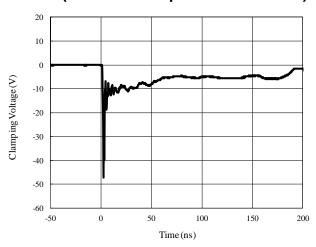




#### Clamping Voltage vs. Peak Pulse Current (8/20µs)



ESD Clamping of I/O to I/O (-8kV Contact per IEC 61000-4-2)





# **Application Information**

SY205206DXC is designed to protect one bi-directional data line against over-voltage and over-current transient events by clamping it to an acceptable reference.

The SY205206DXC pin connections are shown in Figure 2. The protected line is connected to Pin1. Pin2 is connected to the GND, which should connect to a ground plane on the board. The connection traces should be as short as possible to minimize the parasitic inductance.

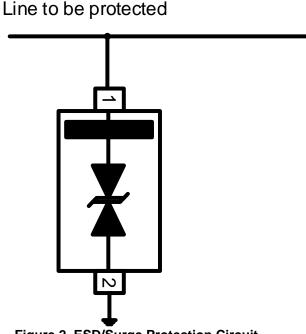


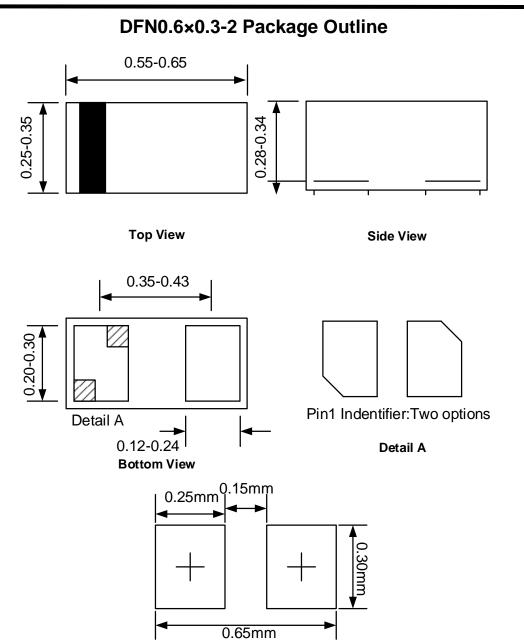
Figure 2. ESD/Surge Protection Circuit

### **PCB Layout Guidelines**

For optimum ESD protection and circuit performance, the following PCB layout guidelines are recommended:

- Place SY205206DXC as close to the connector port as possible.
- Use a large via to connect the SY205206DXC pin to the ground (GND).
- Avoid running signals near board edges.
- The SY205206DXC should be placed near the protected line.
- The distance between SY205206DXC ground pin and the GND reference path should be as short as possible.





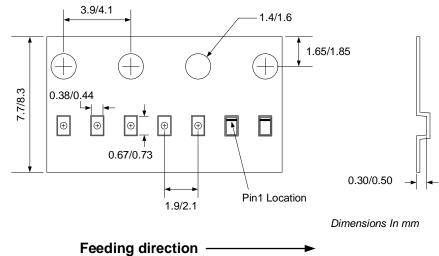
Recommended PCB Layout (Reference only)

Note: All dimensions are in millimeters and exclude mold flash and metal burr.

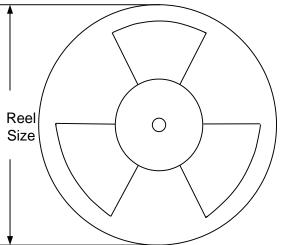


# **Tape and Reel Specification**

### DFN0.6×0.3-2 Taping Orientation



### **Carrier Tape & Reel Specification for Packages**



Package Types	Tape Width (mm)	Pocket Pitch(mm)	Reel Size (Inch)	Qty per Reel(pcs)
DFN0.6×0.3-2	8	2	7"	10000



# **Revision History**

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

<b>Revision Number</b>	Revision Date	Description	Pages changed
0.9	11/20/2020	Initial Release	
1.0	11/20/2021	Production Release	



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