SY20797C

High Efficiency Switched Capacitor Charger

General Description

The SY20797C is a high efficiency switched capacitor charger for high power fast charging applications. As a voltage divider or a current doubler with 50% switching duty cycle, the SY20797C integrates extremely low $R_{DS(ON)}$ MOSFETs and achieves up to 96.8% efficiency when V_{BAT} = 4V and I_{BAT} = 6A. It also provides a 9-channel, 12-bit ADC to monitor input and output voltage, current, and temperature for battery charging management by a host.

The SY20797C offers protection against multiple conditions, including external OVP-FET shutdown for input overvoltage protection, input overcurrent protection, output overvoltage and overcurrent protection, and temperature sensing for VBUS, battery, and die.

Applications

- Smartphones/Tablets
- Other Handhelds

Features

- External OVP Control and Regulation
- High Absolute Maximum Rating of 20V (V_{BUS})
- Battery Voltage Regulation (V_{BAT} REG)
- Battery Current Regulation (I_{BAT} REG)
- Integrated Input-Side NFET to Block Reverse Current
- Dual-Phase Switched Capacitor Converter
  - 8A Output Current Capability
  - Efficiency up to 96.8% when V_{BAT} = 4V, I_{BAT} = 6A
  - Programmable Frequency
- Spread spectrum for improved EMI
- 2:1 Charge-pump Mode and 1:1 Bypass Mode
- Fully Integrated Power MOSFETs with Extremely Low $R_{DS(ON)}$
- 50% Duty Cycle in 2:1 Charge-pump Mode
  - Voltage Divider: Input Voltage = Output Voltage × 2
  - Current Doubler: Output Current = Input Current × 2
- Soft-Start for Inrush Current Limit
- 9-Channel 12-Bit ADC
  - V_{AC}, V_{BUS}, V_{OUT}, V_{BAT}
  - I_{BUS}, I_{BAT}
  - T_{SBUS}, T_{SBAT}, T_{DIE}
- I^2C Interface

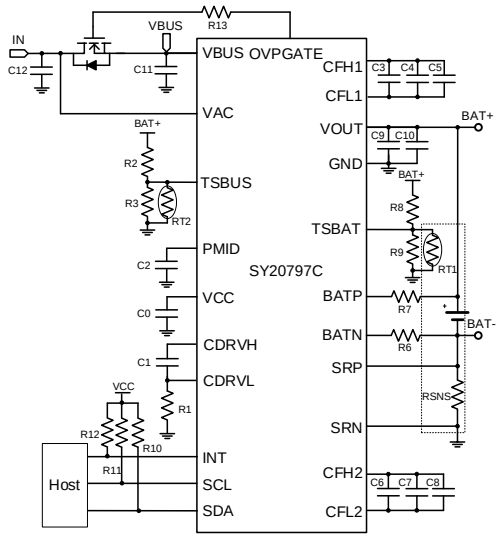


Figure 1. Typical Application Circuit

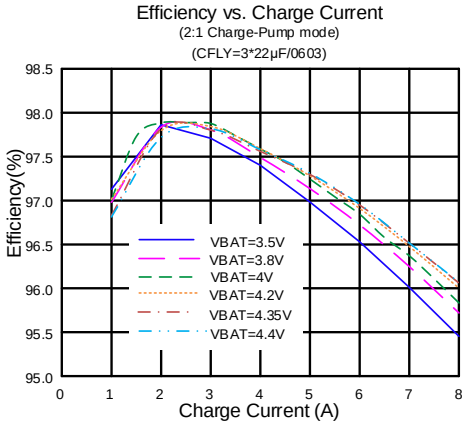


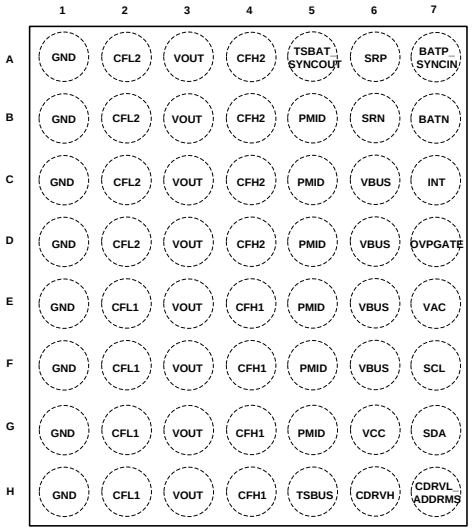
Figure 2. Efficiency vs. Output Current

Ordering Information

Ordering Part Number	Package Type	Top Mark
SY20797CVLS	CSP3.03×3.34-56 RoHS-Compliant and Halogen-Free	**EBN*xyz***

x = year code, y = week code, z = lot number code

Pinout (top view)



Pin Description

Pin No	Pin Name	Description
A1,B1,C1,D1 E1,F1,G1,H1	GND	Ground pin.
A2,B2,C2,D2	CFL2	Low side switching node of switched capacitor converter.
E2,F2,G2,H2	CFL1	Low side switching node of switched capacitor converter.
A3,B3,C3,D3 E3,F3,G3,H3	VOUT	Switched capacitor converter output pin. Connect two 10μF capacitors to GND.
A4,B4,C4,D4	CFH2	High side switching node of switched capacitor converter.
E4,F4,G4,H4	CFH1	High side switching node of switched capacitor converter.
A5	TSBAT_ SYNCOUT	Threshold detector input pin for battery temperature sensing. If the SY20797C is configured as a controller, this pin should be connected to BATP_SYNCIN of the peripheral device.
B5,C5,D5 E5,F5,G5	PMID	Input pin to switched capacitor converter. Connect a 10μF capacitor to GND.
H5	TSBUS	Threshold detector input pin for bus temperature sensing.
A6	SRP	Positive input for battery current sensing. Place a sense resistor between SRP and SRN.
B6	SRN	Negative input for battery current sensing. Place a sense resistor between SRP and SRN.
C6,D6,E6,F6	VBUS	Device power input pin.
G6	VCC	Internal LDO output pin. Connect a 4.7μF MLCC capacitor to ground.
H6	CDRVH	High side switching node of internal charge pump for gate drive. Place a 220nF capacitor between CDRVH and CDRVL_ADDRMS.
A7	BATP_SYNCIN	Positive input for battery voltage sensing. Connect a 100Ω resistor to the positive terminal of the battery pack. If the SY20797C is configured as a peripheral, this pin should be connected to TSBAT_SYNCOUT of the controller device.

B7	BATN	Negative input for battery voltage sensing. Place a 100Ω resistor to the negative terminal of the battery pack.
C7	INT	Open-drain, active-low interrupt output pin. Connect a 10kΩ resistor to pullup voltage. This pin will be pulled low for 256μs if a fault or alarm occurs.
D7	OVPGATE	External FET control pin. Connect to FET gate.
E7	VAC	Input voltage sense pin. Connect to external FET drain.
F7	SCL	I^2C Interface clock pin.
G7	SDA	I^2C Interface data pin.
H7	CDRL_ ADDRMS	Low side switching node of internal charge pump for gate drive. Place a 220nF capacitor between CDRVH and CDRVL_ADDRMS. Also connect a resistor to ground to assign the address and mode of device.

Block Diagram

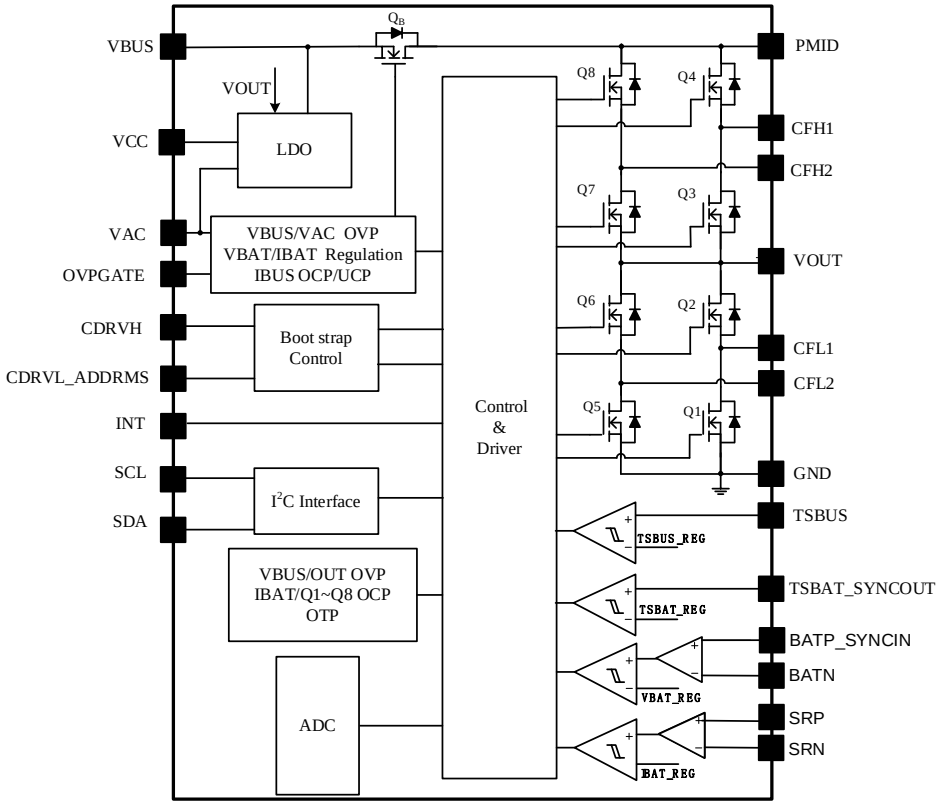


Figure 3. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
VAC	-0.3	36	V
VBUS, PMID, CDRVH	-0.3	20	
CFH1- CFL1, CFH2-CFL2, VOUT, TSBUS, TSBAT_SYNCOUT, BATP	-0.3	7	
OVPGATE-VBUS	-0.3	10.8	
VCC, SRP-SRN, INT, SCL, SDA, BATN, CDRVL_ADDRMS	-0.3	3.6	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering, 10s)		260	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	29	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	5.5	
P_D Power Dissipation T_A = 25°C	3.45	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
VAC	-0.3	12	V
VBUS, PMID, CDRVH	-0.3	12	
CFH1- CFL1, CFH2-CFL2, VOUT, TSBUS, TSBAT_SYNCOUT, BATP	-0.3	6	
OVPGATE-VBUS	-0.3	9.9	
VCC, SRP-SRN, INT, SCL, SDA, BATN, CDRVL_ADDRMS	-0.3	3.3	

Electrical Characteristics

(T_A = 25°C, unless otherwise specified.)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply	VAC Insert Threshold	V_{AC_INSERT}	VAC rising threshold to turn on external FET			3.2	V
		V_{AC_HYS}	Falling hysteresis	200	300	400	mV
	VAC UVLO	V_{AC_UVLO}	Rising threshold	2.5	2.7	2.9	V
		$V_{AC\_UVLOHYS}$	Falling hysteresis	100	200	300	mV
	VBUS UVLO	V_{BUS_UVLO}	Rising threshold	2.4	2.55	2.7	V
		V_{BUS_HYS}	Falling hysteresis	80	150	220	mV
	VOUT UVLO	V_{OUT_UVLO}	Rising threshold	2.4	2.55	2.7	V
		V_{OUT_HYS}	Falling hysteresis	80	150	220	mV
	LDO Output Voltage	V_{CC}	V_{BUS} = 8V, I_{VCC} = 0–30mA	3.37	3.42	3.47	V
	VBUS Quiescent Current	I_{Q_VBUS}	ADC disable, charge disable, OVPGATE not used	0.75	1.1	1.4	mA
			ADC disable, charge disable, OVPGATE used		1.5		mA
			ADC enable, charge disable, OVPGATE not used		1.2	1.5	mA
	VBAT Quiescent Current	I_{Q_VBAT}	ADC disable, charge disable, VBUS not present		10	20	μA
			ADC enable, charge disable		650	900	μA
External OVP Control	External FET Driver Voltage	V_{DRV}	OVPGATE-VBUS	8.4	9	9.5	V
	Turn-On FET Deglitch Time	V_{AC_FETDEG}	Deglitch time between triggering V_{AC_INSERT} and turning on FET	18	20	22	ms
	VAC Present Deglitch Time	V_{AC_INTDEG}	Deglitch time between triggering V_{AC_INSERT} and sending INT	0.8	1	1.2	ms
	FET Turn-Off Time	T_{FETOFF}			100		ns
	FET Turn-Off Reaction Time	$T_{REACTION}$	Delay time between VAC OVP and FET shutdown		100		ns
	VBAT Regulation Accuracy	V_{BAT_REGACC}	The threshold below VBAT_OVP where the device starts regulation, It is set by bit[5:4] of register 0x2C, with the range 50mV to 200mV and the step 50mV.	-20		20	mV
	IBAT Regulation Accuracy	I_{BAT_REGACC}	The threshold below IBAT_OCP where the device starts regulation, It is set by bits[7:6] of register 0x2C, with the range 200mA to 500mA and the step 100mA.	-200		200	mA
	Regulation Timeout	$T_{TIMEOUT}$	Maximum regulation time. If the time expires, the device will not charge.	585	650	715	ms
MOSFET	On-Resistance	$R_{DS(ON)}$	Q_B		10		mΩ
			Q1,Q2,Q3,Q5,Q6,Q7		7		mΩ

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
			Q4,Q8		15		mΩ
Frequency and Duty	Frequency	f_{SW}	Register0x0B, bit[6:4] = '101'	675	750	825	kHz
			Register0x0B, bit[6:4] = '100'	450	500	550	kHz
			Register0x0B, bit[6:4] = '010'	270	300	330	kHz
	Duty-Cycle of Switch Node Output	D_{SW}			50		%
Internal Timer	Device Startup Time	$t_{VCCSART}$	Device startup time from internal VDD > UVLO to I^2C communication			64	ms
	Soft-Start Time	$t_{SOFTSART}$	Soft-start time from CHG_EN = 1 to converter switching			150	ms
	IBUS UCP Timeout Accuracy	$t_{IBUS\_UCP\_TIMEOUT\_ACC}$	Register 0x2B bit[7:5], range: 12.5ms–100s	-10		10	%
	Watchdog Timeout	$t_{TIMEOUT}$	Register 0x0B bit[1:0] = '00'	0.45	0.5	0.55	s
			Register 0x0B bit[1:0] = '01'	0.9	1	1.1	s
			Register 0x0B bit[1:0] = '10'	4.5	5	5.5	s
			Register 0x0B bit[1:0] = '11'	27	30	33	s
	INT Duration Time	t_{INT}	INT pulled low time when an event occurs		256		μs
Protection Threshold and Accuracy	VAC OVP Accuracy	$V_{AC\_OVP\_ACC}$	Register 0x05 bit[2:0], range: 11V–17V, step:1V	-2		2	%
	VAC OVP Hysteresis	$V_{AC\_OVP\_HYS}$			500		mV
	VBUS OVP Accuracy	$V_{BUS\_OVP\_ACC}$	Register 0x06 bit[6:0], range: 6V–12.35V, step:50mV V_{BUS} = 10V	-1		1	%
	VOUT OVP Accuracy	$V_{OUT\_OVP\_ACC}$		4.8	4.9	5	V
	VBAT OVP Accuracy	$V_{BAT\_OVP\_ACC}$	Register 0x00 bit[5:0], range: 3.5V–5.075V, step: 25mV V_{BAT_OVP} = 4.2V to 4.65V	-1		1	%
	VDR OVP Accuracy	$V_{DR\_OVP\_ACC}$	Register 0x05 bit[4] = '0', default	245	300	355	mV
			Register 0x05 bit[4] = '1'	345	400	455	mV
	IBUS OCP Accuracy	$I_{BUS\_OCP\_ACC}$	Register 0x08 bit[3:0], range: 1A–4.75A, step: 250mA I_{BUS_OCP} = 2A	-10		10	%
			I_{BUS_OCP} = 4A	-5		5	%
	IBUS UCP_RISE Accuracy	$I_{BUS\_UCP\_RISE\_ACC}$	Register 0x2B bit[2] = '0'	200	300	400	mA
			Register 0x2B bit[2] = '1'	400	500	600	mA
	IBUS UCP_FALL Accuracy	$I_{BUS\_UCP\_FALL\_ACC}$	Register 0x2B bit[2] = '0'	10	150	290	mA
			Register 0x2B bit[2] = '1'	110	250	390	mA
	IBAT OCP Accuracy	$I_{BAT\_OCP\_ACC}$	R_{SENSE} = 0.002Ω, Register 0x02 bit[6:0], range: 2A–10A, step: 100mA I_{BAT_OCP} = 2A	-5		5	%

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
			I_{BAT_OCP} = 6A	-2		2	%
	TSBAT and TSBUS OTP Accuracy	$T_{S\_OTP\_ACC}$	Falling edge, Register 0x28/0x29 bit[7:0] range: 0–49.8%, step: 0.19531%	-1		1	%
	TDIE_OTP Accuracy	$T_{DIE\_OTP\_ACC}$	Rising threshold		145		˚C
	TDIE_OTP Hysteresis	$T_{DIE\_OTP\_HYS}$	OTP recovery, falling hysteresis		30		˚C
	VBUS_HIGH_ERR Accuracy	$V_{BUS\_HIGH\_ERR\_ACC}$	Detect VBUS/VOUT ratio, rising edge	2.328	2.4	2.472	V/V
	VBUS_LOW_ERR Accuracy	$V_{BUS\_LOW\_ERR\_ACC}$	Detect VBUS/VOUT ratio, falling edge	2	2.04	2.08	V/V
	Converter OCP Threshold	I_{CON_OCP}			16		A
Alarm Threshold and Accuracy	VBUS_OVP_ALM Accuracy	$V_{BUS\_OVP\_ALM\_ACC}$	Register 0x07 bit[6:0], range:6V–12.35V, step: 50mV VBUS_OVP_ALM = 6V to 9V	-0.5		0.5	%
	VBUS_OVP_ALM Hysteresis	$V_{BUS\_OVP\_ALM\_HYS}$	Falling edge		50		mV
	VBAT_OVP_ALM Accuracy	$V_{BAT\_OVP\_ALM\_ACC}$	Register 0x01 bit[5:0], range:3.5V–5.075V, step: 25mV VBAT_OVP = 3.5V to 4.4V	-0.5		0.5	%
	VBAT_OVP_ALM Hysteresis	$V_{BAT\_OVP\_ALM\_HYS}$	Falling edge		50		mV
	IBUS_OCP_ALM Accuracy	$I_{BUS\_OCP\_ACC}$	Register 0x08 bit[3:0], range:1A–4.75A, step: 250mA IBUS_OCP = 2A	-10		10	%
			IBUS_OCP = 4A	-5		5	%
	IBUS_OCP_ALM Hysteresis	$I_{BUS\_OCP\_ALM\_HYS}$	Falling edge		50		mA
	IBAT_OCP_ALM Accuracy	$I_{BAT\_OCP\_ALM\_ACC}$	R_{SENSE} = 0.002Ω, Register 0x02 bit[6:0], range: 2A–10A, step: 100mA IBAT_OCP = 2A	-5		5	%
			IBAT_OCP = 6A	-2		2	%
	IBAT_OCP_ALM Hysteresis	$I_{BAT\_OCP\_ALM\_HYS}$	Falling edge		100		mA
	IBAT_UCP_ALM Accuracy	$I_{BAT\_UCP\_ALM\_ACC}$	R_{SENSE} = 0.002Ω, Register 0x04 bit[6:0], range: 0–6.35A, step: 50mA IBAT_UCP_ALM = 2A	-5		5	%
	IBAT_UCP_ALM Hysteresis	$I_{BAT\_UCP\_ALM\_HYS}$	Falling edge		100		mA
	TSBAT_TSBUS_ALM Accuracy	$T_{S\_OTP\_ALM\_ACC}$	Falling edge, range:0–50%,Step:0.19531% TSBAT_TSBUS_ALM Threshold = TSBAT_OTP + 4% or TSBUS_OTP + 4%	-1		1	%
	TSBAT_TSBUS_ALM Hysteresis	$T_{S\_OTP\_ALM\_ALM\_HYS}$	Rising edge		5		%
	TDIE_OTP_ALM Accuracy	$T_{DIE\_OTP\_ALM\_ACC}$	Register 0x2A bit[7:0], range: 25˚C –152.5˚C, step: 0.5˚C	-4		4	˚C
	TDIE_OTP_ALM Hysteresis	$T_{DIE\_OTP\_ALM\_HYS}$	Falling edge		10		˚C

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
ADC	ADC Sample Rate	f_{SAMPLE_RATE}			10		kHz
	ADC Data Rate t_{DATA}	t_{DATA_ADC}	11bit, 8 averages report data for each channel		800		μs
	VBUS ADC Accuracy	$V_{BUS\_ADC\_ACC}$	Range:0V–14V, VBUS = 8V	-0.75		0.75	%
	IBUS ADC Accuracy	$I_{BUS\_ADC\_ACC}$	Range:0–5A, IBUS = 4A	-5		5	%
	VAC ADC Accuracy	$V_{AC\_ADC\_ACC}$	Range:0V–14V, VAC = 8V	-0.75		0.75	%
	VOUT ADC Accuracy	$V_{OUT\_ADC\_ACC}$	Range:0V–5V, VOUT = 4V	-0.75		0.75	%
	VBAT ADC Accuracy	$V_{BAT\_ADC\_ACC}$	Range:0V–5V, VBAT = 3.5V to 4.5V	-0.5		0.5	%
	IBAT ADC Accuracy	$I_{BAT\_ADC\_ACC}$	Range:0–10A, IBAT = 6A, R_{SENSE} = 0.002Ω	-2.5		2.5	%
	TDIE ADC Accuracy	$T_{DIE\_ADC\_ACC}$	Range:0–150 ˚C, step: 0.5 ˚C	-4		4	˚C
	TSBUS ADC Accuracy	$T_{SBUS\_ADC\_ACC}$	Range:0–50% TSBUS pin voltage = 0.2V to 2V	-1		1	%
	TSBAT ADC Accuracy	$T_{SBAT\_ADC\_ACC}$	Range:0–50% TSBAT pin voltage = 0.2V to 2V	-1		1	%
I^2C Interface	Logic Input High Voltage		SCL, SDA vs GND	1.4			V
	Logic Input Low Voltage		SCL, SDA vs GND			0.5	V
	Logic Output Low Voltage	V_{OL}	SDA vs GND			0.4	V
	I^2C Input Capacitance		SCL, SDA		5		pF
	SCL Operating Frequency	$f_{(SCL)}$				400	kHz
	Bus Free Time Between Stop and Start Conditions	$t_{(BUF)}$		1.3			μs
	Hold Time after Repeated Start Condition. First Clock is Generated after this Period.	$t_{(HDSTA)}$		0.6			μs
	Repeated Start Condition Setup Time	$t_{(SUSTA)}$		0.6			μs
	Stop Condition Setup Time	$t_{(SUSTO)}$		0.6			μs
	Data Hold Time	$t_{(HDDAT)}$				0.9	μs
	Data Setup Time	$t_{(SUDAT)}$		100			ns
	SCL Clock Low Period	$t_{(LOW)}$		1.3			μs
	SCL Clock High Period	$t_{(HIGH)}$		0.6			μs
	Clock/Data Fall Time	t_F				300	ns
	Clock/Data Rise Time	t_R				300	ns

Note 1: Stresses beyond the above “Absolute Maximum Ratings” may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

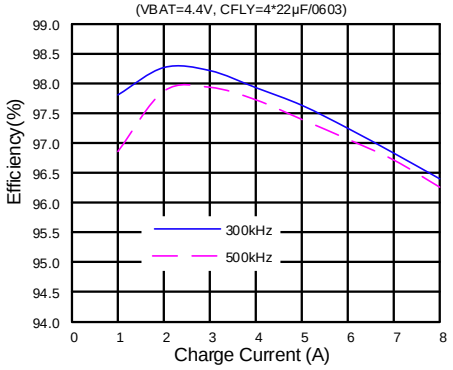
Note 2: Package thermal resistance is measured in the natural convection at TA = 25˚C on an 8.5cm×7.7cm size four-layer Silergy Evaluation Board.

Note 3: The device is not guaranteed to function outside its operating conditions.

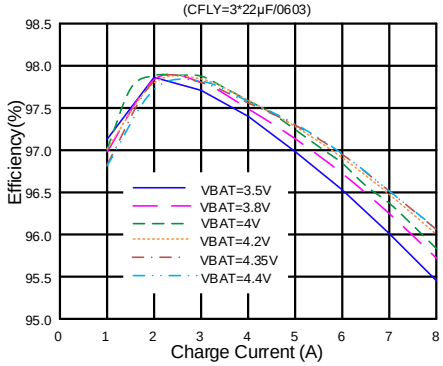
Typical Performance Characteristics

(V_{IN} = 13.5V, L = 4.7μH(CLF10040T-4R7M), R_{FSW} = 62kΩ, R_{CTRL} = 10kΩ, T_A = 25°C, otherwise specified.)

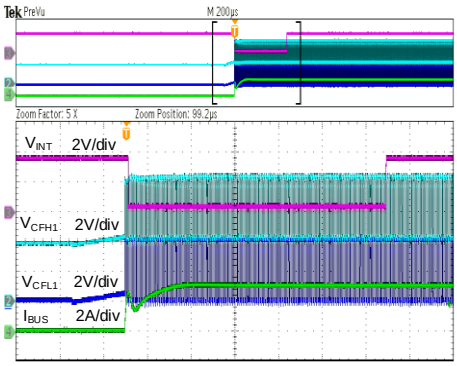
Efficiency vs. Charge Current
(2:1 Charge-Pump mode)
(VBAT=4.4V, CFLY=4*22μF/0603)



Efficiency vs. Charge Current
(2:1 Charge-Pump mode)
(CFLY=3*22μF/0603)

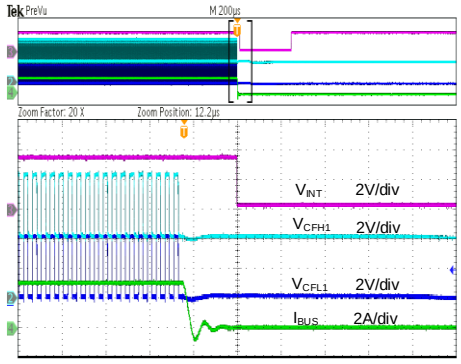


CHG_EN Enable Control Test
(2:1 Charge-Pump mode startup)



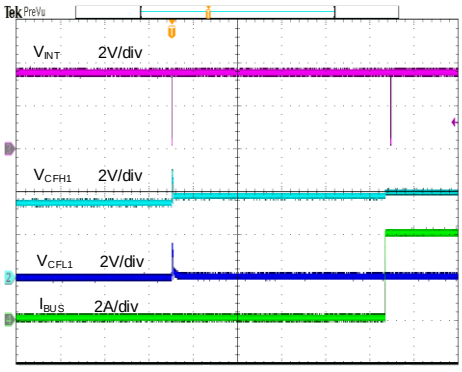
Time (40μs/div)

CHG_EN Enable Control Test
(2:1 Charge-Pump mode shutdown)



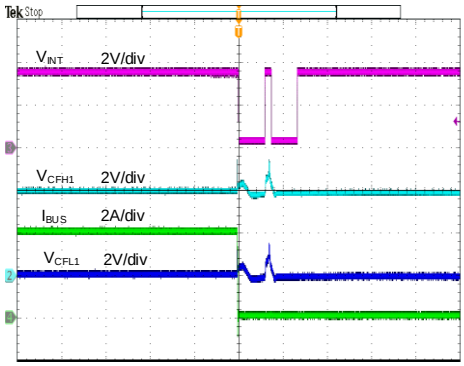
Time (10μs/div)

1:1 Bypass Mode Enable Control Test
(Startup)



Time (20ms/div)

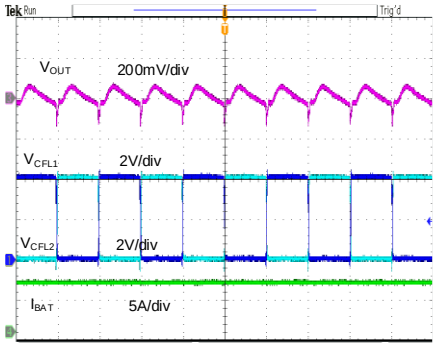
1:1 Bypass Mode Enable Control Test
(Shutdown)



Time (400μs/div)

Output Voltage Ripple

(2:1 Charge-Pump mode, V_{AC}=8.33V, V_{BAT}=4V, IBAT=6A)



Time (1μs/div)

Detailed Description

Overview

The SY20797C is a high efficiency switched capacitor converter for high power fast charging applications. As a voltage divider or a current doubler with 50% switching duty cycle, it integrates extremely low $R_{DS(ON)}$ MOSFETs to achieve 97% efficiency and up to 8A maximum charging current. It also provides a 9-channel, 12-bit ADC to monitor input and output voltage, current, and temperature for battery charging management by a host.

The SY20797C offers protection against multiple conditions, including external OVP-FET shutdown for input overvoltage protection, input overcurrent protection, output overvoltage and overcurrent protection, and temperature sensing for VBUS, battery, and die.

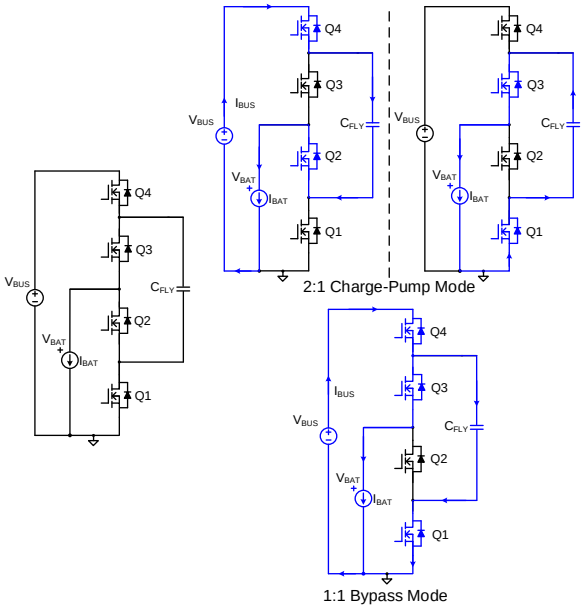


Figure 4. Single-Phase Switched Capacitor Converter

OVP-FET Control

The SY20797C's VAC and OVPGATE pins are used to monitor the adaptor voltage and control the external OVP-FET. As shown in Figure 5, the OVP-FET is driven by the OVPGATE pin if VAC pin voltage is higher than the V_{AC_INSERT} threshold. To protect the low voltage device, OVP-FET will be turned off in less than 100ns if VAC pin voltage is higher than the V_{AC_OVP} threshold. VAC overvoltage protection logic includes automatic recovery.

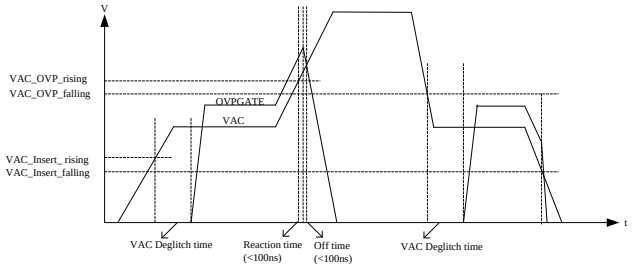


Figure 5. OVP-FET Control

Soft-Start

The SY20797C uses a pre-charge stage to charge the flying capacitor before switching. When the CHG_EN bit is enabled, a 50Ω resistor is connected to CFL1/CFL2 to limit the pre-charge current. At the end of the pre-charge time, the CFL1/CFL2 voltage is detected. If CFL1/CFL2 is pulled lower than 100mV, the pre-charge stage is considered complete. Otherwise, the pre-charge stage is considered as failing and SY20797C will report a 'CFLY_DIG' fault, which means a CFLY short during converter soft-start.

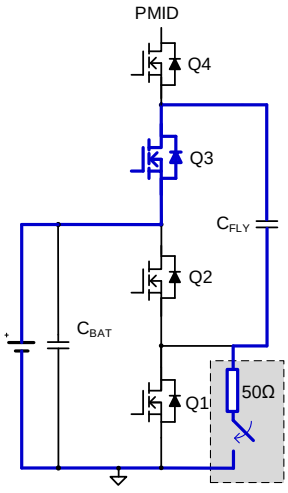


Figure 6. Pre-Charge Circuit

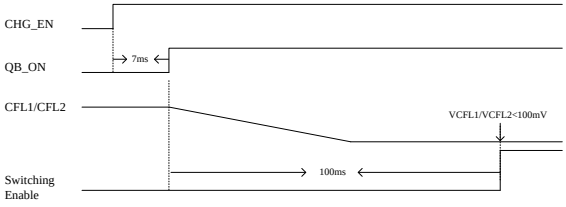


Figure 7. Soft-Start

I²C Address and Mode Selection

The CDRVL_ADDRMS pin is used to set the default I²C address and mode as shown in Table 1. Two devices can be paralleled for higher charging power if they are configured as host and peripheral, respectively. For synchronization, the host's TSBAT_SYNCOUT pin outputs a PWM signal to the peripheral's BATP_SYNCIN pin to achieve phase interleaving.

Table 1: I²C Address and Mode Selection

CDRVL_ADDRMS Pin Resistor To GND	I²C Address	Mode	V_{AC_OVP} Default Value
18kΩ	0x65	Host	6.5V
39kΩ	0x66	Peripheral	Disabled
75kΩ	0x65	Standalone	11V
>150kΩ	0x66	Standalone	6.5V

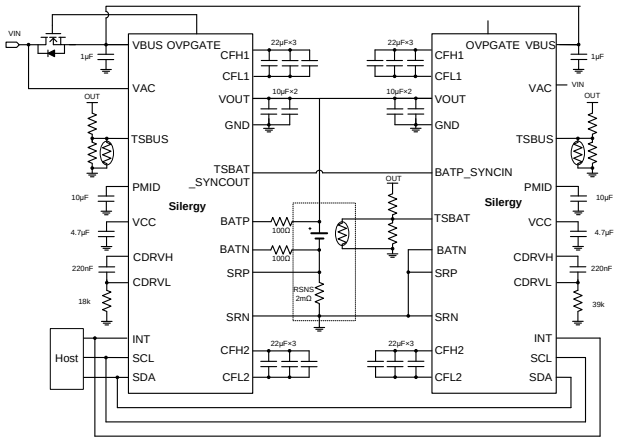


Figure 8. I²C Address and Mode Selection

Protection Modes

Overtemperature Protection

The SY20797C provides overtemperature protection for the junction, bus connector, and battery pack. If junction temperature is higher than 145°C, the SY20797C will stop charging and reset the CHG_EN bit to '0'. For bus connector and battery pack temperature sensing, a resistor divider circuit is added as shown in Figure 9. RT is a negative coefficient thermistor and the protection threshold is calculated as follows:

$$\text{TSBUS/TSBAT Threshold}(\%) = \frac{R_2//R_T}{R_1 + R_2//R_T}$$

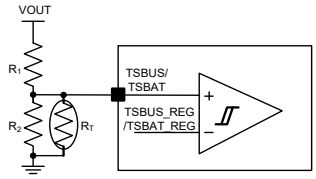


Figure 9. Temperature Sensing

Note that TSBUS and TSBAT thresholds are percentages of VOUT that are programmable using registers 0x28 and 0x29, and VOUT ADC should be enabled if either TSBUS or TSBAT is used. As with junction temperature protection, the SY20797C will stop charging and reset the CHG_EN bit to '0' if the TSBAT or TSBUS threshold is triggered.

Overvoltage Protection

The SY20797C provides overvoltage protection for VBUS, VOUT, and battery (battery voltage is sensed by BATP and BATN pins). If any of these voltage thresholds are triggered, the SY20797C will stop charging and reset the CHG_EN bit to '0'. In high charging current applications, it is recommended that BATP and BATN pins connect a 100Ω resistor to the battery pack positive and negative terminals.

Overvoltage protection and alarm thresholds VBUS_OVP and VBUS_OVP_ALM are set by registers 0x06 and 0x07, respectively. In 2:1 charge-pump mode, the thresholds are directly set by these registers, while in 1:1 bypass mode the thresholds are divided by two.

Overcurrent Protection

The SY20797C provides overcurrent protection for BUS and battery. Input current IBUS is sensed by blocking FET Q_B, and battery charging current detected by SRP and SRN pins is sensed by a 5mΩ/2mΩ/1mΩ resistor. If the IBUS OCP or IBAT OCP threshold is triggered, the SY20797C will stop charging and reset the CHG_EN bit to '0'.

Input Undercurrent Protection

The SY20797C provides undercurrent protection (I_{BUS_UCP}) to prevent reverse current from battery to VBUS. When CHG_EN is enabled, a counting timer with duration set by IBUS_UCP_TIMEOUT (register 0x2B) is activated. A timeout occurs and IBUS_UCP_TIMEOUT_FLAG (register 0x0A) is set if the bus current is still below the IBUS_UCP rising threshold when the timer expires. The IBUS_UCP falling threshold will be enabled and the counting timer will be disabled once IBUS is higher than the IBUS_UCP rising threshold. If IBUS falls below the IBUS_UCP falling threshold, IBUS_UCP_FALL will be triggered and the SY20797C will stop charging and reset the CHG_EN bit to '0'. It should be noted that the IBUS_UCP rising and falling thresholds are simultaneously set by IBUS_UCP_RISE_THRESH (bit[2] of register 0x2B).

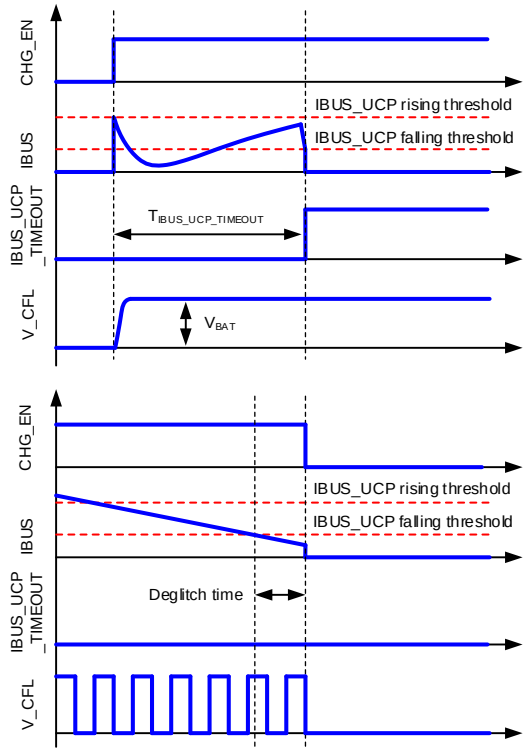


Figure 10. Input Undercurrent Protection

VBUS Range Protection

Before the device begins charging, VBUS should be approximately 2 × VOUT in 2:1 charge-pump mode and approximately VOUT in 1:1 bypass mode. The SY20797C has two fixed thresholds to monitor the ratio of VBUS and VOUT: $V_{BUS\_HIGH\_ERR}$ and $V_{BUS\_LOW\_ERR}$. The SY20797C will begin soft-start and switching only when $V_{BUS\_LOW\_ERR} < V_{BUS}/V_{OUT} < V_{BUS\_HIGH\_ERR}$ in 2:1 charge-pump mode and when $V_{BUS\_LOW\_ERR}/2 < V_{BUS}/V_{OUT} < V_{BUS\_HIGH\_ERR}/2$ in 1:1 bypass mode. After charging is enabled, the VBUS range protection will be disabled.

VBAT and IBAT Regulation

The SY20797C features an integrated regulation circuit to protect the battery and limit instantenous VBAT and IBAT

transients. For VBAT regulation, the monitored differential voltage between BATP and BATN pin, i.e., $V_{BATP-BATN}$, is compared to VBAT_REG threshold, and the drive voltage of OVP FET will be controlled to limit VBUS if $V_{BATP-BATN}$ is greater than VBAT_REG threshold. As a result VBAT transients will be effectively reduced. For IBAT regulation, the monitored differential voltage between SRN and SRP pin is first converted into a current value $I_{SRN-SRP}$, and then compared to the IBAT_REG threshold. If $I_{SRN-SRP}$ exceeds IBAT_REG, the drive voltage of OVP FET will be controlled to reduce VBUS, which in turn reduces the output voltage to limit instant IBAT transients. If regulation is triggered and persists for $t_{REG\_TIMEOUT}$, the SY20797C will stop charging and reset the CHG_EN bit to '0'.

Dropout Voltage Protection (VDR_OVP)

In regulation status, the external OVP-FET operates in linear mode and might generate considerable power loss. The VDR_OVP function monitors the voltage drop between the VAC and VBUS pins to prevent the OVP-FET and system from overheating. If the VDR_OVP threshold is triggered, the SY20797C will stop charging and reset the CHG_EN bit to '0'.

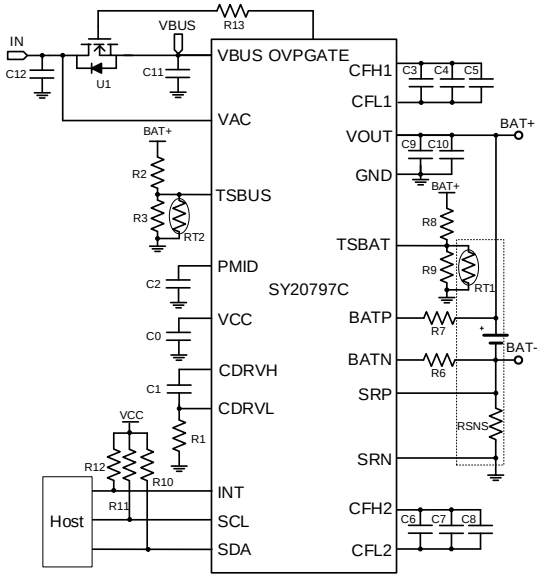
Watchdog Timer

The SY20797C provides a watchdog timer to terminate charging if the device does not receive read or write commands before the watchdog timer expires. The CHG_EN bit and ADC_EN bit will be reset to '0' if this occurs.

INT

INT is an open-drain, active-low interrupt output pin. It should be pulled up by an external voltage source. When the SY20797C triggers an event, the INT pin will be pulled low for 256μs to notify the host, The corresponding STAT bit and FLAG bit will also be set to '1'. The STAT bit will be reset to '0' if the event is cleared. Read action or power reset can clear the FLAG bit. The MASK bit prevents the INT signal from being sent to the host, but will not stop the STAT and FLAG from updating.

Applications Schematic



BOM List

Designator	Description	Part Number	Manufacturer
U1	PowerPAK SO-8	SiR472DP	
C0	4.7μF/25V, 0603	GRM188R61E475KE11D	muRata
C3, C4, C5, C6, C7, C8	22μF/10V, 0603	GRM188R61A226ME15D	muRata
C11, C12	1μF/25V, 0805	GRM219R71E105KA88D	muRata
C2, C9, C10	10μF/25V, 0805	GRM21BR61E106KA73L	muRata
C1	220nF/50V, 0603		
R6, R7	100Ω, 0603		
R13	10Ω, 0603		
RSNS	2mΩ, 1206		
R1	75kΩ, 0603		
R10, R11, R12	10kΩ, 0603		
R2, R3, R8, R9	100kΩ, 0603		

Layout Design

Follow these PCB layout considerations for optimal performance and to prevent noise and electromagnetic interference:

- To minimize noise, place a typical X5R or better grade ceramic capacitor as close as possible to the VAC, BUS, PMID, and GND pins. Minimize the loop areas formed by C_{VAC} and the VAC/GND pins, C_{BUS} and the BUS/GND pins, and C_{PMID} and the PMID/GND pins. A 10μF low ESR ceramic capacitor is recommended.
- To improve charge pump efficiency, use X5R or better grade low ESR ceramic capacitors for the flying capacitors. Refer to the efficiency curve in the typical performance characteristics to select capacitor value. The flying capacitors should be placed as close as possible to the SY20797C on the same layer.
- The output capacitor is selected to handle the output ripple noise requirements. Use a low ESR ceramic capacitor with voltage rating higher than the maximum output voltage. The output capacitance should be at least 10μF × 2 ceramic capacitors.

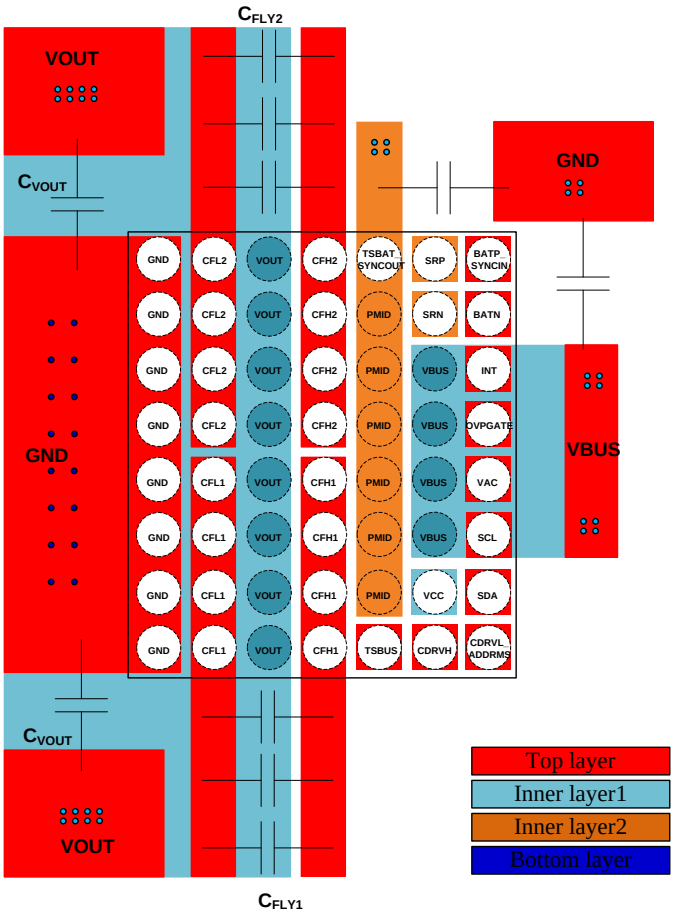


Figure 11. Suggested PCB Layout

Register Map

I²C Peripheral Address: 0x66 (standalone1), 0x65 (standalone2), 0x66 (peripheral), 0x65 (host).

Register	ACRONYM	Default Value			
		Standlone1	Standlone2	Peripheral	Host
0x00	VBAT_OVP and Charge Mode Control	0x22	0x22	0xA2	0x22
0x01	VBAT_OVP_ALM	0x1C	0x1C	0x9C	0x1C
0x02	IBAT_OCP	0x3D	0x3D	0xBD	0x3D
0x03	IBAT_OCP_ALM	0x3C	0x3C	0xBC	0x3C
0x04	IBAT_UCP	0x28	0x28	0xA8	0x28
0x05	AC_PROTECTION	0x07	0x00	0x00	0x07
0x06	VBUS_OVP	0x3A	0x3A	0x3A	0x3A
0x07	VBUS_OVP_ALM	0x38	0x38	0xB8	0x38
0x08	IBUS_OCP_UCP	0x0D	0x0D	0x0D	0x0D
0x09	IBUS_OCP_ALM	0x50	0x50	0x50	0x50
0x0A	CONVERTER_STATE	0x00	0x00	0x00	0x00
0x0B	CHG_CTL	0x40	0x40	0x40	0x40
0x0C	CHG_CTL1	0x00	0x00	0x20	0x46
0x0D	INT_STAT	0x00	0x00	0x00	0x00
0x0E	INT_FLAG	0x00	0x00	0x00	0x00
0x0F	INT_MASK	0x00	0x00	0x00	0x00
0x10	FLT_STAT	0x00	0x00	0x00	0x00
0x11	FLT _FLAG	0x00	0x00	0x00	0x00
0x12	FLT _MASK	0x00	0x00	0x00	0x00
0x13	DEVICE_INFO	0x0E	0x0E	0x0E	0x0E
0x14	ADC_CTL	0x00	0x00	0x00	0x00
0x15	AD_ EN	0x00	0x00	0xF8	0x06
0x16	IBUS_ADC1	0x00	0x00	0x00	0x00
0x17	IBUS_ADC0	0x00	0x00	0x00	0x00
0x18	VBUS_ADC1	0x00	0x00	0x00	0x00
0x19	VBUS_ADC0	0x00	0x00	0x00	0x00
0x1A	VAC_ADC1	0x00	0x00	0x00	0x00

0x1B	VAC_ADC0	0x00	0x00	0x00	0x00
0x1C	VOUT_ADC1	0x00	0x00	0x00	0x00
0x1D	VOUT_ADC0	0x00	0x00	0x00	0x00
0x1E	VBAT_ADC1	0x00	0x00	0x00	0x00
0x1F	VBAT_ADC0	0x00	0x00	0x00	0x00
0x20	IBAT_ADC1	0x00	0x00	0x00	0x00
0x21	IBAT_ADC0	0x00	0x00	0x00	0x00
0x22	TSBUS_ADC1	0x00	0x00	0x00	0x00
0x23	TSBUS_ADC0	0x00	0x00	0x00	0x00
0x24	TSBAT_ADC1	0x00	0x00	0x00	0x00
0x25	TSBAT_ADC0	0x00	0x00	0x00	0x00
0x26	TDIE_ADC1	0x00	0x00	0x00	0x00
0x27	TSBAT_ADC0	0x00	0x00	0x00	0x00
0x28	TSBUS_OTP	0x15	0x15	0x15	0x15
0x29	TSBAT_OTP	0x15	0x15	0x15	0x15
0x2A	TDIE_ALM	0xC8	0xC8	0xC8	0xC8
0x2B	REG_CTL	0xE0	0xE0	0xE0	0xE0
0x2C	REG_THRESHOLD	0x00	0x00	0x00	0x00
0x2D	REG_FLAG	0x00	0x00	0x00	0x00
0x2E	REG_STAT_FLAG	0x00	0x00	0x00	0x00

Register reset map

Reset by Watchdog of Register 0x0B bit[2:0]			
Register	Bit and Name	Register	Bit and Name
0x0C	Bit[7]: CHG_EN	0x14	Bit[7]: ADC_EN
Not reset by REG_RST of Register 0x0B bit[7]			
Register	Bit and Name	Register	Bit and Name
0x05	Bit[4]: VDR_OVP_THRESHOLD_SET	0x11	All bits of FLT_FLAG register
0x0A	Bit[3]: IBUS_UCP_TIMEOUT_FLAG	0x2B	Bit[7:5]: IBUS_UCP_TIMEOUT
	Bit[2]: SWITCHING_STAT		Bit[4]: REG_EN
	Bit[1]: CON_OCP_FLAG		Bit[3]: VOUT_OVP_DIS
0x0B	Bit[6:4]: FSW_SET		Bit[1]: IBAT_RSEN
0x0D	All bits of INT_STAT register	0x2C	All bits of REG_THRESHOLD register
0x0E	All bits of INT_FLAG register	0x2D	All bits of REG_FLAG register
0x10	All bits of FLT_STAT register		

VBAT_OVP and Charge Mode Control Register (Register 0x00)

Bit	R/W	Default	Description	
[7]	R/W	0	VBAT_OVP_DIS	Battery OVP enable bit. 0: Enable (default) 1: Disable Read only and default = 1 for peripheral
[6]	R/W	0	Charge mode control	Charge mode selecting bit, CH_EN must be set to '1' to start charging. 0: Forward 2:1 charge-pump mode 1: Forward 1:1 bypass mode
[5:0]	R/W	10_0010	VBAT_OVP	Battery OVP threshold VBAT_OVP = 3.5V + bit[5:0] × LSB (default: 4.35V) LSB = 25mV

VBAT_OVP_ALM Register (Register 0x01)

Bit	R/W	Default	Description	
[7]	R/W	0	VBAT_OVP_ALM_DIS	Battery OVP alarm enable bit. 0: Enable (default) 1: Disable Read only and default = 1 for peripheral
[6]	R	0	Reserved	
[5:0]	R/W	01_1100	VBAT_OVP_ALM threshold	Battery OVP alarm threshold. VBAT_OVP_ALM = 3.5V + bit[5:0] × LSB (default: 4.2V) LSB = 25mV

IBAT_OCP Register (Register 0x02)

Bit	R/W	Default	Description	
[7]	R/W	0	IBAT_OCP_DIS	Battery OCP enable bit. 0: Enable (default) 1: Disable Read only and default = 1 for peripheral
[6:0]	R/W	011_1101	IBAT_OCP	Battery OCP threshold. IBAT_OCP = 2A + bit[6:0] × LSB (default: 8.1A) LSB = 100mA Any setting over 10A is set to 10A.

IBAT_OCP_ALM Register (Register 0x03)

Bit	R/W	Default	Description	
[7]	R/W	0	IBAT_OCP_ALM_IS	Battery OCP alarm enable bit. 0: Enable (default) 1: Disable Read only and default = 1 for peripheral

[6:0]	R/W	011_1100	IBAT_OCP _ALM	Battery OCP alarm threshold. IBAT_OCP_ALM = 2A + bit[6:0] × LSB (default: 8A) LSB = 100mA

IBAT_UCP_ALM Register (Register 0x04)

Bit	R/W	Default	Description	
[7]	R/W	0	IBAT_UCP_ALM_DIS	Battery UCP alarm enable bit. 0: Enable (default) 1: Disable Read only and default = 1 for peripheral
[6:0]	R/W	010_1000	IBAT_UCP _ALM	Battery UCP alarm threshold. IBAT_UCP_ALM = bit[6:0] × LSB (default: 2A) LSB = 50mA

AC_PROTECTION Register (Register 0x05)

Bit	R/W	Default	Description	
[7]	R	0	VAC_OVP_STAT	Set 1 when a VAC_OVP event occurs. Persists until condition is no longer valid. 0: No VAC_OVP fault 1: VAC_OVP fault is occurring
[6]	R	0	VAC_OVP_FLAG	VAC_OVP event. Cleared upon read. 0: No VAC_OVP fault 1: VAC_OVP fault has occurred
[5]	R/W	0	VAC_OVP_MASK	Mask VAC_OVP event to send INT. 0: Not masked (default) 1: Masked
[4]	R/W	0	VDR_OVP_THRESHOLD_SET	Voltage difference between VAC and VBUS that will cause the device to stop switching. 0: 300mV (default) 1: 400mV
[3]	R/W	0	VDR_OVP_DEGLITCH_SET	Deglitch time after the device reaches the VDR_OVP threshold before the device stops switching. 0: 8μs (default) 1: 5ms
[2:0]	R/W	111	VAC_OVP	000-110 setting is determined by VAC_OVP = 11V + bit[3:0] × 1V. Writing 1 to all of these bits sets the VAC_OVP to 6.5V. Default for peripheral = 000 Default for standalone2 = 000

VBUS_OVP Register (Register 0x06)

Bit	R/W	Default	Description	
[7]	R/W	0	VBUS_PD_EN	VBUS pulldown resistor enable bit. 0: Pulldown disable (default) 1: Pulldown enable (1kΩ resistor)
[6:0]	R/W	011_1010	VBUS_OVP	VBUS OVP threshold. 2:1 charge-pump mode: VBUS_OVP = 6V + bit[6:0] ×50mV, Default = 8.9V 1:1 bypass mode: VBUS_OVP = 3V + bit[6:0] ×25mV, Default = 4.45V

VBUS_OVP_ALM Register (Register 0x07)

Bit	R/W	Default	Description	
[7]	R/W	0	VBUS_OVP_ALM_DIS	VBUS OVP alarm disable bit. 0: Enable (default) 1: Disable Read only and default = 1 for peripheral
[6:0]	R/W	011_1000	VBUS_OVP_ALM	VBUS OVP alarm threshold. 2:1 charge-pump mode: VBUS_OVP_ALM = 6V + bit[6:0] ×50mV Default: 8.8V 1:1 bypass mode: VBUS_OVP_ALM = 3V + bit[6:0] ×25mV Default: 4.4V

IBUS_OCP_UCP Register (Register 0x08)

Bit	R/W	Default	Description	
[7]	R/W	0	IBUS_OCP_DIS	IBUS_OCP disable bit. 0: Enable (default) 1: Disable
[6]	R	0	IBUS_UCP_RISE_FLAG	Set 1 and send an INT when IBUS current is higher than IBUS_UCP_RISE threshold. Clear upon read. 0: No IBUS_UCP_RISE 1: IBUS_UCP_RISE event has occurred
[5]	R/W	0	IBUS_UCP_RISE_MASK	Masks an IBUS_UCP_RISE event to send an INT 0: Not masked (default) 1: Masked
[4]	R	0	IBUS_UCP_FALL_FLAG	Set 1 and send an INT when IBUS current lower than IBUS_UCP_FALL threshold. Clear upon read. 0: No IBUS_UCP_FALL 1:IBUS_UCP_FALL event has occurred

[3:0]	R/W	1101	IBUS_OCP	IBUS OCP threshold IBUS_OCP = 1A + bit[3:0] × 250mA, Default: 4.25A

IBUS_OCP_ALM Register (Register 0x09)

Bit	R/W	Default	Description	
[7]	R/W	0	IBUS_OCP_ALM_DIS	IBUS_OCP_ALM disable bit 0: Enable (default) 1: Disable
[6:0]	R/W	101_0000	IBUS_OCP_ALM	IBUS OCP alarm threshold. IBUS_OCP_ALM = bit[6:0] × 50mA, Default: 4A

CONVERTER_STATE Register (Register 0x0A)

Bit	R/W	Default	Description	
[7]	R	0	TDIE_OTP_FLAG	Set 1 and send an INT when die temperature is higher than TDIE threshold. Clear upon read. 0: Normal 1: TDIE_OTP has occurred
[6]	R	0	TDIE_OTP_STAT	Set 1 when die temperature is higher than TDIE threshold. Persists until condition is no longer valid. 0: Normal 1: TDIE_OTP is occurring
[5]	R	0	VBUS_LOW_ERR_FLAG	Set 1 and send an INT when VBUS/VOUT is lower than VBUS_LOW_ERR threshold. Clear upon read. 0: Normal 1: VBUS_LOW_ERR has occurred
[4]	R	0	VBUS_HIGH_ERR_FLAG	Set 1 and send an INT when VBUS/VOUT is higher than VBUS_HIGH_ERR threshold. Clear upon read. 0: Normal 1: VBUS_HGIH_ERR has occurred
[3]	R	0	IBUS_UCP_TIMEOUT_FLAG	Set 1 and send an INT when IBUS is not ramped to the IBUS_UCP_RISE threshold in IBUS_UCP_TIMEOUT time after CHG_EN = 1. Cleared upon read. 0: Normal 1: IBUS_UCP_TIMEOUT has occurred
[2]	R	0	SWITCHING_STAT	Set 1 and send an INT when the converter starts switching and IBUS_UCP_TIMEOUT timer start. Only one INT is sent when switching starts. Persists until condition is no longer valid. 0: Normal

				1: SWITCHING is occurring
[1]	R	0	CON_OCP_FLAG	Set 1 and send an INT when converter current is higher than CON_OCP threshold. Clear upon read. 0: Normal 1: CON_OCP has occurred
[0]	R	0	CFLY_DIAG_FLAG	Set 1 and send an INT when CFLY shorts during converter soft-start. Clear upon read. 0: Normal 1: CFLY_DIG has occurred

CHG_CTL Register (Register 0x0B)

Bit	R/W	Default	Description	
[7]	R/W	0	REG_RST	Register reset. 0: No register reset (default) 1: Reset registers
[6:4]	R/W	100	FSW_SET	Set the switching frequency. 000: 250kHz 001: 250kHz 010: 300kHz 011: 375kHz 100: 500kHz(default) 101: 750kHz 110: 850kHz 111: 1MHz
[3]	R	0	WDT_FLAG	Set 1 and send an INT upon watchdog timeout. Clear upon read. 0: Normal 1: WDT has occurred
[2]	R/W	0	WDT_DIS	Watchdog disable. 0: Enabled (default) 1: Disabled
[1:0]	R/W	00	WDT_TIMER	Watchdog timer setting. 00: 0.5s (default) 01: 1s 10: 5s 11: 30s

CHG_CTL1 Register (Register 0x0C)

Bit	R/W	Default	Description	
[7]	R/W	0	CHG_EN	Charger control bit. 0: Charger disable (default) 1: Charge enable

[6:5]	R	00	MS	Host, peripheral, or standalone operation. 00: Standalone 01: Peripheral 1x: Host
[4:3]	R/W	00	CHG_FSHIFT	Adjust switching frequency for EMI. 00: Nominal frequency (default) 01: Nominal frequency + 10% 10: Nominal frequency - 10% 11: Spread spectrum enable for EMI, +/- 10% nominal frequency change
[2]	R/W	0	TSBUS_OTP_DIS	TSBUS over-temperature protection disable bit. 0: Enable (default) 1: Disable Default for host = 1
[1]	R/W	0	TSBAT_OTP_DIS	TSBAT over-temperature protection disable bit. 0: Enable (default) 1: Disable Default for host = 1
[0]	R/W	0	TDIE_OTP_DIS	TDIE over-temperature protection disable bit. 0: Enable (default) 1: Disable

INT_STAT Register (Register 0x0D)

Bit	R/W	Default	Description	
[7]	R	0	VBAT_OVP_ALM_STAT	Set 1 when VBAT is higher than VBAT_OVP_ALM threshold. Persists until condition is no longer valid. 0: Normal 1: VBAT_OVP_ALM is occurring
[6]	R	0	IBAT_OCP_ALM_STAT	Set 1 when IBAT is higher than IBAT_OCP_ALM threshold. Persists until condition is no longer valid. 0: Normal 1: IBAT_OCP_ALM is occurring
[5]	R	0	VBUS_OVP_ALM_STAT	Set 1 when VBUS is higher than VBUS_OVP_ALM threshold. Persists until condition is no longer valid. 0: Normal 1: VBUS_OVP_ALM is occurring
[4]	R	0	IBUS_OCP_ALM_STAT	Set 1 when IBUS is higher than IBUS_OCP_ALM threshold. Persists until condition is no longer valid. 0: Normal 1: IBUS_OCP_ALM is occurring

[3]	R	0	IBAT_UCP_ALM_STAT	Set 1 when IBAT is lower than IBAT_UCP_ALM threshold. Persists until condition is no longer valid. 0: Normal 1: IBAT_UCP_ALM is occurring
[2]	R	0	VAC_INSERT_STAT	Set 1 when VAC voltage is higher than the VAC_INSERT threshold. 0: Normal 1: VAC_INSERT is occurring
[1]	R	0	VOUT_INSERT_STAT	Set 1 when VOUT voltage is higher than the VOUT_INSERT threshold. 0: Normal 1: VOUT_INSERT is occurring
[0]	R	0	ADC_DONE_STAT	Set 1 when the ADC conversion is completed in 1-shot mode. This bit will change to '0' when an ADC conversion is requested in 1-shot mode, and it will change back to '1' when the conversion is complete. During continuous conversion mode, this bit will be '0' 0: Conversion not complete 1: Conversion complete

INT_FLAG Register (Register 0x0E)

Bit	R/W	Default	Description	
[7]	R	0	VBAT_OVP_ALM_FLAG	Set 1 and send an INT when VBAT is higher than VBAT_OVP_ALM threshold. Clear upon read. 0: Normal 1: VBAT_OVP_ALM has occurred
[6]	R	0	IBAT_OCP_ALM_ FLAG	Set 1 and send an INT when IBAT is higher than IBAT_OCP_ALM threshold. Clear upon read. 0: Normal 1: IBAT_OCP_ALM has occurred
[5]	R	0	VBUS_OVP_ALM_ FLAG	Set 1 and send an INT when VBUS is higher than VBUS_OVP_ALM threshold. Clear upon read. 0: Normal 1: VBUS_OVP_ALM has occurred
[4]	R	0	IBUS_OCP_ALM_ FLAG	Set 1 when IBUS is higher than IBUS_OCP_ALM threshold. Persists until condition is no longer valid. 0: Normal 1: IBUS_OCP_ALM is occurring
[3]	R	0	IBAT_UCP_ALM_ FLAG	Set 1 and send an INT when IBUS is higher than IBUS_OCP_ALM threshold. Clear upon read.

				0: Normal 1: IBUS_OCP_ALM has occurred
[2]	R	0	VAC_INSERT_ FLAG	Set 1 and send an INT when VAC is higher than VAC_INSERT threshold. Clear upon read. 0: Normal 1: VAC_INSERT has occurred
[1]	R	0	VOUT_INSERT_FLAG	Set 1 and send an INT when VOUT is higher than VOUT_INSERT threshold. Clear upon read. 0: Normal 1: VOUT_INSERT has occurred
[0]	R	0	ADC_DONE_FLAG	Set 1 and send an INT when ADC conversion is completed in 1-shot mode. Clear upon read. 0: Normal 1: Conversion completed

INT_MASK Register (Register 0x0F)

Bit	R/W	Default	Description	
[7]	R/W	0	VBAT_OVP_ALM_MASK	VBAT_OVP_ALM mask. 0: Not masked (default) 1: Masked
[6]	R/W	0	IBAT_OCP_ALM_ MASK	IBAT_OCP_ALM mask. 0: Not masked (default) 1: Masked
[5]	R/W	0	VBUS_OVP_ALM_ MASK	VBUS_OVP_ALM mask. 0: Not masked (default) 1: Masked
[4]	R/W	0	IBUS_OCP_ALM_ MASK	IBUS_OCP_ALM mask. 0: Not masked (default) 1: Masked
[3]	R/W	0	IBAT_UCP_ALM_ MASK	IBAT_UCP_ALM mask. 0: Not masked (default) 1: Masked
[2]	R/W	0	VAC_INSERT_ MASK	VAC_INSERT mask. 0: Not masked (default) 1: Masked
[1]	R/W	0	VOUT_INSERT_ MASK	VOUT_INSERT mask. 0: Not masked (default) 1: Masked
[0]	R/W	0	ADC_DONE_MASK	ADC_DONE mask. 0: Not masked (default) 1: Masked

FLT_STAT Register (Register 0x10)

Bit	R/W	Default	Description	
[7]	R	0	VBAT_OVP_STAT	Set 1 when VBAT is higher than VBAT_OVP threshold. Persists until condition is no longer valid. 0: Normal 1: VBAT_OVP is occurring
[6]	R	0	IBAT_OCP_STAT	Set 1 when IBAT is higher than IBAT_OCP threshold. Persists until condition is no longer valid. 0: Normal 1: IBAT_OCP is occurring
[5]	R	0	VBUS_OVP_STAT	Set 1 when VBUS is higher than VBUS_OVP threshold. Persists until condition is no longer valid. 0: Normal 1: VBUS_OVP has occurred
[4]	R	0	IBUS_OCP_STAT	Set 1 when IBUS is higher than IBUS_OCP threshold. Persists until condition is no longer valid. 0: Normal 1: IBUS_OCP is occurring
[3]	R	0	TSBUS_TSBAT_OTP_ ALM_STAT	Set 1 when the TSBUS or TSBAT threshold has been within 4% of the TSBUS_OTP or TSBAT_OTP set threshold. 0: Normal 1:TSBUS_TSBAT_OTP_ALM is occurring
[2]	R	0	TSBAT_OTP_STAT	Set 1 when TSBAT is lower than TSBUS_OTP set threshold. 0: Normal 1: TSBUS_OTP is occurring
[1]	R	0	TSBUS_OTP_STAT	Set 1 when the TSBUS is lower than TSBUS_OTP set threshold. 0: Normal 1: TSBUS_OTP is occurring
[0]	R	0	TDIE_OTP_ALM_STAT	Set 1 when die temperature is higher than TDIE_OTP_ALM threshold. Persists until condition is no longer valid. 0: Normal 1: TDIE_OTP_ALM is occurring

FLT _FLAG Register (Register 0x11)

Bit	R/W	Default	Description	
[7]	R	0	VBAT_OVP_FLAG	Set 1 and send an INT when VBAT is higher than VBAT_OVP threshold. Clear upon read. 0: Normal 1: VBAT_OVP has occurred
[6]	R	0	IBAT_OCP_FLAG	Set 1 and send an INT when IBAT is higher than IBAT_OCP threshold. Clear upon read. 0: Normal 1: IBAT_OCP has occurred
[5]	R	0	VBUS_OVP_FLAG	Set 1 and send an INT when VBUS is higher than VBUS_OVP threshold. Clear upon read. 0: Normal 1: VBUS_OVP has occurred
[4]	R	0	IBUS_OCP_FLAG	Set 1 and send an INT when IBUS is higher than IBUS_OCP threshold. Clear upon read. 0: Normal 1: IBUS_OCP has occurred
[3]	R	0	TSBUS_TSBAT_OTPALM_FLAG	Set 1 when the TSBUS or TSBAT threshold has been within 4% of the TSBUS_OTP or TSBAT_OTP set threshold. Clear upon read. 0: Normal 1: TSBUS_TSBAT_OTP_ALM has occurred
[2]	R	0	TSBAT_OTP_FLAG	Set 1 and send an INT when TSBAT is lower than TSBAT_OTP threshold. Clear upon read. 0: Normal 1: TSBAT_OTP has occurred
[1]	R	0	TSBUS_OTP_FLAG	Set 1 and send an INT when TSBUS is lower than TSBUS_OTP threshold. Clear upon read. 0: Normal 1: TSBUS_OTP has occurred
[0]	R	0	TDIE_OTP_ALM_FLAG	Set 1 and send an INT when TDIE is higher than TDIE_OTP_ALM threshold. Clear upon read. 0: Normal 1: TDIE_OTP_ALM has occurred

FLT _MASK Register (Register 0x12)

Bit	R/W	Default	Description	
[7]	R/W	0	VBAT_OVP_MASK	Masks a VBAT_OVP event to send an INT. 0: Not masked (default) 1: Masked
[6]	R/W	0	IBAT_OCP_MASK	Masks an IBAT_OCP event to send an INT. 0: Not masked (default) 1: Masked
[5]	R/W	0	VBUS_OVP_MASK	Masks a VBUS_OVP event to send an INT. 0: Not masked (default) 1: Masked
[4]	R/W	0	IBUS_OCP_MASK	Masks an IBUS_OCP event to send an INT. 0: Not masked (default) 1: Masked
[3]	R/W	0	TSBUS_TSBAT_OTP_ALM_MASK	Masks a TSBUS_TSBAT_OTP_ALM event to send an INT. 0: Not masked (default) 1: Masked
[2]	R/W	0	TSBAT_OTP_MASK	Masks a TSBAT_OTP event to send an INT 0: Not masked (default) 1: Masked
[1]	R/W	0	TSBUS_OTP_MASK	Masks a TSBUS_OTP event to send an INT 0: Not masked (default) 1: Masked
[0]	R/W	0	TDIE_OTP_ALM_MASK	Masks a TDIE_ALM_OTP event to send an INT. 0: Not masked (default) 1: Masked

DEVICE_INFO Register (Register 0x13)

Bit	R/W	Default	Description
[7:4]	R	0000	Device Revision.
[3:0]	R	1110	Device ID: 1110.

ADC_CTL Register (Register 0x14)

Bit	R/W	Default	Description	
[7]	R/W	0	ADC_EN	ADC control. 0: Disable (default) 1: Enable

[6]	R/W	0	ADC_RATE	ADC conversion rate control. 0: Continuous mode (default) 1: 1-shot mode
[5:1]	R	0000_0	Reserved	
[0]	R/W	0	IBUS_ADC_DIS	IBUS_ADC control. 0: Enable conversion (default) 1: Disable conversion Read only and default = 1 for peripheral

AD_ EN Register (Register 0x15)

Bit	R/W	Default	Description	
[7]	R/W	0	VBUS_ADC_DIS	VBUS ADC control bit. 0: Enable (default) 1: Disable Read only and default = 1 for peripheral
[6]	R/W	0	VAC_ADC_DIS	VBAT_ADC control bit. 0: Enable (default) 1: Disable Read only and default = 1 for peripheral
[5]	R/W	0	VOUT_ADC_DIS	VOUT ADC control bit. 0: Enable (default) 1: Disable Read only and default = 1 for peripheral
[4]	R/W	0	VBAT_ADC_DIS	VBAT ADC control bit. 0: Enable (default) 1: Disable Read only and default = 1 for peripheral
[3]	R/W	0	IBUS_ADC_DIS	IBAT_ADC control bit. 0: Enable (default) 1: Disable Read only and default = 1 for peripheral
[2]	R/W	0	TSBUS_ADC_DIS	TSBUS_ADC control bit. 0: Enable (default) 1: Disable Read only and default = 1 for host
[1]	R/W	0	TSBAT_ADC_DIS	TSBAT_ADC control bit. 0: Enable (default) 1: Disable Read only and default = 1 for host
[0]	R/W	0	TDIE_ADC_DIS	TDIE_ADC control bit. 0: Enable (default) 1: Disable

IBUS_ADC1 Register (Register 0x16)

Bit	R/W	Default	Description	
[7]	R	0	Sign bit	0: Positive 1: Negative
[6:0]	R	000_0000	IBUS_ADC1	IBUS ADC high byte. HSB<6:0>: 5120mA, 2560mA, 1280mA, 640mA, 320mA, 160mA, 80mA

IBUS_ADC0 Register (Register 0x17)

Bit	R/W	Default	Description	
[7:0]	R	0000_0000	IBUS_ADC0	IBUS ADC low byte. LSB<7:0>: 40mA, 20mA, 10mA, 5mA, 2.5mA, 1.25mA, 0.625mA, 0.3125mA IBUS_ADC = (-1)^(Reg0x16 bit[7]) × (Reg0x16 bit[6:0] × 80mA + Reg0x17 bit[7:0] × 0.3125mA)

VBUS_ADC1 Register (Register 0x18)

Bit	R/W	Default	Description	
[7]	R	0	Sign bit	0: Positive 1: Negative
[6:0]	R	000_0000	VBUS_ADC1	VBUS ADC high byte. HSB<6:0>: 16384mV, 8192mV, 4096mV, 2048mV, 1024mV, 512mV, 256mV

VBUS_ADC0 Register (Register 0x19)

Bit	R/W	Default	Description	
[7:0]	R	0000_0000	VBUS_ADC0	VBUS ADC low byte. LSB<7:0>: 128mV, 64mV, 32mV, 16mV, 8mV, 4mV, 2mV, 1mV VBUS_ADC = (-1)^(Reg0x18 bit[7]) × (Reg0x18 bit[6:0] × 256mV + Reg0x19 bit[7:0] × 1mV)

VAC_ADC1 Register (Register 0x1A)

Bit	R/W	Default	Description	
[7]	R	0	Sign bit	0: Positive 1: Negative
[6:0]	R	000_0000	VAC_ADC1	VAC ADC high byte. HSB<6:0>: 16384mV, 8192mV, 4096mV, 2048mV, 1024mV, 512mV, 256mV

VAC_ADC0 Register (Register 0x1B)

Bit	R/W	Default	Description	
[7:0]	R	0000_0000	VAC_ADC0	VAC ADC low byte. LSB<7:0>: 128mV, 64mV, 32mV, 16mV, 8mV, 4mV, 2mV, 1mV VAC_ADC = (-1)^(Reg0x1A bit[7]) × (Reg0x1A bit[6:0] × 256mV + Reg0x1B bit[7:0] × 1mV)

VOUT_ADC1 Register (Register 0x1C)

Bit	R/W	Default	Description	
[7]	R	0	Sign bit	0: Positive 1: Negative
[6:0]	R	000_0000	VOUT_ADC1	VOUT ADC high byte. HSB<6:0>: 8192mV, 4096mV, 2048mV, 1024mV, 512mV, 256mV, 128mV

VOUT_ADC0 Register (Register 0x1D)

Bit	R/W	Default	Description	
[7:0]	R	0000_0000	VOUT_ADC0	VOUT ADC low byte. LSB<7:0>: 64mV, 32mV, 16mV, 8mV, 4mV, 2mV, 1mV, 0.5mV VOUT_ADC = (-1)^(Reg0x1C bit[7]) × (Reg0x1C bit[6:0] × 128mV + Reg0x1D bit[7:0] × 0.5mV)

VBAT_ADC1 Register (Register 0x1E)

Bit	R/W	Default	Description	
[7]	R	0	Sign bit	0: Positive 1: Negative
[6:0]	R	000_0000	VBAT_ADC1	VBAT ADC high byte. HSB<6:0>: 8192mV, 4096mV, 2048mV, 1024mV, 512mV, 256mV, 128mV

VBAT_ADC0 Register (Register 0x1F)

Bit	R/W	Default	Description	
[7:0]	R	0000_0000	VBAT_ADC0	VBAT ADC low byte. LSB<7:0>: 64mV, 32mV, 16mV, 8mV, 4mV, 2mV, 1mV, 0.5mV VBAT_ADC = (-1)^(Reg0x1E bit[7]) × (Reg0x1E bit[6:0] × 128mV + Reg0x1F bit[7:0] × 0.5mV)

IBAT_ADC1 Register (Register 0x20)

Bit	R/W	Default	Description	
[7]	R	0	Sign bit	0: Positive 1: Negative
[6:0]	R	000_0000	IBAT_ADC1	IBAT ADC high byte. HSB<6:0>: 10240mA, 5120mA, 2560mA, 1280mA, 640mA, 320mA, 160mA

IBAT_ADC0 Register (Register 0x21)

Bit	R/W	Default	Description	
[7:0]	R	0000_0000	IBAT_ADC0	IBAT ADC low byte. LSB<7:0>: 80mA, 40mA, 20mA, 10mA, 5mA, 2.5mA, 1.25mA, 0.625mA IBAT_ADC = (-1)^(Reg0x20 bit[7]) × (Reg0x20 bit[6:0] × 160mA + Reg0x21 bit[7:0] × 0.625mA)

TSBUS_ADC1 Register (Register 0x22)

Bit	R/W	Default	Description	
[7]	R	0	Sign bit	0: Positive 1: Negative
[6:2]	R	00000	Reserved	
[1:0]	R	00	TSBUS_ADC1	TSBUS ADC high byte. HSB<1:0>: 50%, 25%

TSBUS_ADC0 Register (Register 0x23)

Bit	R/W	Default	Description	
[7:0]	R	0000_0000	TSBUS_ADC0	TSBUS ADC low byte. LSB<7:0>: 12.5%, 6.25%, 3.125%, 1.5625%, 0.78125%, 0.39063%, 0.19531%, 0.09766% TSBUS_ADC = (-1)^(Reg0x22 bit[7]) × (Reg0x22 bit[1:0] × 25% + Reg0x23 bit[7:0] × 0.09766%)

TSBAT_ADC1 Register (Register 0x24)

Bit	R/W	Default	Description	
[7]	R	0	Sign bit	0: Positive 1: Negative

[6:2]	R	00000	Reserved	
[1:0]	R	00	TSBAT_ADC1	TSBAT ADC high byte. HSB<1:0>: 50%, 25%

TSBAT_ADC0 Register (Register 0x25)

Bit	R/W	Default	Description	
[7:0]	R	0000_0000	TSBAT_ADC0	TSBAT ADC low byte. LSB<7:0>: 12.5%, 6.25%, 3.125%, 1.5625%, 0.78125%, 0.39063%, 0.19531%, 0.09766% TSBAT_ADC = (-1)^(Reg0x24 bit[7]) × (Reg0x24 bit[1:0] × 25% + Reg0x25 bit[7:0] × 0.09766%)

TDIE_ADC1 Register (Register 0x26)

Bit	R/W	Default	Description	
[7]	R	0	Sign bit	0: Positive 1: Negative
[6:1]	R	000_000	Reserved	
[0]	R	0	TDIE _ADC1	TDIEADC high byte. HSB<0>: 128°C

TDIE_ADC0 Register (Register 0x27)

Bit	R/W	Default	Description	
[7:0]	R	0000_0000	TDIE _ADC0	TDIE ADC low byte. LSB<7:0>: 64°C, 32°C, 16°C, 8°C, 4°C, 2°C, 1°C, 0.5°C TDIE_ADC = (-1)^(Reg0x26 bit[7]) × (Reg0x26 bit[0] × 128°C + Reg0x27 bit[7:0] × 0.5°C)

TSBUS_OTP Register (Register 0x28)

Bit	R/W	Default	Description	
[7:0]	R	0001_0101	TSBUS_OTP	TSBUS Percentage Fault Threshold. TSBUS_FLT = TSBUS_FLT[7:0] × 0.19531% Default = 4.1%

TSBAT_OTP Register (Register 0x29)

Bit	R/W	Default	Description	
[7:0]	R	0001_0101	TSBAT_OTP	TSBAT Percentage Fault Threshold. TSBAT_FLT = TSBAT_FLT[7:0] × 0.19531% Default = 4.1%

TDIE_ALM Register (Register 0x2A)

Bit	R/W	Default	Description	
[7:0]	R	1100_1000	TDIE_ALM	TDIE alarm fault threshold setting. TDIE_ALM = 25°C + bit[7:0] × 0.5°C Default = 125°C

REG_CTL Register (Register 0x2B)

Bit	R/W	Default	Description	
[7:5]	R/W	111	IBUS_UCP_TIMEOUT	Adjustable timeout for IBUS to rise to IBUS_UCP_RISE threshold. 000: Timeout disabled 001: 12.5ms 010: 25ms 011: 50ms 100: 100ms 101: 400ms 110: 1.5s 111: 100s (default)
[4]	R/W	0	REG_EN	Enables the device to regulate the output based on VBAT_OVP and IBAT_OCP thresholds. 0: Disable (default) 1: Enable
[3]	R/W	0	VOUT_OVP_DIS	VOUT overvoltage control bit. 0: Enable (default) 1: Disable
[2]	R/W	0	IBUS_UCP_RISE_THRESH	IBUS_UCP_RISE threshold. IBUS current should rise to this threshold within the IBUS_UCP_TIMEOUT period. 0: 300mA rising, 150mA falling (default) 1: 500mA rising, 250mA falling
[1]	R/W	0	IBAT_RSENSE	This bit selects the external battery current sense resistor value of 1mΩ or 2mΩ. 0: 2mΩ (default) 1: 1mΩ
[0]	R/W	0	VAC_PD_EN	VAC pulldown resistor control bit. 0: Disable (default) 1: Enable(125Ω resistor)

REG_THRESHOLD Register (Register 0x2C)

Bit	R/W	Default	Description	
[7:6]	R/W	00	IBAT_REG	These two bits set the threshold below IBAT_OCP where the device starts regulation. 00: 200mA below IBAT_OCP setting (default) 01: 300mA below IBAT_OCP setting 10: 400mA below IBAT_OCP setting 11: 500mA below IBAT_OCP setting
[5:4]	R/W	0	VBAT_REG	These two bits set the threshold below VBAT_OVP where the device starts regulation. 00: 50mV below VBAT_OVP setting (default) 01: 100mV below VBAT_OVP setting 10: 150mV below VBAT_OVP setting 11: 200mV below VBAT_OVP setting
[3]	R	0	VBAT_REG_STAT	Set 1 when VBAT_REG is active. Persists until condition is no longer valid. 0: Normal 1: VBAT_REG is occurring
[2]	R	0	IBAT_REG_STAT	Set 1 when IBAT_REG is active. Persists until condition is no longer valid. 0: Normal 1: IBAT_REG is occurring
[1]	R	0	VDR_OVP_STAT	Set 1 when the voltage difference between VAC and VBUS is higher than VDR_OVP threshold. Persists until condition is no longer valid. 0: Normal 1: VDR_OVP is occurring
[0]	R	0	VOUT_OVP_STAT	Set 1 when the VOUT is higher than VOUT_OVP threshold. Persists until condition is no longer valid. 0: Normal 1: VOUT_OVP is occurring

REG_FLAG Register (Register 0x2D)

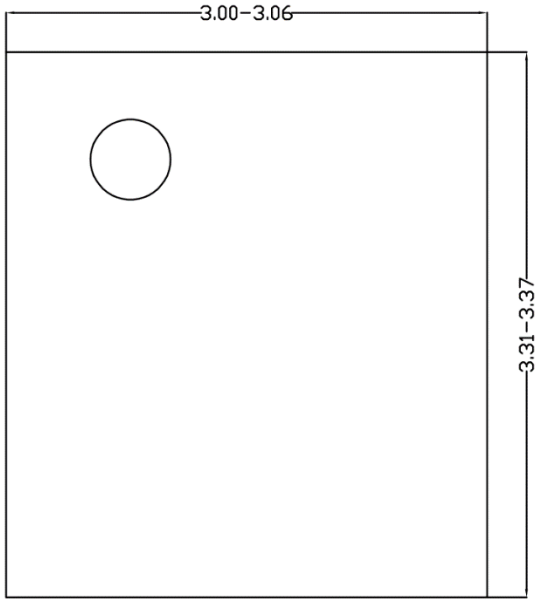
Bit	R/W	Default	Description	
[7]	R	0	VBAT_REG_FLAG	Set 1 and send an INT when VBAT_REG has been active. Clear upon read. 0: Normal 1: VBAT_REG has occurred
[6]	R	0	IBAT_REG_FLAG	Set 1 and send an INT when IBAT_REG has been active. Clear upon read. 0: Normal

				1: IBAT_REG has occurred
[5]	R	0	VDR_OVP_FLAG	Set 1 and send an INT when VDR_OVP has occurred. Clear upon read. 0: Normal 1: VDR_OVP has occurred
[4]	R	0	VOUT_OVP_FLAG	Set 1 and send an INT when VOUT_OVP has occurred. Clear upon read. 0: Normal 1: VOUT_OVP has occurred
[3]	R/W	0	VBAT_REG_MASK	Masks an VBAT_REG event to send an INT 0: Not masked (default) 1: Masked
[2]	R/W	0	IBAT_REG_MASK	Masks an IBAT_REG event to send an INT 0: Not masked (default) 1: Masked
[1]	R/W	0	VDR_OVP_MASK	Masks an VDR_OVP event to send an INT 0: Not masked (default) 1: Masked
[0]	R/W	0	VOUT_OVP_MASK	Masks an VOUT_OVP event to send an INT 0: Not masked (default) 1: Masked

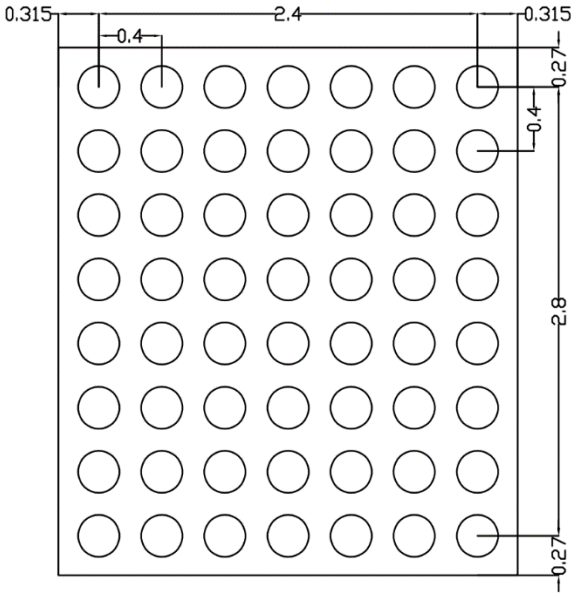
REG_STAT_FLAG Register (Register 0x2E)

Bit	R/W	Default	Description	
[7:5]	R	000	Reserved	
[4]	R/W	0	VBUS_LOW_ERR_DEGLITCH_SET	This bit sets the deglitch time for VBUS_LOW_ERR. 0: 10μs (default) 1: 10ms
[3]	R/W	0	IBUS_UCP_FALL_DEGLTICH_SET	This bit sets the deglitch time for VBUS_UCP_FALL. 0: 10μs (default) 1: 5ms
[2:0]	R	000	Reserved	

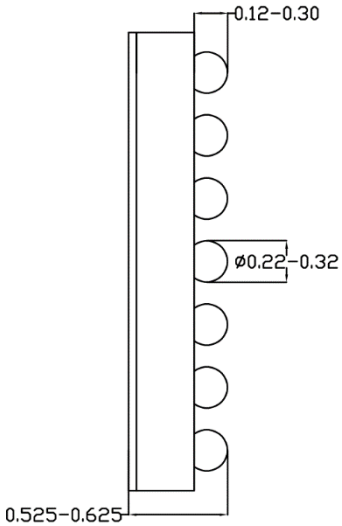
CSP3.03 × 3.34-56 Package Outline Drawing



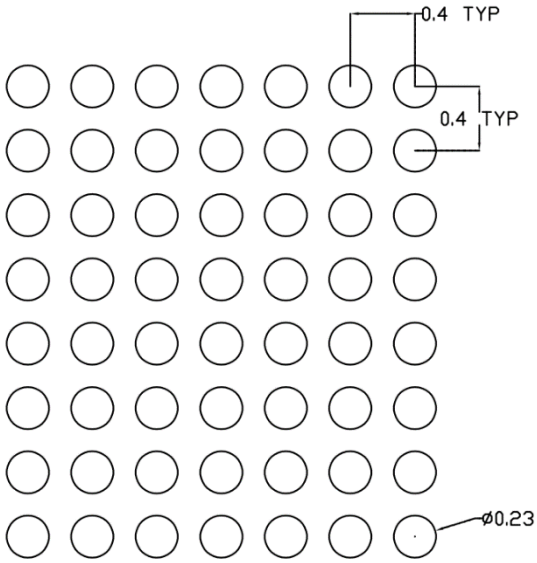
Top view



Bottom view



Side view



Recommended PCB layout
(Reference only)

Note: All dimensions are in millimeter and exclude mold flash and metal burr.

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