SY22121

Asynchronous Boost Regulator With Two Current Sinks for Smartphone LCD Panel

General Description

SY22121, high efficiency Boost regulator with two matching current sinks operates with fixed switching frequency and peak current mode control, and can drive up to two strings of white LEDs in LCD panel backlight applications. It operates over a wide input voltage range from 2.7V to 28V with a resistor programmable LED current up to 30mA.

The integrated 40V power MOSFETs and dual current sinks, compensation, and soft-start reduce the number of external components required. The integrated analog PWM dimming and 1-wire digital dimming provide accurate LED current control.

The SY22121 also provides open/short LED, Boost output overvoltage, and overtemperature protection.

The SY22121 is available in a Pb-Free WLCSP

1.31mm ×1.31mm-9 bump package.

Features

- 2.7V to 28V Input Voltage Range
- Fixed 1MHz Switching Frequency
- Programmable LED Current Up To 30mA per String With ±1% Accuracy
- 2 Current Sinks -Up to 10 LEDs per String
- Quiescent Current I_Q 500 μA(typ.)
- Shutdown Current I_{SHDN} 2μA (typ.)
- Integrated 40V/250mΩ Boost Switch
- LED Sink Voltage 165mV (typ.)
- 1-Wire Digital Dimming on the EN Pin
- Up to 100:1 PWM Brightness Control at 20kHz with 500ns (typ.) Minimum On-Time
- Cycle-by-Cycle Inductor Current Limit
- Internal Compensation
- Internal Soft-Start Limits Inrush Current
- Open/Short LED, Overvoltage, and Overtemperature Protection
- RoHS-Compliant and Halogen-Free
- WLCSP 1.31mm×1.31mm-9 Package

Applications

- Smartphones, Tablets
- LCD Display Backlights

Typical Application

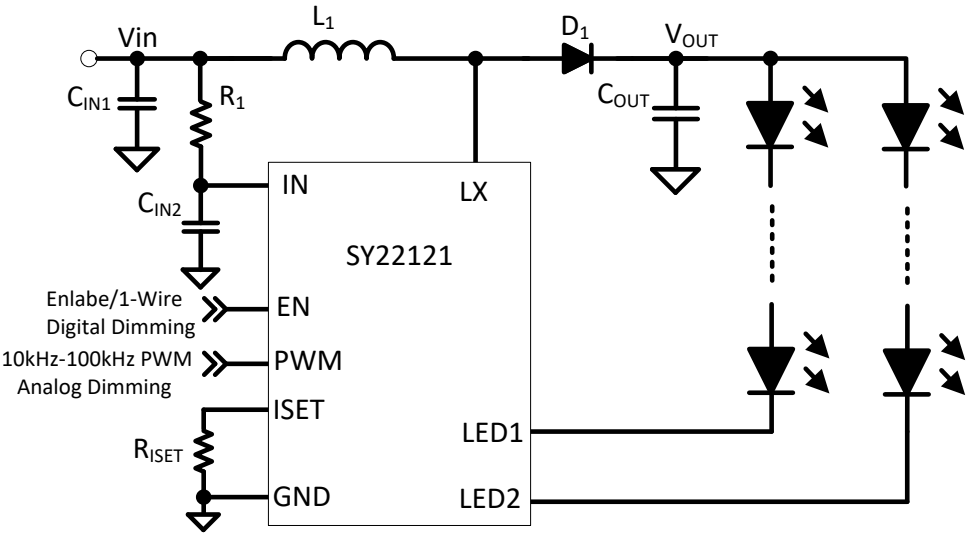


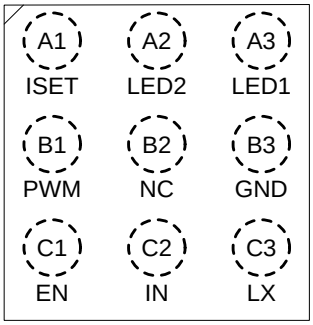
Figure 1. Typical Application Circuit

Ordering Information

Ordering Part Number	Package Type	Top Mark
SY22121POC	WLCSP 1.31mm×1.31mm-9 RoHS-Compliant and Halogen-Free	By***xyz***

x = year code, y = week code, z = lot number code

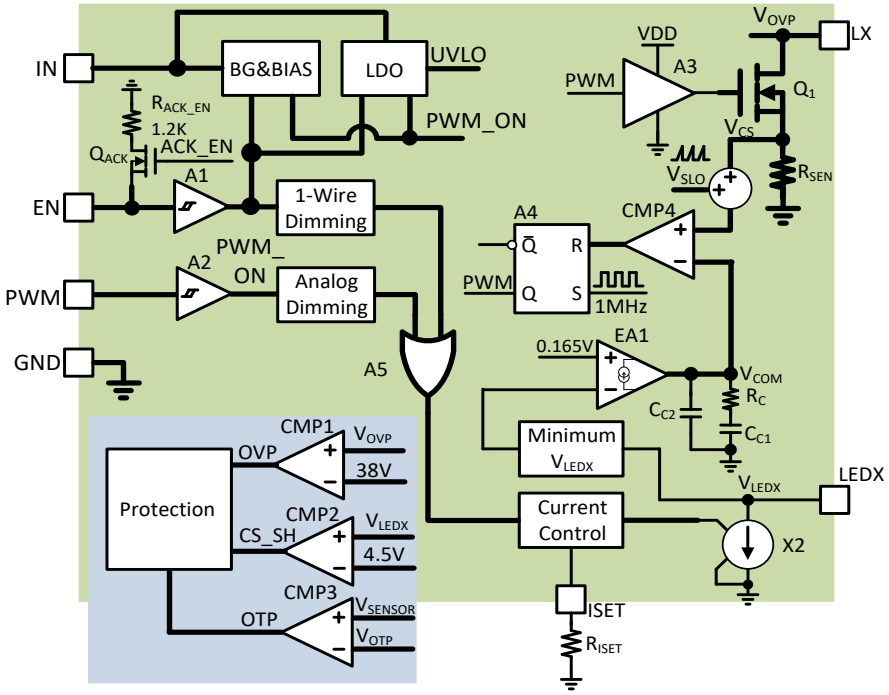
Pinout (top view)



Pin Description

Pin No.	Pin Name	Pin Description
A1	ISET	LED current programming pin. Connect a resistor to ground to program the current in each LED string up to 30mA. LED current: $I_{LED} = (1.229 \times 1030)/R_{ISET}$ mA, where R_{ISET} is in kΩ.
A2	LED2	The current source pin for LED String 2. Connect this pin to the cathode of the LED. Connect this pin to ground when not used.
A3	LED1	The current source pin for LED String 1. Connect this pin to the cathode of the LED. Connect this pin to ground when not used.
B1	PWM	PWM dimming input. 10kHz–100kHz dimming frequency range. Ensure the minimum PWM ON time is more than 500ns.
B2	NC	Null pad. It can be connected to the adjacent pin.
B3	GND	Ground pin.
C1	EN	Enable control and 1-wire digital signal input. Connect this pin to IN when not used.
C2	IN	Input voltage pin. Decouple this pin to the GND pin with a ceramic capacitor.
C3	LX	Internal switching MOSFET drain. This pin is used for sensing the output voltage for open LED protection.

Block Diagram



Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
IN, EN, PWM	-0.3	30	V
LX,LED1,LED2	-0.3	40	
ISET	-0.3	3.6	
Junction Temperature, Operating		150	°C
Lead Temperature (Soldering,10s)		260	
Storage Temperature	-65	150	

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
IN	2.7	28	V
LX	IN	38	
Inductor L	4.7	10	µH
Input Capacitor	1.0		µF
Output Capacitor	1.0	2.2	
Junction Temperature	-40	125	°C
Ambient Temperature	-40	85	

Thermal Information

Parameter (Note 2)	WLCSP 1.31*1.31_9	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	107	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	1.5	
P_D Power Dissipation T_A = 25°C	0.93	W

Electrical Characteristics

(V_{IN} = 3.6V, T_A = 25°C, unless otherwise specified.)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input voltage	Input Voltage Range	V_{IN}		2.7		28	V
	Quiescent Current	I_Q	EN = 1,PWM = 1,LED1 = LED2 = 1V		500		μA
	Shutdown Current	I_{SHDN}	EN = 0		2		μA
	IN UVLO Rising Threshold	$V_{IN,UVLO}$			2.5	2.7	V
	UVLO Hysteresis	$V_{UVLO,HYS}$			100		mV
EN and PWM Dimming	PWM Input Low Logic	V_{PWML}				0.4	V
	PWM Input High Logic	V_{PWMH}		1.5			V
	PWM Dimming Accuracy	I_{LEDAVE}	R_{ISET} = 63.4kΩ (I_{LEDX} = 19.97mA) PWM = 10kHz/10% Duty I_{LEDAVE} = (I_{LED1} + I_{LED2})/2	1.797	1.997	2.197	mA
	EN Input Low Logic	V_{ENL}				0.4	V
	EN Input High Logic	V_{ENH}		1.5			V
	PWM Internal Pulldown Resistor	R_{PWM}			800		kΩ
	EN Internal Pulldown Resistor	R_{EN}			800		kΩ
	PWM Width to Shutdown	t_{PWMSD}	PWM high to low		15		ms
	EN Width to Shutdown	t_{ENSD}	EN high to low		1		ms
Oscillator	Switching Frequency	F_{SW}		0.8	1	1.2	MHz
	Boost Stage Maximum Duty Cycle	D_{MAX}	Guarantee by design		95		%
Power MOSFET R_{DSON}		R_{DSON}	V_{IN} = 3.6V		250		mΩ
Current Sink Regulation	LED Current Setting	I_{LEDAVE}	R_{ISET} = 63.4kΩ (I_{LEDX} = 19.97mA) I_{LEDAVE} = (I_{LED1}+I_{LED2})/2	19.57	19.97	20.36	mA
	LED Current Matching	I_{LEDM}	R_{ISET} = 63.4kΩ (I_{LEDX} = 19.97mA), (I_{LEDMAX} - I_{LEDAVE})/I_{LEDAVE}		1%	2%	
	LED Regulation Voltage	V_{LEDx}	Guarantee by design		165		mV
Protection	Main MOSFET Peak Current Limit	I_{LIM}	D = D_{MAX}	1	1.5		A
	OVP Rising Threshold	V_{OVP}		36	38	39.5	V
	LED String Shorted Shutoff Threshold	$V_{LEDXOVP}$	Measured on LEDx pin	4.2	4.5	4.8	V

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
1-Wire Digital Dimming Interface	1-Wire Detection Delay	t_{SWP_DEL}	Measured from EN low to high	100			μs
	1-Wire Detection Time	t_{SWP_DET}	EN pin low width	260			μs
	1-Wire Detection Window(Note 4)	t_{SWP_WIN}	Measured the time from the first and second EN rising edge time	1			ms
	Start Time of Program Stream	t_{START}		2			μs
	End Time of Program Stream	t_{EOS}		2		360	μs
	High Time of Low Bit (Logic 0)	t_{H_LB}		2		120	μs
	Low Time of Low Bit (Logic 0)	t_{L_LB}		$2xt_{H\_LB}$		240	μs
	High Time of High Bit (Logic 1)	t_{H_HB}		$2xt_{H\_LB}$		240	μs
	Low Time of High Bit (Logic 1)	t_{L_HB}		2		120	μs
	Acknowledge Valid Time	t_{ACK_VAL}				2	μs
	Duration of Acknowledge Condition	t_{ACK_DUR}				512	μs
Thermal Shutdown	Thermal Shutdown Temperature	T_{SD}	Guarantee by design		160		°C
	Thermal Shutdown Hysteresis	T_{HYS}	Guarantee by design		15		°C

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

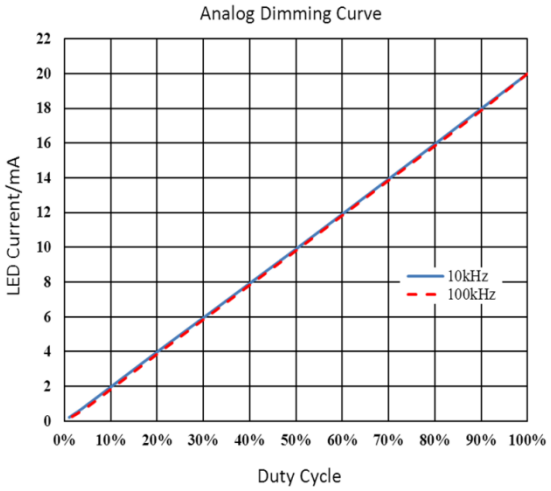
Note 3: The device is not guaranteed to function outside its operating conditions.

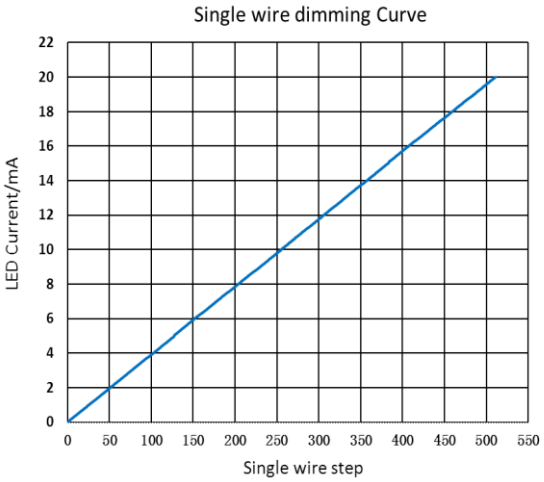
Note 4: To select the1-wire digital dimming interface, after $t_{DIGITAL\_DELAY}$ delay from EN low to high, drive the EN pin low for more than $t_{DIGITAL\_DETECT}$ before $t_{DIGITAL\_WIN}$ expires.

Note 5: Acknowledge condition active 0. This condition is only applied when the RFA bit is set to 1. To use this feature, the master must have an open-drain output, and the data line needs to be pulled up by the master with a resistor load.

Typical Performance Characteristics

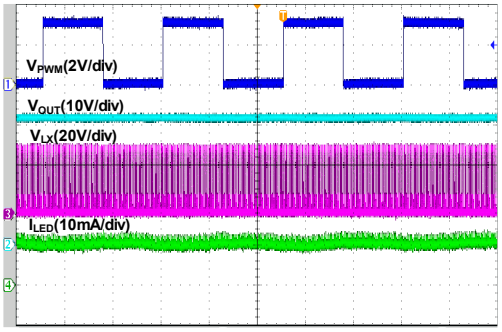
(V_{IN} = 3.6V, I_{LED} = 20mA, 2 LED strings, 10 LEDs per string)





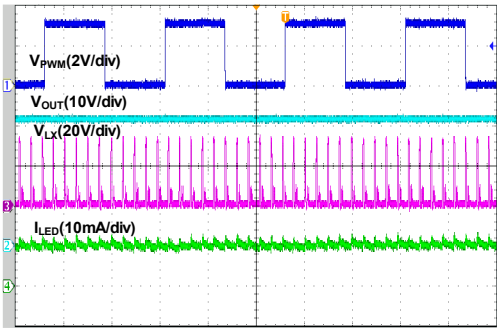
Analog Dimming

(f_{PWM}=10kHz d=50%)

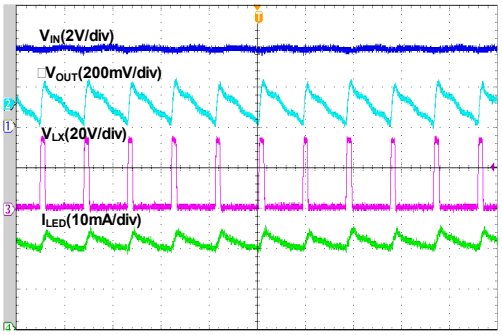


Analog Dimming

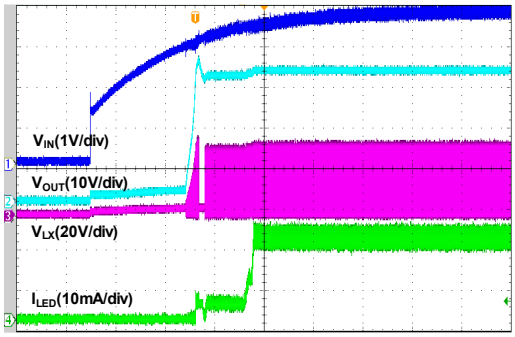
(f_{PWM}=100kHz d=50%)



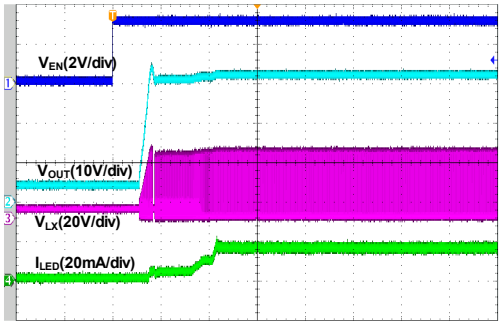
Steady state



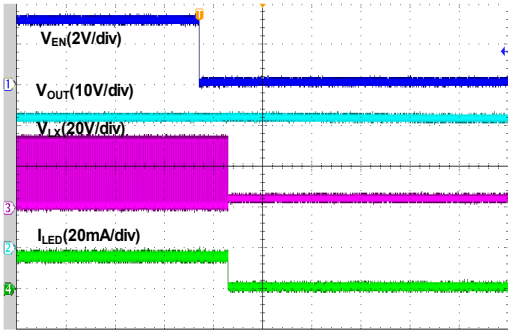
Start up from V_{IN}



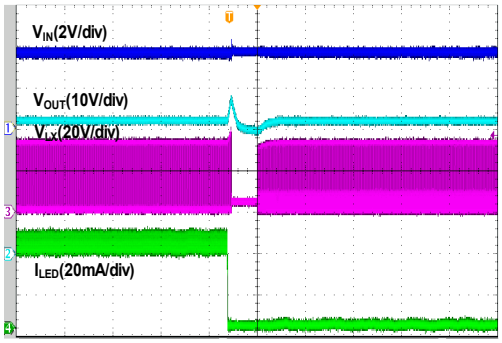
EN start up



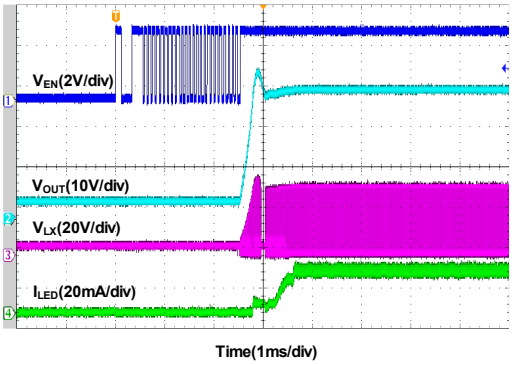
EN shut down



Open LED protection(Open LED2)



Single wire start up



Detailed Description

The SY22121 high efficiency Boost regulator with two matching current sinks operates using fixed frequency and peak current mode control with slope compensation. The device can drive up to two strings of white LEDs in LCD panel backlight applications. It operates over a wide input voltage range from 2.7V to 28V with a resistor programmable LED current up to 30mA.

The integrated 40V Boost power MOSFET and dual channel current sink, compensation, and soft-start reduce the number of external components required. The integrated analog PWM dimming and 1-wire digital dimming provide accurate LED current control.

The SY22121 also provides open/short LED,overvoltage, and overtemperature protections.

LED Current Setting

The SY22121 current sinks can provide up to 30mA current per channel. Independent of the dimming method, the maximum LED string current (current when dimming duty cycle is 100%) can be programmed using an external resistor R_{ISET} (kΩ) connected to the ISET pin according to the equation below:

$$I_{LEDMAX} = （1.229V \times 1030)/R_{ISET}$$

Boost Soft-start

When enabled, SY22121 starts ramping up the output voltage by using a reduced cycle-by-cycle current limit of I_{LIMST} (0.7A typ.), for a duration of t_{LIMST} (5ms typ.). This reduces the inrush current at power-up.

Brightness Control

The SY22121 controls the LED strings current using analog dimming. It can receive either a 10kHz~100KHz PWM signal at the PWM pin (PWM analog dimming) or digital commands at the EN pin (1-wire digital dimming) for brightness adjustment. If the 1-wire dimming interface is selected, the PWM pin should be driven high. If PWM interface is selected, the EN pin should be driven high.

1-Wire Digital Dimming

The EN pin can be used as a digital interface for brightness control. In order to enable the 1-wire digital interface, the IC must recognize the following digital pattern on the EN pin every time it starts from shutdown mode:

1. V_{IN} voltage is higher than the UVLO threshold and the PWM pin is pulled high.

2. The 1-wire digital interface detection window starts when the EN pin is pulled from low to high to enable the SY22121.

3. After the digital dimming detection delay (t_{SWP_DEL}, 100μs) expires, EN needs to be driven low for more than the digital dimming detection time (t_{SWP_DET}, 260μs).

step 3 must be finished before the 1-wire digital interface detection window (t_{SWP_WIN}, 1ms) expires. Once step 3 is finished, the 1-wire digital interface is enabled and 1-wire digital communication can start. See Figure 2 for the digital dimming pattern timing.

Timing definitions: t_{SWP_DEL} is the time required for the internal bias and reference to settle, t_{SWP_DET} is the time used to detect 1-wire dimming mode and measure the EN pin low time, t_{SWP_WIN} is the 1-wire dimming mode window time, t_{ENSD} is the delay time to turn off (shutdown) the device.

The SY22121 supports 9-bit brightness code to achieve 511 steps dimming. Using the 1-wire digital interface, a master can program the 9-bit code BRT_CODE[8:0]D8 (MSB) to D0 (LSB) to any of the 511 current steps with a single command. The default code for BRT_CODE[8:0] is 0b000000000 when the device is enabled the first time. The programmed value will be stored in an internal register and used to set the dual-channel current according to the following equation:

$$I_{LEDX} = I_{LEDMAX} \times BRT\_CODE[8:0]/511$$

where I_{LEDMAX} is the maximum LED current set by R_{ISET} at the ISET pin, and BRT_CODE[8:0] is the 9-bit brightness code D8–D0 programmed using the 1-wire digital interface.

The code will be reset to its default value when the device is shut down or disabled.

When the 1-wire digital interface is used, the PWM pin can be connected to the V_{IN} pin. In this case, the EN pin alone can enable and disable the device. Pull EN low for more than 2.5ms(Max.) or pull PWM low for more than 25ms(Max.) to force the device in shutdown mode.

1-Wire Digital Programming

The 1-wire digital interface is a simple but flexible single-pin interface to configure the current for both channels.

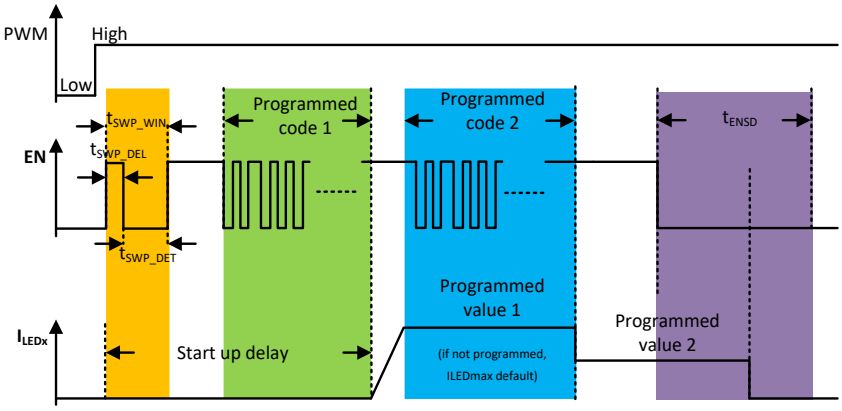


Figure 2. 1-wire Digital Dimming

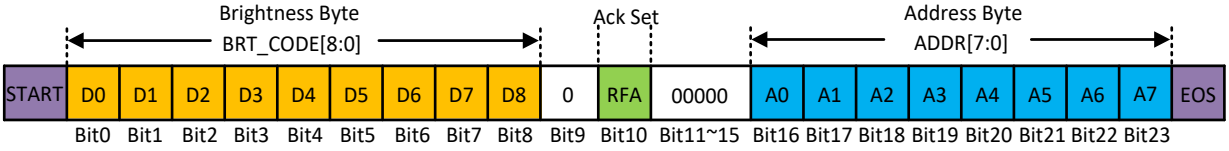


Figure 3. 1-Wire Digital Interface Protocol

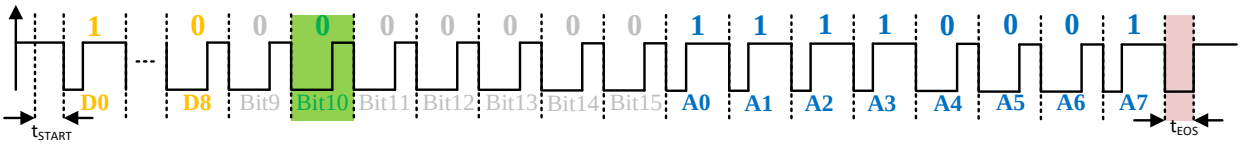


Figure 4. 1-Wire Digital Interface Timing, with ACK_EN= 0

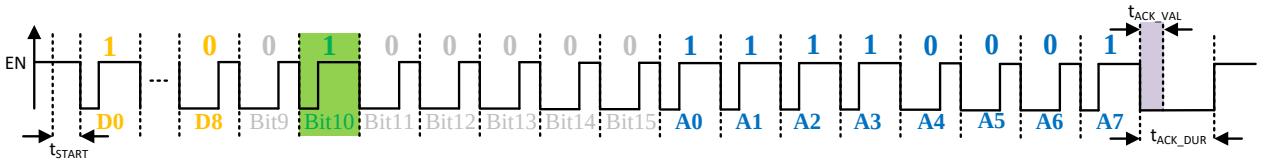


Figure 5. 1-Wire Digital Interface Timing, with ACK_EN=1

Figure 3 and Table 1 give an overview of the protocol used by the SY22121. A command consists of 24 bits, including an 8-bit device address byte ADDR[7:0] and a 16-bit data byte. All 24 bits should be transmitted together each time, with the LSB transmitted first. The device address byte A7 (MSB) through A0 (LSB) is fixed as 0x8F. The brightness byte BRT_CODE[8:0] includes the 9 bits D8 (MSB) through D0 (LSB) for brightness information, along with the ACK_EN bit. The ACK_EN bit set to 1 indicates the request for acknowledge condition. The acknowledge condition is only applied when the protocol is received correctly.

Figure 4 shows the protocol without acknowledge request (ACK_EN bit = 0), and Figure 5 shows the protocol with acknowledge request (ACK_EN bit = 1). The EN pin must be pulled high for at least t_{START} (2μs) before the bit transmission starts with the falling edge, after SY22121 is initialize in 1-wire mode. The transmission of each command ends with an end of stream (EOS) condition for at least t_{EOS} (2μs). Note that if ACK_EN=1, the SY22121 needs more than t_{ACK_VAL} (2μs) to pull down the EN pin after the 24th data bit transmitted.

Table 1. 1-Wire Digital Interface Bit

Byte	Bit Number	Name	Direction	Default	Description
ADDR[7:0] 0x8F	23	ADDR_Bit7	I	1	8-bit device address, fixed to 0x8F for SY22121
	22	ADDR_Bit6	I	0	
	21	ADDR_Bit5	I	0	
	20	ADDR_Bit4	I	0	
	19	ADDR_Bit3	I	1	
	18	ADDR_Bit2	I	1	
	17	ADDR_Bit1	I	1	
	16	ADDR_Bit0	I	1	
NULL Bit[5:1] 0b00000	15	NULL_Bit5	I	0	zero bits, 0b00000
	14	NULL_Bit4	I	0	
	13	NULL_Bit3	I	0	
	12	NULL_Bit2	I	0	
	11	NULL_Bit1	I	0	
RFA 0b0	10	ACK_EN	I	0	Acknowledge enable set.'1' acknowledge is enabled, the chip will pull down EN pin to make the master receive the slave feedback when the 24th bit transmitted and becomes as output pin;'0' acknowledge is disabled, the chip will implement the EOS routine.
Null Bit[0] 0b0	9	NULL_Bit0	I	0	zero bit, 0b0
BRT_CODE[8:0] 0x1FF	8	BRT_CODE_Bit8	I	1	9-bit brightness code
	7	BRT_CODE_Bit7	I	1	
	6	BRT_CODE_Bit6	I	1	
	5	BRT_CODE_Bit5	I	1	
	4	BRT_CODE_Bit4	I	1	
	3	BRT_CODE_Bit3	I	1	
	2	BRT_CODE_Bit2	I	1	
	1	BRT_CODE_Bit1	I	1	
	0	BRT_CODE_Bit0	I	1	

1-Wire Data Recognition

Bit detection is based on a logic detection scheme, where the criteria is the relationship between t_{LOW} and t_{HIGH}, as shown in Figure 6. This can be simplified to:

- Low Bit (Logic 0): $t_{LOW} \geq 2 \times t_{HIGH}$
- High Bit (Logic 1): $t_{HIGH} \geq 2 \times t_{LOW}$

The bit detection starts on the falling edge of the data, and ends on the next falling edge. Depending on the relationship between t_{HIGH} and t_{LOW}, a logic 0 or logic 1 is detected. The device only acknowledges the command if the following conditions are met:

- Acknowledge is requested by setting the ACK_EN bit to 1.
- The transmitted device address matches 0x8F.
- All 24 bits are received correctly.

Following a delay of t_{ACK_VAL} from the moment when the last falling edge of the bitstream is detected, an internal pull down switch is turned on to pull the EN pin low for the time t_{ACK_DUR} (512μs max.), signaling the acknowledge condition. During the t_{ACK_VAL} delay the master keeps the line low. After the delay, it should release the line to a high impedance state in order to be able to detect the acknowledge condition. A command is received correctly when reading a logic zero. The EN pin can be used again

by the master when the acknowledge condition ends, after a duration of t_{ACK_DUR}.

Note that during the acknowledge state, SY22121 uses an open drain structure. When the master uses a GPIO with push-pull output stage ensure that the pin is configured as input while waiting for acknowledge, in order to be able to read the low level correctly.

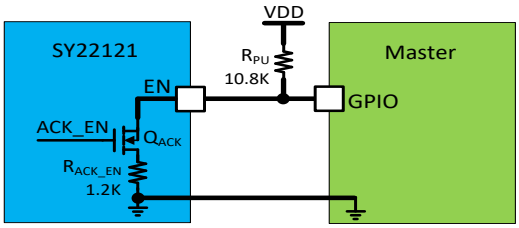


Figure6. EN Action When ACK_EN=1 And ACK Activated

Figure 7 shows the 1-wire interface bit detection timing.

If the input signal high level takes 1/3 or lower of the bit period, a 0 logic is detected. If high level takes 2/3 or more of the bit period, a logic 1 is detected.

1 logic level: High level time t_{H_HB} is 2 times more than low level time t_{L_HB}

0 logic level: Low level time t_{L_LB} is 2 times more than high level time t_{L_LB}

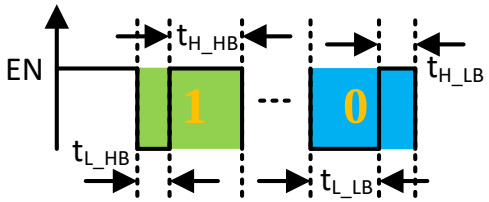


Figure7. 1-Wire Digital Interface Timing Bit Coding

PWM Dimming

If the 1-wire digital interface is not enabled during start up, the PWM control interface is automatically enabled, and the SY22121 receives PWM dimming signals on the PWM pin to control LED brightness.

When using the PWM interface, the EN pin can be connected to logic high. In this case, the PWM pin is used to enable and disable the IC, as follows:

- Pull the PWM high or apply PWM signals at the PWM pin to enable the IC.
- Pull the PWM pin low for more than 25ms (Max.) to force the device in shutdown mode.

The SY22121 can only start up after both the EN and PWM signals are applied. See Figure 8 for PWM dimming interface timing.

If EN is enabled after PWM:

t_{11}: Power On Reset (POR) time delay.

t_{12}: Time delay for the internal bias and reference settling time after POR .

t_{13}: Time of current reference chopping.

t_{14}: EN shutdown delay .

If PWM is enabled before EN:

t_{21}: POR time delay

t_{22}: Time delay for the internal bias and reference settling time after POR .

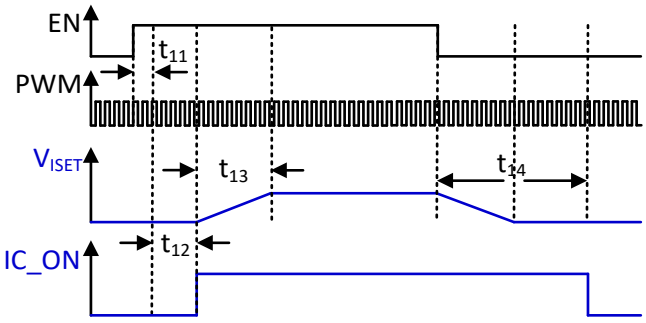
t_{23}: Time of current reference chopping.

t_{24}: PWM shutdown delay.

In PWM operation, LED brightness is controlled using a PWM signal (10kHz-100kHz) applied at the PWM pin. The device accepts a minimum ON pulse width of 500ns. Therefore, a 100:1 dimming ratio can be achieved when using a PWM frequency of 20 kHz(50μs).

The PWM signal is internally filtered using a RC circuit shown in Figure 9 . The component values are R_F=4.26Meg and C_F=55.5pF. The LED current reference charging time constant is $3xR_FxC_F$=710us (0 to 95%). The relation between the LED string current and PWM duty cycle is shown in the following equation (assuming that the EN pin is constantly high):

$$I_{LEDX} = I_{LEDMAX} \times D_{PWM}$$



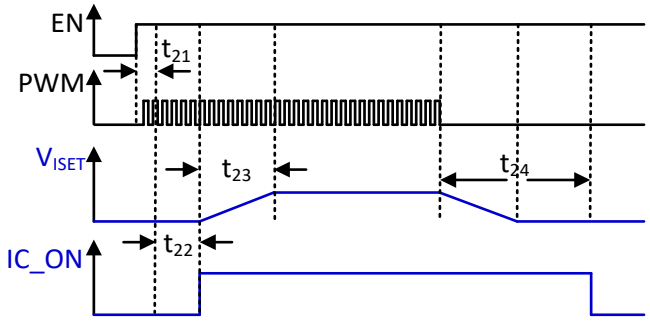


Figure 8. PWM Dimming Interface

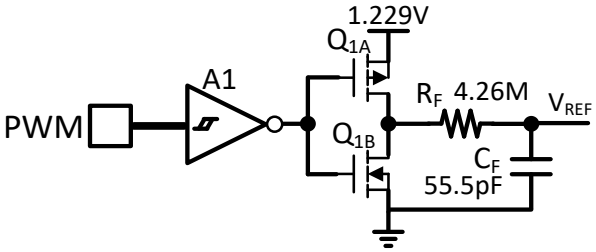


Figure 9. PWM Duty Cycle RC Filtering

Application Information

The following paragraphs describe the selection process for the LED current setting resistor R_{ISET}, input capacitor C_{IN}, output capacitor C_{OUT}, inductor L, and rectifier diode D.

LED Current Setting Resistor R_{ISET}

LED1 and LED2 are the 2-channel LED driver outputs. The sink current of each channel can be programmed with a resistor R_{ISET} between the ISET pin and ground:

$$I_{LED}=I_{SET}(mA)=\frac{1.229V\times 1030}{R_{ISET}(k\Omega)}$$

For R_{ISET} = 63.4kΩ, the LED current is set to 20mA. The maximum sink current of each channel is 30mA. For higher current applications, both channels can be paralleled. The LED current evenly flows through the paralleled channels due to good current matching.

Input Capacitor C_{IN}

The ripple current through input capacitor C_{IN} is calculated as follows:

$$I_{CIN\_RMS}=\frac{V_{IN}\times(V_{OUT}-V_{IN})}{2\sqrt{3}\times L\times F_{SW}\times V_{OUT}}$$

Select an X5R or X7R grade ceramic capacitor with capacitance greater than 1μF and able to handle the ripple current. Place the ceramic capacitor as close as possible to the IN and GND pins. Minimize the loop area formed by C_{IN2} and the IN/GND pins.

Output Capacitor C_{OUT}

Select the output capacitor C_{OUT} to handle the output ripple requirements. This ripple voltage is related to the capacitor's capacitance value and its equivalent series resistance (ESR). For the best performance, use an X5R or better grade low ESR ceramic capacitor. The voltage rating of the output capacitor should be higher than the maximum output voltage. The minimum required

capacitance can be calculated as follows:

$$C_{OUT}=\frac{N\times I_{LED}\times(V_{OUT}-V_{IN})}{F_{SW}\times V_{OUT}\times V_{RIPPLE}}$$

where V_{RIPPLE} is the peak-to-peak output ripple and N is the number of LED strings (the maximum N is 2).

For LED applications, the equivalent resistance of the LED is typically low. The output capacitance should be large enough to attenuate the ripple current through the LED. For most applications, a ceramic capacitor with a value of at least 1μF is sufficient.

Boost Inductor L

Consider the following when choosing this inductor:

1) Choose the inductance to provide a ripple current that is approximately 40% of the maximum output current. The recommended inductance is calculated as:

$$L=\left(\frac{V_{IN}}{V_{OUT}}\right)^2\frac{(V_{OUT}-V_{IN})}{N\times I_{LED}\times F_{SW}\times 40\%}$$

where f_{SW} is the switching frequency, N is the number of LED strings, and I_{LED} is the current of each LED string.

2) The inductor's saturation current rating must be greater than the peak inductor current under full load:

$$I_{SAT,MIN}>\left(\frac{V_{OUT}}{V_{IN}}\right)\times N\times I_{LED}+\left(\frac{V_{IN}}{V_{OUT}}\right)\times\frac{(V_{OUT}-V_{IN})}{2\times F_{SW}\times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement.

The recommended Boost inductance is 4.7uH~10uH.

Rectifier Diode D:
To accommodate the SY22121's high switching speed, choose a Schottky diode with low forward voltage and fast switching speed. The diode's voltage rating must be higher than the SY22121's maximum output voltage, and the diode's average and peak current rating should exceed the SY22121's average output current and peak inductor current.

Fault Protection

Open LED Protection
When any LED string is open, the respective LEDx pin will be pulled to ground, and the Boost output voltage will be increased by the control loop as it tries to regulate this lower LEDx voltage to the target value (165mV typ.). The SY22121 monitors the voltages on the LX pin during each boost switch turn off. When the overvoltage protection (OVP) is triggered, the boost will stop switching and the output voltage will drop. After 100μs, the Boost will resume switching, and the device will check and mark off the abnormal current sink channel. If LX pin OVP is triggered again, the device will check and mark off the other abnormal current sink channel，and the device will latch off.

Short LED Protection
The SY22121 allows one LED diode short in a string. If one LED diode in a string is shorted, the normal string's LEDx pin voltage is regulated to about 165mV, and the abnormal string's LEDx pin voltage will be higher. Normally, with only one diode shorted, the higher LEDx pin voltage does not reach the LEDx OVP threshold $V_{LEDXOVP}$. When more than one LED diode in the same LED string become shorted, the voltage at the LEDx pin driving the string will exceed $V_{LEDXOVP}$ (4.5V typ.), and a short LED fault is triggered. If the short LED fault lasts for more than 6.5ms, the device will mark off and disable that string. When both strings are marked off, the IC will also latch off the boost converter. Cycle input power, the enable signal, or the PWM signal to turn on the disabled string once the fault condition is removed.

Overcurrent Protection
The SY22121 provides a cycle-by-cycle peak current limit. The internal boost MOSFET turns off when the inductor current reaches this current threshold and it remains off until the beginning of the next switching cycle. This protects the device and external components under overload conditions.

Diode and Inductor Short
The SY22121 monitors the peak current to protect against diode and inductor shorts by cycle-by-cycle peak current limit.

Overtemperature Protection
To prevent overheating and permanent damage, the SY22121 shuts down if the junction temperature exceeds 160°C. When the temperature drops below T_{SD}-T_{HYS}, normal operation resumes.

Layout Design

To achieve optimal design, follow these PCB layout considerations:

- Minimize the loop formed by C_{IN1}, Boost inductor L_1, Boost diode D_1, and C_{OUT}.
- To achieve the best thermal and noise performance, maximize the PCB copper area connecting to the GND pin. A ground plane is highly recommended if board space allows.
- Place C_{IN2} close to the IN and GND pins, and minimize the loop area formed by C_{IN2} and GND.
- Minimize the PCB copper area associated with the LX output to reduce the switching noise.
- In order to reduce crosstalk, small signal components must be placed close to the IC and must not be adjacent to the LX net on the PCB layout.
-

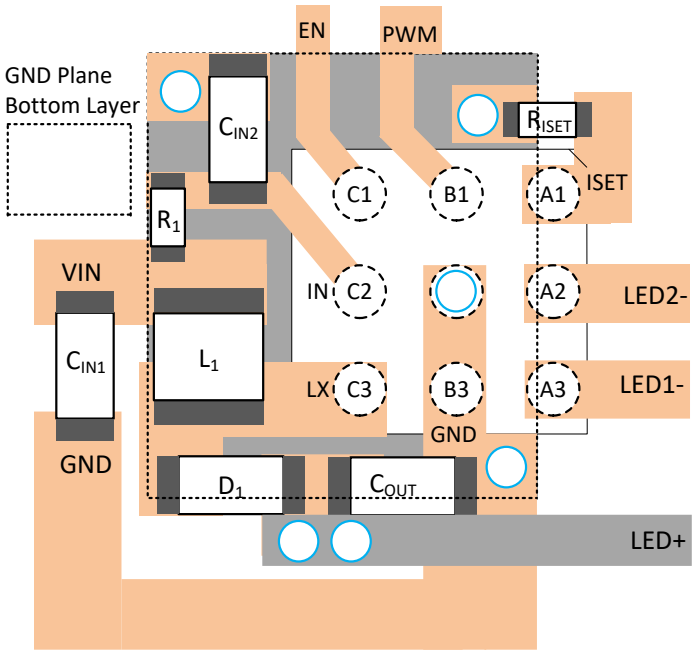
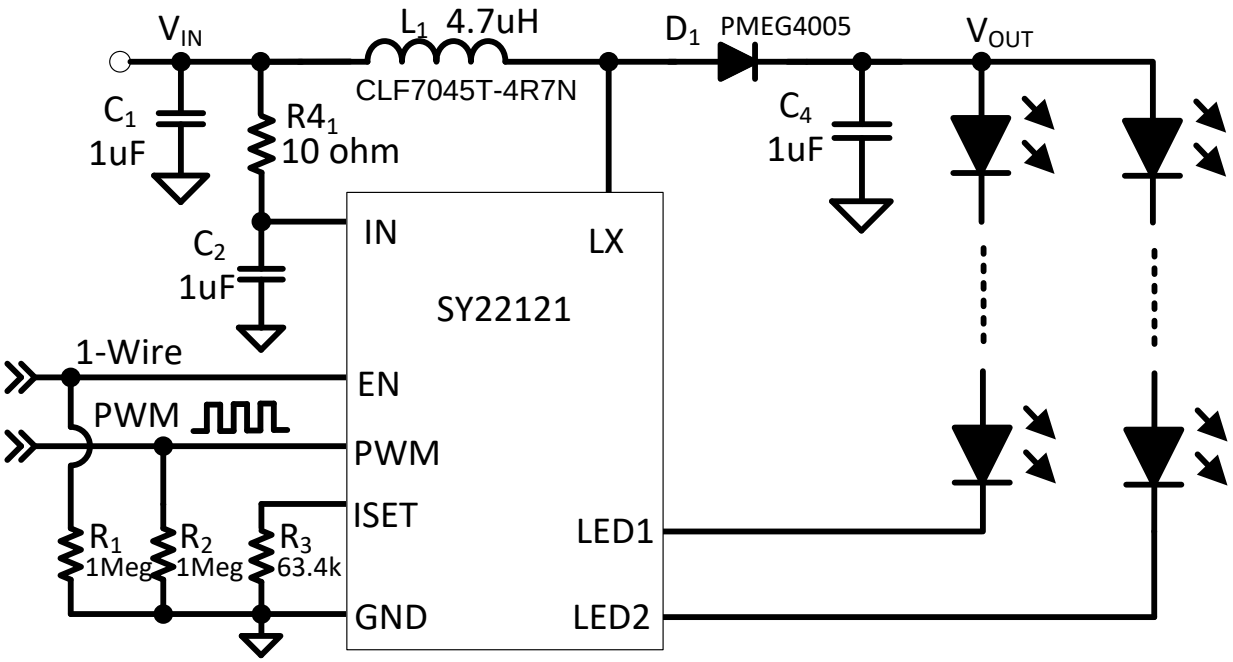


Figure 10. Layout Example

Typical Application Schematic

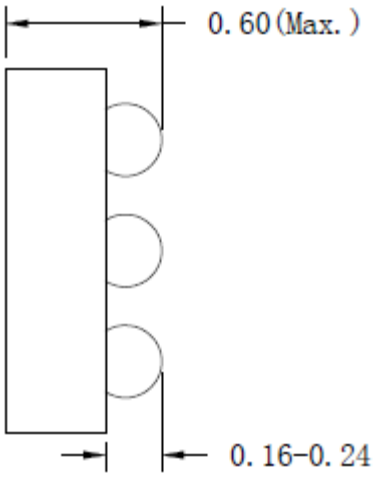
Input Voltage (V)	LED Configuration
2.7-28	2 strings, 20mA per string



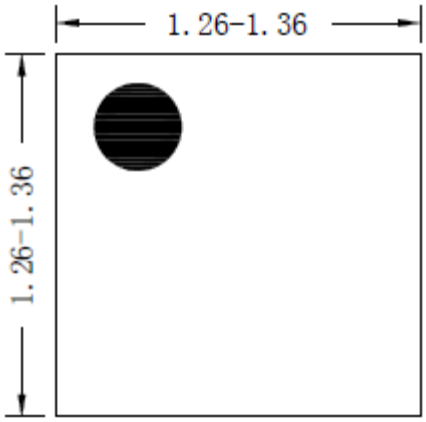
BOM List

Reference Designator	Description	Part Number	Manufacturer
U_1	2-String LED driver	SY22121POC	Silergy
C_1,C_2,C_4	1μF/50V/X5R,0603	C1608X5R1H105K	TDK
L_1	4.7μH/4.1A	CLF7045T-4R7N	TDK
D_1	Schottky Diode 40V/0.5A	PMEG4005	NXP
R_1,R_2	1MΩ, 0603,5%	RC0603JR-071ML	Yageo
R_3	63.4kΩ, 0603,1%	RC0603FR-0763K4L	Yageo
R_4	10Ω, 0603,5%	RC0603JR-0710RL	Yageo

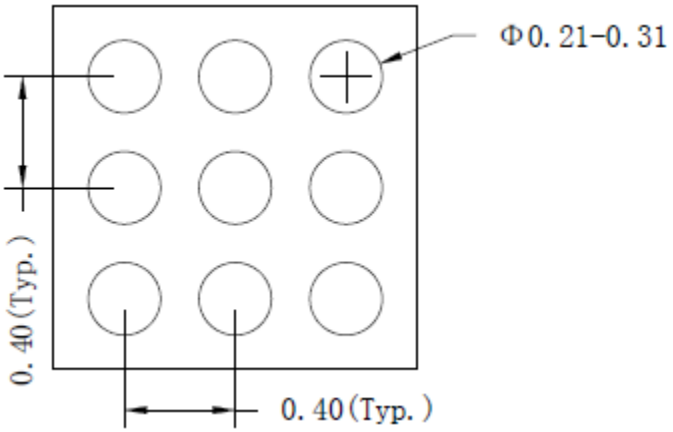
CSP1.31×1.31-9 Package Outline and PCB Layout



Side View



Top view

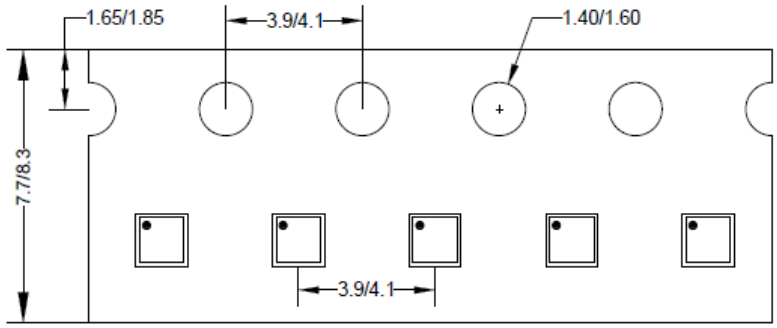


Bottom view

Note: *All dimensions are in millimeters and exclude mold flash and metal burr.*

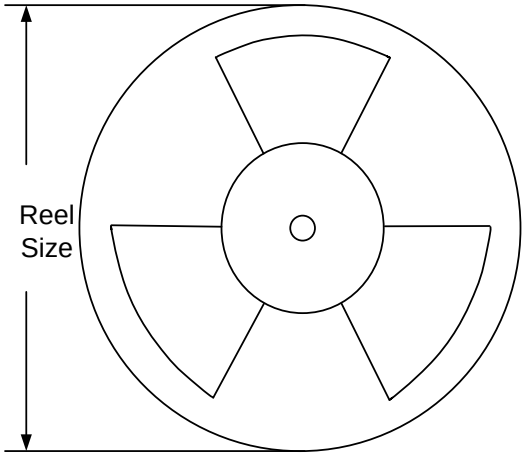
Taping and Reel Specification

CSP1.31×1.31 taping orientation



Feeding direction →

Carrier tape and reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
CSP1.31×1.31	**8**	**4**	**7"**	**280**	**160**	**3000**

Others: NA

Revision History

Date	Revision	Change
Mar.21, 2017	Revision 1.0	Production Release
Mar.21, 2016	Revision 0.9	Initial Release

The revision history provided is for informational purposes only and is believed to be accurate, however, not warrantied. Please make sure that you have the latest revision.

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