Application Note: SY28611S

Dimming Interface Converter Compatible With 0/1~10V Dimming Resistor Dimming And PWM Dimming

General Description

SY28611S is a dimming interface converter whose input signal can be a 0/1~10V dimming signal, resistor, or PWM signal. It recognizes the signal automatically. The final output of SY28611S is a PWM signal which is used to control a dimmable CC regulator or drive an opto-coupler to achieve isolated dimming. The frequency of output PWM signal and the source current to passive 0~10V dimmer/Resistor can be set by external capacitor and resistor.

Ordering Information

SY28611□(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY28611SFAC	SO8	--

Features

- Compatible with 0/1~10V Dimming, Resistor Dimming and PWM Dimming
- Recognize Different Dimming Signal Automatically
- Integrate 60V LDO Module to Simplify External Circuit
- The Source Current for Passive 0~10V Dimmer Can Be Set
- The Frequency of Output Can Be Set
- RoHS Compliant and Halogen Free
- Compact package: SO8

Applications

- LED Dimming

Typical Applications

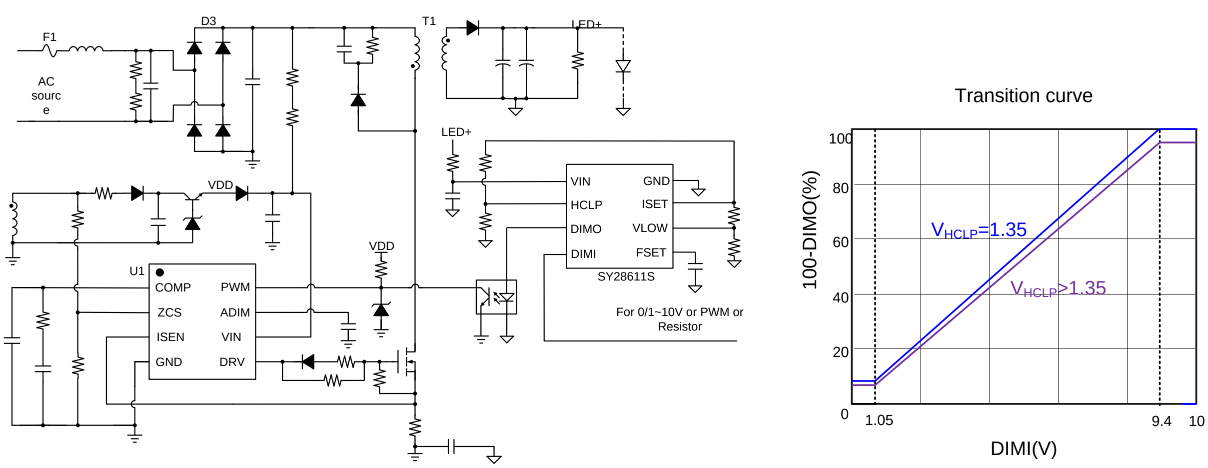
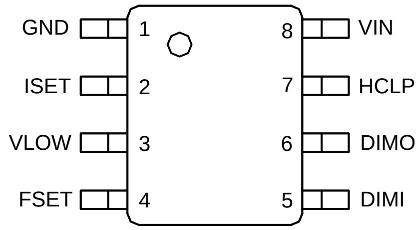


Figure.1 Schematic Diagram

Pinout (top view)



(SO8)

Top Mark: **CGH*xyz*, (**Device code: CGH; ***x=year code, y=week code, z= lot number code*****)**

Pin Name	Pin number	Pin Description
GND	1	Ground pin
ISET	2	Source current setting pin. V_{ISET} is a 2.2V voltage source. This pin is used to set the source current of DIMI pin for passive dimmer. $I_{sr} = \frac{5 \times 2.2}{R_{ISET}}$
VLOW	3	Low clamp set pin. The minimum duty is set by V_{VLOW}, as showed below. $D_{Min} = \frac{0.918 - V_{VLOW}}{3 \cdot V_{HCLP} - V_{VLOW}}$
FSET	4	Dimming frequency setting pin. This pin is used to set the frequency of DIMO pin. $f_{DIM} = \frac{30 \cdot 10^{-6}}{(3 \cdot V_{HCLP} - V_{LOW}) \cdot C_{FSET}}$
DIMI	5	Dimming input pin. Dimming signal is connected to this pin. It maybe is a 0/1~10V analog signal, resistor or a PWM signal.
DIMO	6	Dimming output pin. This pin will output a PWM signal to driver opto-coupler for separation dimming.
HCLP	7	High clamp set pin. The maximum duty is set by V_{HCLP}, as showed below. $D_{MAX} = \frac{8.1 - 2 \times V_{VLOW}}{6 \cdot V_{HCLP} - 2 \cdot V_{VLOW}}$
VIN	8	Power supply pin. This pin provides power supply for IC.

Block Diagram

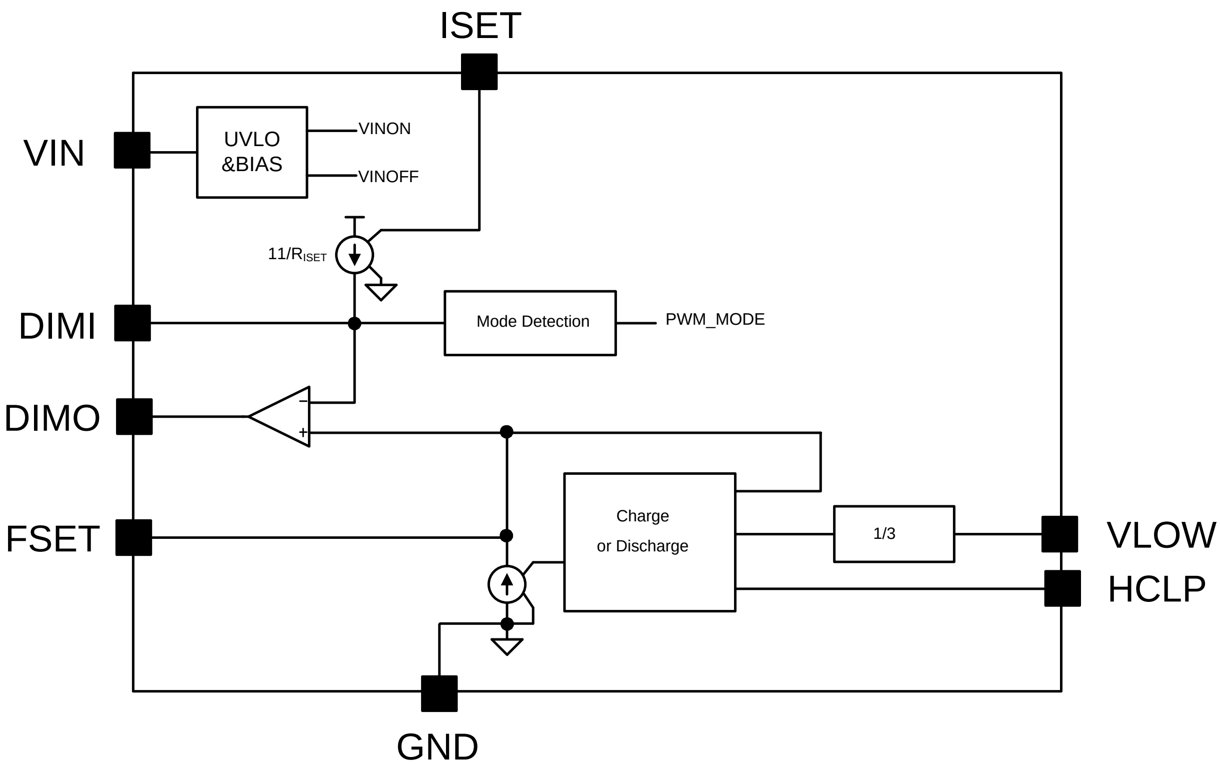


Figure.2 Block Diagram

Absolute Maximum Ratings (Note 1)

VIN -- -0.3V~58V
ISET, FSET, VLOW, HLCLP-- -0.3V~3.6V
DIMI,DIMO -- 0.3V~20V
Power Dissipation, @ TA = 25°C SO8 --- 0.8W
Package Thermal Resistance (Note 2)
SO8,θ_{JA}-- 88°C/W
SO8, θ_{JC}-- 45°C/W
Maximum Junction Temperature -- 125°C
Lead Temperature (Soldering, 10 sec.) --- 260°C
Storage Temperature Range -- -65°C to 150°C

Recommended Operating Conditions

VIN --- V_{VIN_ON} ~55V
Junction Temperature Range -- -40°C to 125°C

Electrical Characteristics

(V_{IN} = 15V, T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Section						
VIN Voltage Range	V_{VIN}		V_{VIN_ON}		55	V
VIN Turn-on Threshold	V_{VIN_ON}		8.3	9.1	10	V
VIN Turn-off Threshold	V_{VIN_OFF}			V_{VIN_ON} -1.4		V
DIMI Section						
MAX DIMI Source Current	I_{SR_MAX}	R_{ISET}=5.5Kohm	1.84	2	2.16	mA
Range of Minimum Dimming Voltage	V_{LOW_RANGE}		0.1		V_{ISET}	V
Ref Voltage of ISET	V_{ISET}		2.1	2.2	2.3	V
Maximum Dimming Voltage	V_{HIGH}		9	9.4	9.8	V
Max Duty of PWM	D_{PWM_MAX}			99(note 3)		%
Min Duty of PWM	$D_{PWM-MIN}$			0		%
PWM ON Voltage Threshold	V_{PWM_ON}		2.3			V
PWM OFF Voltage Threshold	V_{PWM_OFF}				0.8	V
Minimum PWM Frequency	F_{PWM_MIN}		400		10k	Hz
Thermal Section						
Thermal Shut Down Temperature	T_{SD}			145		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

Note 3: If PWM duty is 100% and its amplitude is not 10V, SY28611S could not recognize the current state is PWM mode or not. But if the amplitude of PWM is 10V, the maximum duty is 100%.

Operation

SY28611S is a dimming interface converter whose input signal can be a 0/1~10V dimming signal, resistor, or PWM signal. It recognizes the signal automatically.

When input signal is 0/1~10V dimming signal, It will be converted into a PWM signal to driver opto-coupler or dimmable IC.

When input signal is a resistor, there is a current flowing out from DIMI pin to produce a voltage at the resistor. Then It works as same as 0/1~10V dimming input.

When input signal is a PWM signal, it is converted into a reverse PWM signal.

There are two working modes: Low-clamp is used to clamp the minimum duty cycle. High-clamp is used to clamp the maximum duty cycle. Two working modes can be set by VLOW pin and HCLP pin, respectively.

More detail information is discussed below.

Applications Information

1. Start up

Supposing DIMI is floating.

DIMO follow VIN before VIN reach V_{IN_ON}. After reaching V_{IN_ON}, IC begin to work and DIMO is regulated by DIMI.

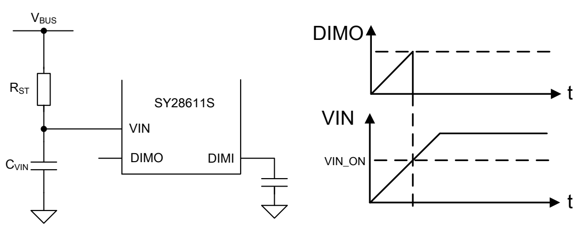


Fig.3 Start up

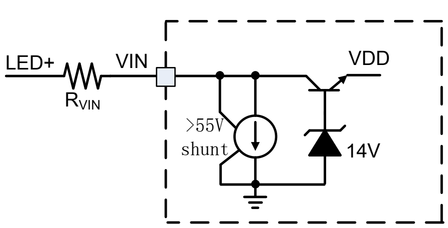


Fig.4 internal LDO

IC integrates a 60V LDO for simplifying peripheral device.

There is a shunt current if VIN voltage is larger than 55V which helps to protect IC when power voltage is high than 55V.

2. Dimming Input

(1) 0/1~10V Dimming

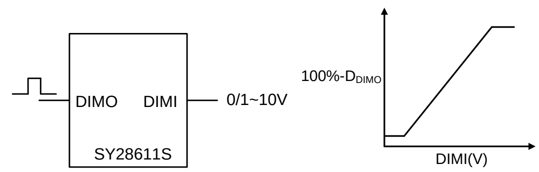


Fig.5 0/1~10V Dimming

If input signal of DIMI pin is 0/1~10V, it is converted into reversed duty signal.

(2) Resistor Dimming

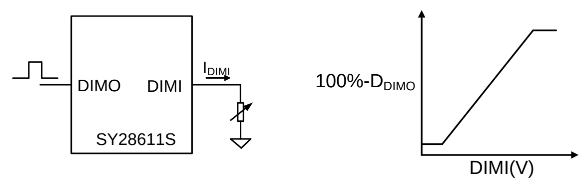


Fig.6 Resistor Dimming

If DIMI is connected with a variable resistor, there is a current flow from DIMI pin to drive the resistor and produce 0~10V signal. Also, the current exists in 0/1~10V dimming application.

(3) PWM Dimming

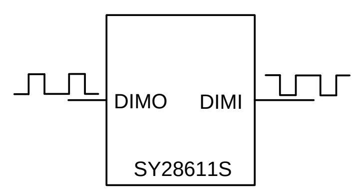


Fig.7 PWM Dimming

If input dimming signal is PWM signal, IC converts it into a reversed PWM signal.

3. Working Mode Setting

(1) High clamp mode

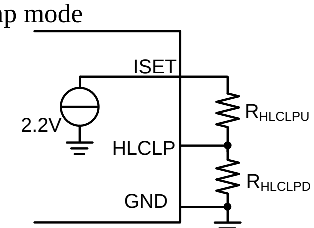


Fig.8 High clamp mode setting

As showed above, High clamp mode is used to set the maximum duty which can regulate the full load current in some special application.

If the voltage of HLCLP pin is larger than 1.35V.The turning point of DIMI is always 9.4V, and the maximum duty can be calculated by the following formula.

$$D_{MAX}=\frac{8.1-2\times V_{VLOW}}{6\cdot V_{HCLP}-2\cdot V_{VLOW}}$$

With different R_{HLCLPU} and R_{HLCLPD}, the maximum duty is set. The design result is showed as bellow.

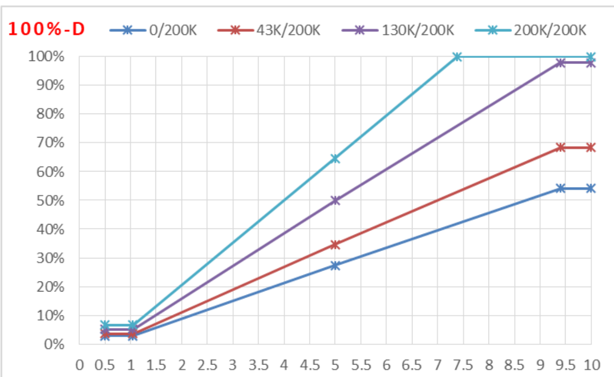


Fig.9 High clamp mode design result

(2) Low Clamp Mode

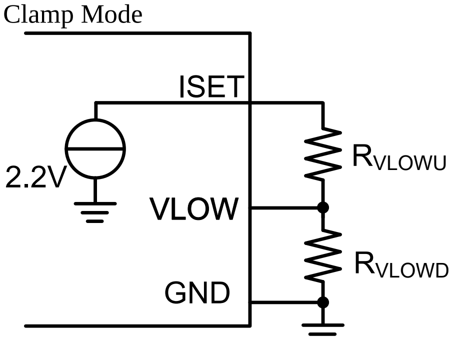


Fig.10 Low clamp mode setting

As showed above, Low clamp mode is used to set the minimum duty which can regulate the light load current in some special application.

If the voltage of VLOW pin is less than 0.918V, The turning point of DIMI is always 1.05V, and the minimum duty can be calculated by the following formula.

$$D_{Min}=\frac{0.918-V_{VLOW}}{3\cdot V_{HCLP}-V_{VLOW}}$$

With different R_{VLOWU} and R_{VLOWD}, the minimum duty is set. The design result is showed as bellow.

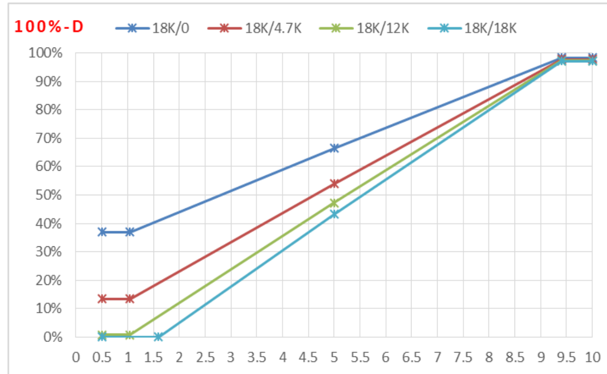


Fig.11 Low clamp mode design result

4. Curve Translation

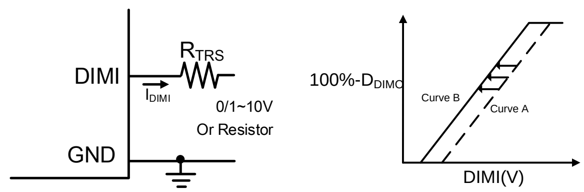


Fig.12 curve translation setting

To translate the converted curve, R_{TRS} is set. With greater R_{TRS}, converted curve is changed from A to B as showed above.

5. DIMI Current Set

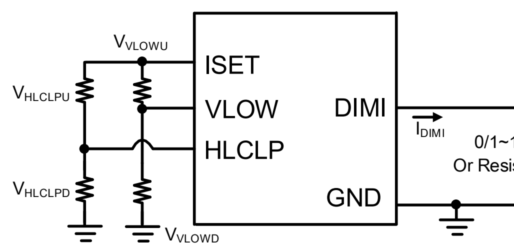


Fig.13 DIMI current setting

If the dimmer is passive device or a resistor, there should be a drive current to power the dimmer.
The current is set by:

$$I_{DIMI}=\frac{5\times 2.2}{R_{ISET}}$$

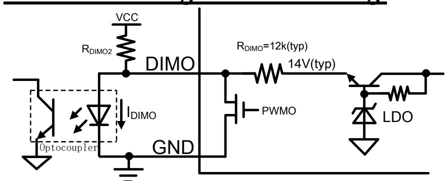
$$R_{ISET}=(R_{HLCLPU}+R_{HLCLPD})//(R_{VLOWU}+R_{VLOWD})$$

6. Frequency Setting

There is a 20uA current charge or discharge FSET capacitor to produce a reference triangle wave.
The frequency is set by:

$$f_{DIM} = \frac{30 \cdot 10^{-6}}{(3 \cdot V_{HCLP} - V_{LOW}) \cdot C_{FSET}}$$

7.DIMO Driving Current Setting.



If the optocoupler is driven by SY28611. The sink current is decided by R_{DIMO} and R_{DIMO2}.

$$I_{DIMO} = \frac{14-1}{R_{DIMO}} + \frac{VCC-1}{R_{DIMO2}}$$

Some examples are showed below.

VCC (V)	20	20	30
R_{DIMO2} (ohm)	NC	20k	20k
I_{DIMO} (mA)	1.08	2.03	2.53

8. Recommended Peripheral Circuit

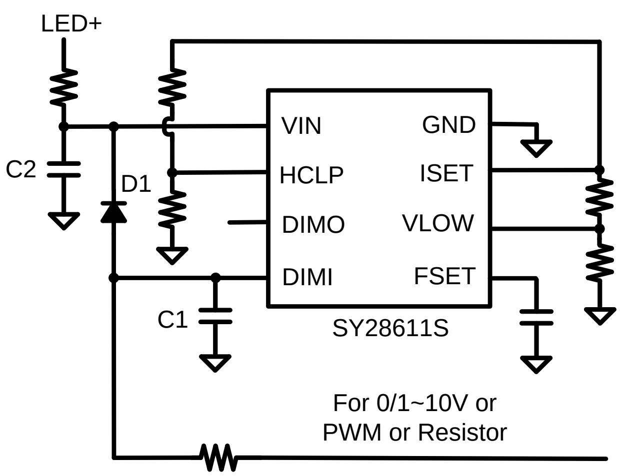


Fig.14 Recommended Circuit

C1 is the DIMI pin capacitor and 1nF is recommended. C2 is the VCC capacitor and 1nF is recommended. D1 is the DIMI pin protecting Diode and usually 1N4148 is chosen.

Design Example

A design example of typical application is shown below step by step.

#1. Identify design specification

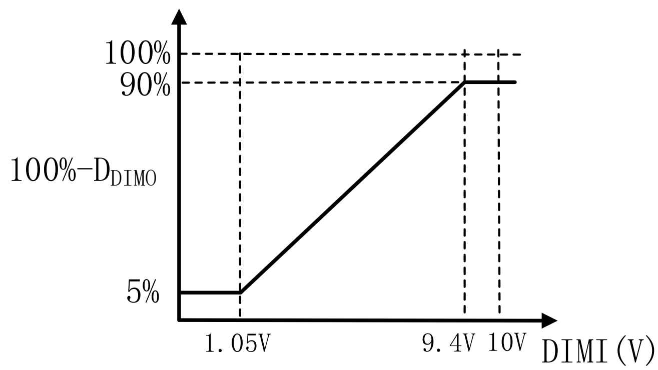


Fig.15 Target Curve

Target parameter			
I_{DIMI}	500uA	Fs	1kHz
V_{LCLP}	1.05	D_{MIN}	5%
V_{HCLP}	9.4	D_{MAX}	90%

(a) VLOW calculation:

Set R_{VLOWD} =24K;

Because,

$$D_{MAX}=\frac{8.1-2\times V_{VLOW}}{6\cdot V_{HCLP}-2\cdot V_{VLOW}};\quad and\quad D_{Min}=\frac{0.918-V_{VLOW}}{3\cdot V_{HCLP}-V_{VLOW}}$$

So,

$$\frac{D_{Min}}{D_{Max}}=\frac{2\times\left(0.918-V_{VLOW}\right)}{8.1-2\times V_{VLOW}}\rightarrow\frac{5\%}{90\%}=\frac{2\times\left(0.918-V_{VLOW}\right)}{8.1-2\times V_{VLOW}}$$

We can get that: V_{VLOW} = 0.7337V;

$$R_{VLOWU}=\frac{(2.2-V_{VLOW})\times R_{VLOWD}}{V_{VLOW}}$$

We can get that: R_{VLOWU} =47.964K

So R_{VLOWU} =51K

(b). HCLAMP calculation

Due to, V_{VLOW} = 0.7337V;

$$90\% = \frac{8.1 - 2\times 0.7337}{6\cdot V_{HCLP} - 2\times 0.7337}$$

So, V_{HCLP} = 1.4728V

$$\frac{2.2}{\mathrm{R}_{HCLPU} + \mathrm{R}_{HCLPD}} = \frac{V_{HCLP}}{\mathrm{R}_{HCLPD}} \quad \rightarrow \quad \mathrm{R}_{HCLPU} = \frac{(2.2 - V_{HCLP})\times \mathrm{R}_{HCLPD}}{V_{HCLP}}$$

$$\mathrm{R}_{HCLPU} = \frac{(2.2 - V_{HCLP})\times \mathrm{R}_{HCLPD}}{V_{HCLP}} \quad \rightarrow \quad \mathrm{R}_{HCLPU} = 0.49375\times \mathrm{R}_{HCLPD}$$

Because,

$$R_{ISET} = (R_{HLCLPU} + R_{HLCLPD}) // (R_{VLOWU} + R_{VLOWD})$$

$$R_{ISET} = \frac{2.2V}{(\frac{500uA}{5} - 14.23uA)} = 25.65K$$

$$R_{HLCLPU} + R_{HLCLPD} = \frac{R_{ISEN}\times (R_{VLOWU} + R_{VLOWD})}{(R_{VLOWU} + R_{VLOWD}) - R_{ISEN}}$$

$$R_{HLCLPU} + R_{HLCLPD} = \frac{25.65K\times (48K + 24K)}{(48K + 24K) - 25.65K} \quad \rightarrow \quad R_{HLCLPU} + R_{HLCLPD} = 39.8K$$

So,

$$R_{HCLPD} = 26.6K \approx 27K$$
$$R_{HCLPU} = 13.1K \approx 13K$$

(e). Fs calculation

$$f_{DIM} = \frac{30\cdot 10^{-6}}{(3\cdot V_{HCLP} - V_{LOW})\cdot C_{FSET}}$$

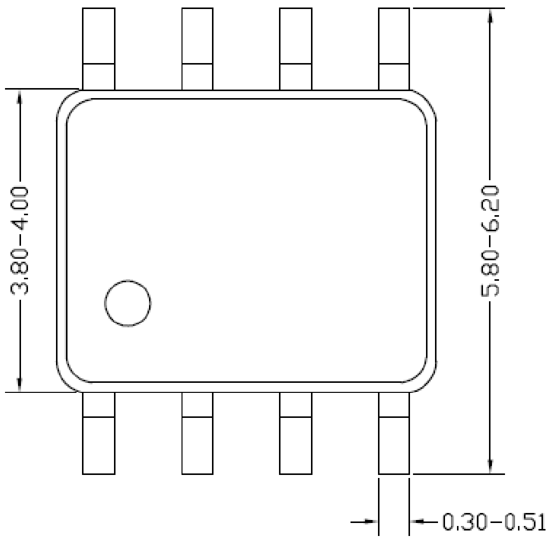
So,

$$C_{FSET} = 8.14nF \approx 8.2nF$$

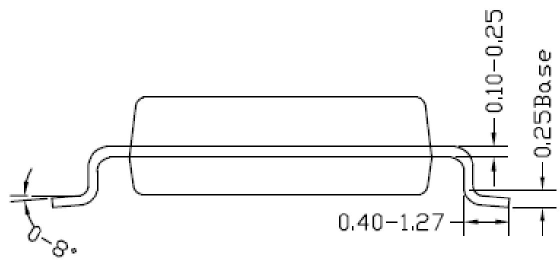
(f). The design Result

Conditions			
R_{HLCLPU}	13k ohm	R_{HLCLPD}	27k ohm
R_{VLOWU}	51k ohm	R_{VLOWD}	24k ohm
R_{TRS}	0.01k ohm	C_{FSET}	8.2nF

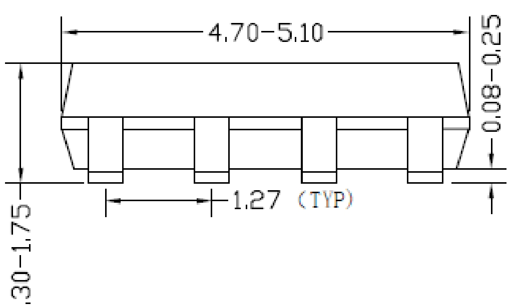
SO8 Package outline & PCB layout design



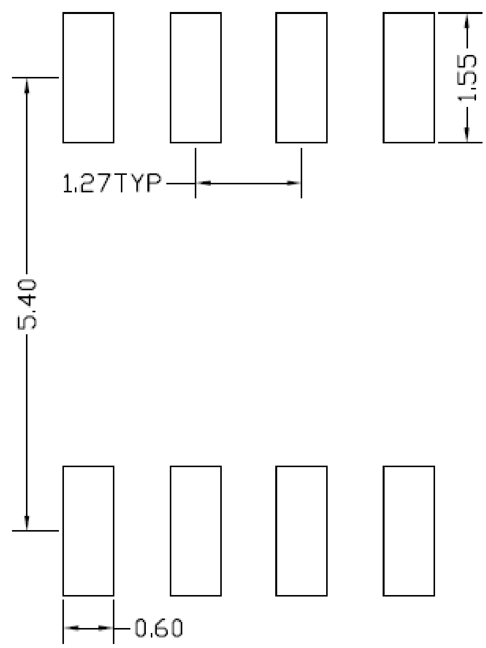
Top view



Side view



Front view

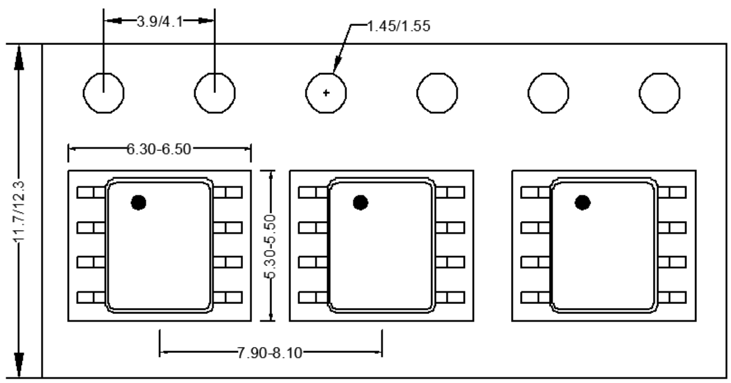


Recommended Pad Layout (Reference only)

Notes: All dimension in millimeter and exclude mold flash & metal burr.

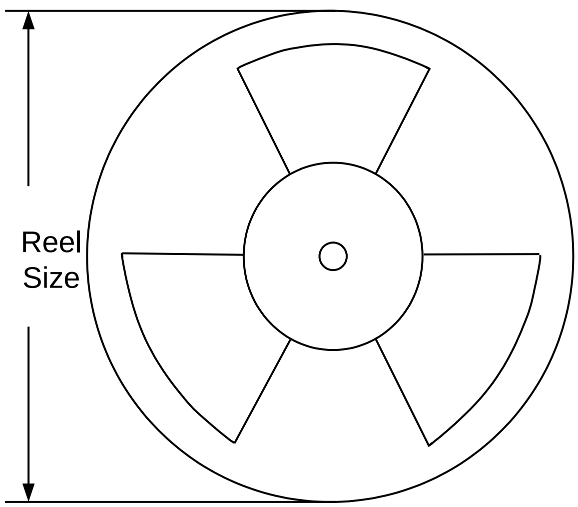
Taping & Reel Specification

1. Taping orientation for packages（SO8）



Feeding direction →

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SO8	12	8	13"	400	400	2500

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
December 30, 2019	Revision 0.9	Initial Release

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