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Buck converter for SSL applications

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Document information

Info	Content
Keywords	Buck, down, converter, driver, topology, AC/DC, DC/DC, SMPS, LED
Abstract	This document describes how to design a buck converter that can be used to drive a LED string. It also illustrates the method of calculating components in the Boundary Conduction Mode (BCM).

Revision history

Rev	Date	Description
v.2	20110623	second issue Modifications: • text and formulas updated • template updated to latest version • all illustrations upgraded to new AQL standard
v.1	20091014	first issue.

1. Introduction

The buck converter is one of the most common and often used Switch Mode Power Supply (SMPS) topologies. This topology is also known as a down converter because of its main feature - the output voltage is always lower than the input voltage. A buck converter can be remarkably efficient (up to 95 % for integrated circuits) and self-regulating. This makes it useful for tasks such as converting a 12 V to 24 V typical battery voltage in a laptop, down to the few volts needed by the processor. This topology can be used not only to convert voltage, but is also suitable to act as a current source, depending on the control method. A number of Silergy LED drivers can operate in buck mode.

2. Scope

2.1 Scope

This application note discusses the general principles and considerations to be addressed when designing a buck converter and especially a buck converter for LEDs in Boundary Conduction Mode with valley detect. There is a separate chapter for losses and key component calculations. This application note can be used when designing a buck converter using several of Silergys LED driver ICs, such as SSL1523, SSL2101, SSL2102, SSL2108, SSL2109 and UBA 3070. Dimmability and mains dimmability are not discussed within this application note, as this is specific for each IC solution.

2.2 General philosophy of the application note

The layout of this document is constructed to enable each chapter on a related subject to be read with a minimum of cross-references to other documents or data sheets. This leads to repetition as some of the information within this application note is also available in other, more dedicated application notes. In most cases, typical values are given to enhance readability.

- Section 3 discusses the theory of operation. It demonstrates how voltages and currents flow during one converter cycle. It also gives a short overview of the trade-off between CCM and BCM/DCM modes.
- Section 4 provides information on how to design key components, such as the inductor value. It describes the resultant calculation of peak current with BCM, when valley detection is used.
- Section 5 shows some power calculations, to give the designer an insight into the loss mechanisms in the converter, and how choices affect efficiency.
- Section 6 briefly covers LED current tolerance and stability.

2.3 Related documents and tools.

Further information regarding design tools and the driver ICs mentioned in this document can be either found on the product page for the specific IC (Internet link), or are available through the local sales office.

3. Theory of operation

The operation of the buck converter is relatively simple, comprising an inductor and two switches that control the inductor input current. It alternates between connecting the inductor to source voltage to store energy in the inductor, and discharging the inductor into the load.

Figure 1 shows a simplified application diagram of a buck converter connected to a voltage supply and a load. For a basic understanding of the application, V_I and V_o can be regarded as DC. In a practical application, a MOSFET or bipolar transistor replaces switch S1, and a diode replaces switch S2.

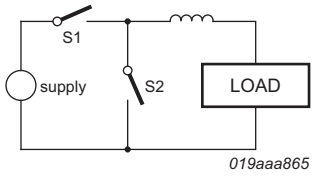


Fig 1. Basic configuration circuit

The circuit is defined by the state of the switches. With two switches there are four modes, but not all of them are applicable. Modes 1 and 2 are the most important and nearly always present, while mode 3 is only present in Discontinuous Conduction Mode (DCM). Mode 4 must be prevented, since this would short circuit the supply. The state of the switches in modes 1 to 3 is displayed in Table 1.

Table 1. Possible modes of operation

Mode	S1	S2	Duration
1	On	Off	$\delta 1 \times t_{total}$
2	Off	On	$\delta 2 \times t_{total}$
3	Off	Off	$\delta 3 \times t_{total}$

The operation of the buck-back converter is briefly explained on the next page. The figures show the equivalent circuit diagrams for the first two modes. Simplified waveforms are also shown for one complete switching cycle.

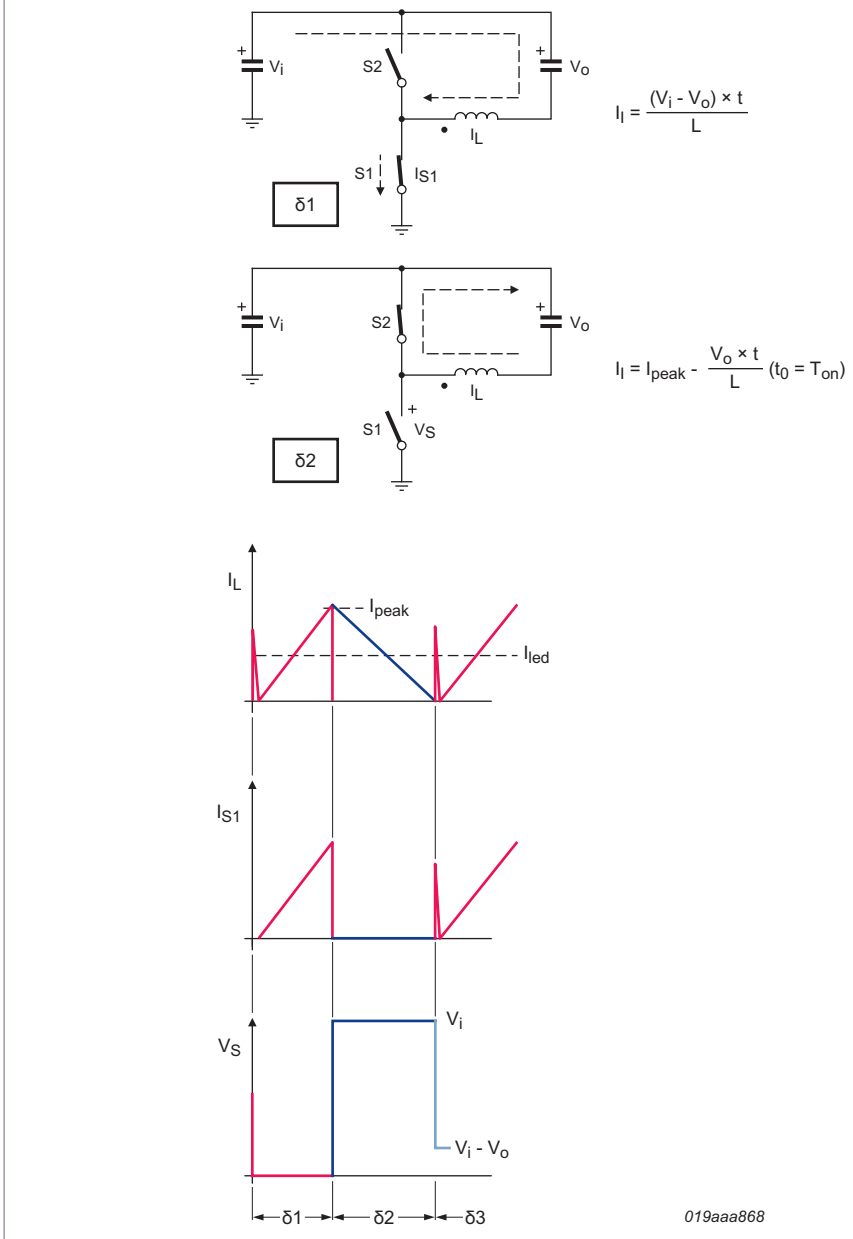


Fig 2. Buck waveforms - discontinuous conduction mode

During the time $\delta 1 \times t_{total}$ (Mode 1), switch S1 is switched on and a current starts to flow through inductor L. At the moment switch S1 is switched off, the secondary switch S2 is closed and a current flows towards the output. During the conduction time of switch S2, the energy in the inductor is reduced. The time interval $\delta 3$ is entered when the current through switch S2 has decreased to zero. This mode of operation is referred to as the Discontinuous Conduction Mode (DCM). The border between DCM and Continuous Conduction Mode (CCM) is reached when the time $\delta 3 \times t_{total}$ has become zero. This is referred to as the Boundary Conduction Mode (BCM). The CCM mode is present when the inductor current does not reach zero throughout the cycle.

Switch S2 is often replaced by a diode. It must be ensured that Mode 3 is entered only when the current through the inductor is zero. If both switches open when there is still current running through the inductor, the current will try and seek another path, and a very high voltage peak will be the result. The peak might damage the switches or the inductor, but this can be prevented by using a suitable diode for S2.

Both Continuous mode and Discontinuous mode buck solutions are common, and each solution has the following specific advantages and disadvantages:

- The CCM converter has less input and output current ripple than the discontinuous mode version, so it requires less additional filtering.
- The CCM converter has lower core losses because less of the BH-curve is utilized. It must, however, have an inductor value inverse to the current ripple, which results in a much bigger core and more windings. This counters the lower core losses, and gives more wire losses.
- The CCM converter cannot be regulated to low values and the control margin is determined by the current ripple.
- The DCM converter has no hard current switching when S1 starts to conduct. As a result, only a switching method that is optimized for low switch-off losses can be used.
- The DCM converter makes full use of magnetic energy storage which allows it to work with a smaller inductor.

The above list illustrates that discontinuous mode is the most effective solution for small form factor dimmable SSL solutions.

A BCM converter offers even more advantages because the discontinuous mode has a dead time during which the inductor is not used. It offers the smallest size and the lowest switching losses, and full dimmability. The ripple current at both the input and output is, however, higher and so more buffering and filtering is needed to reduce this and to reach mains conducted emission standards such as FCC15 and IEC55015.

4. Key components design procedure

This chapter offers guidance when designing a Boundary Conduction Mode buck converter for SSL applications:

4.1 Output current versus peak current

A typical minimal buck application circuit driving one string of LEDs is shown in Figure 3. The starting parameters when designing such a circuit are the required LED current and the LED voltage. Assuming the converter operates in BCM, the relationship between output current and inductor peak current is straightforward:

$$I_{peak} = 2 \times I_{led} \quad (1)$$

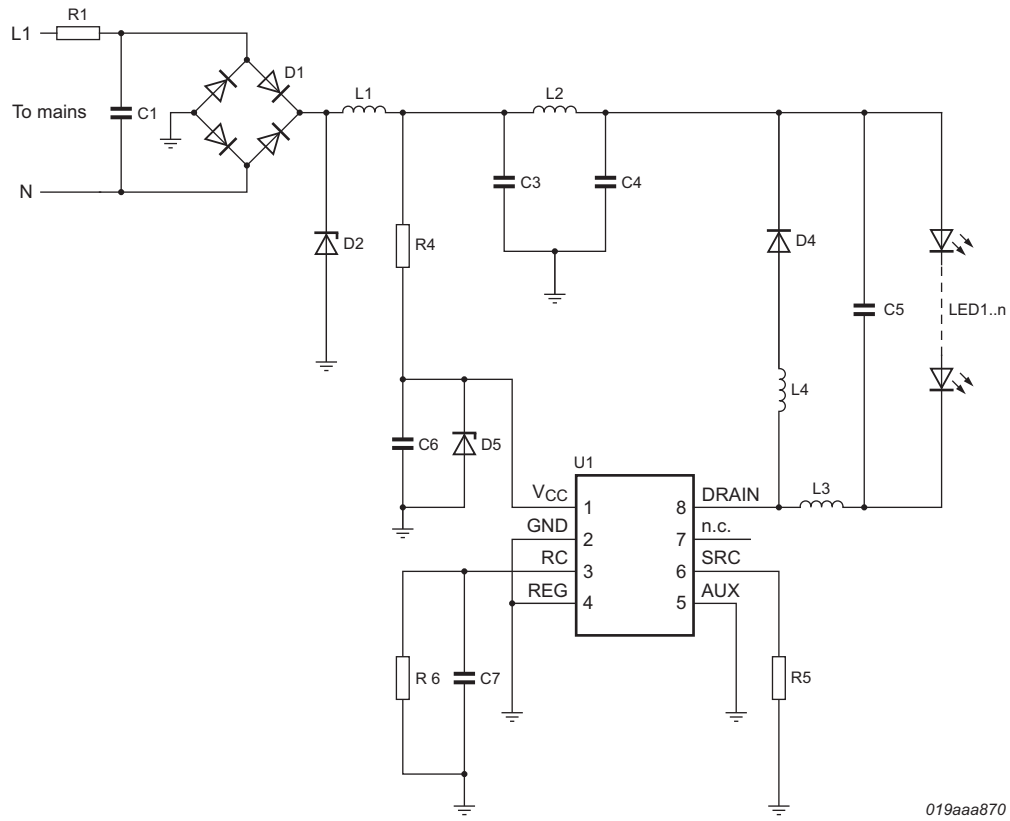


Fig 3. Typical buck application

Remark: The LED assembly in Figure 3 is connected above L3. This is to prevent the LEDs having a voltage variation equal to the drain voltage. Because the LED assembly is large with extended wires and a heatsink, it has substantial capacitive coupling to its surroundings. This capacitive coupling has a detrimental effect on efficiency and EMC.

The same inductor (L3 in Figure 3) is used for charging and discharging energy, resulting in a direct dependency between $\delta 1$ and $\delta 2$, the LED forward voltage and the input voltage.

$$\frac{(V_i - V_o)}{V_o} = \frac{\delta 2}{\delta 1} = \frac{t_2}{t_1} \quad (2)$$

4.2 Inductor dimensioning

Since there is a direct relationship between the sum of t1 and t2 and converter frequency, the inductor value can easily be derived when choosing the converter frequency:

$$f = \frac{1}{T} \quad (3)$$

$$\delta_1 + \delta_2 = 1 \quad (4)$$

$$I_{peak} = \delta_1 \times \frac{V_i - V_o}{f \times L_3} \quad (5)$$

Combining 1 to 5 results in Equation 6:

$$L_3 = \frac{1}{2 \times I_{led} \times f} \times \frac{V_0^2 - (V_i \times V_o)}{V_i} \quad (6)$$

Example:

When f = 100 kHz, I_{led} = 700 mA, V_I = 200 V and V_O = 100 V, then δ1 = 50 %, I_{peak} = 1.4 A and L_3 = 357 μH. Applying this to formula 2, t1 = 5 μs, t2 = 5 μs.

and:

f = 100 kHz, I_{led} = 700 mA, V_I = 200 V, V_O = 10 V. I_{peak} = 1.4 A, δ1 = 5 %, δ2 = 95 %, L_3 = 67.8 μH, t1 = 0.5 μs, t2 = 9.5 μs

4.3 Valley detect

The next converter cycle starts after t2 has ended and the converter current has reached zero. As a result, the switch reactivates with a substantial voltage over it. There is a capacitance over the supply and the switch, which comprises several components:

- The parallel capacitance of the inductor
- The reverse charge of the freewheel diode
- The drain-gate capacitance of the switch

When discharging this capacitance, the energy stored is dissipated in the switch (P_{sw}).

$$P_{sw} = \frac{1}{2} \times C_p \times V_{sw1}^2 \times f \quad (7)$$

Example: If f = 100 kHz, V_{sw1} = 200 V and C_p = 100 pF, then P_{sw} = 200 mW.

As a result, the switch heats up and the efficiency is decreased. To counter this, Silergy converters incorporate a unique feature referred to as valley detection. This is special circuitry that senses when the voltage on the drain of the switch has reached its lowest value. Consequently, the next cycle is started and the switching losses are reduced significantly.

There is, however, another effect, a time (t3) is introduced during which there is little current running in the inductor. t3 constitutes half the period of the resonant frequency:

$$t_{valley} = \pi \times \sqrt{L_p \times C_p} \quad (8)$$

Example: If L_p = L3 = 357 μH and C_p = 100 pF, then t_{valley} = 0.594 μs

To be most effective, two conditions must be met:

- The excitation voltage (V_o) must be close to half the input voltage
- The L_pC_p combination must be under damped

$$V_o = \frac{1}{2} \times V_i \quad \text{and} \quad R_{ser}^2 \times C_p^2 - 4 \times L_p \times C_p \ll 0 \quad (9)$$

R_{ser} is the serial damping resistor within the L_p C_p circuit, and consists of coil resistance and magnetic losses.

Example: If V_i = 200 V, V_o= 100 V which is 0.5 V_I then the first condition is met.

If R_{ser} = 1 Ω, C_p = 100 pF, L_p = 357 μH, then the resultant damping factor is -1.43×10^{-13}. This is smaller than 0, and so the second condition is also met.

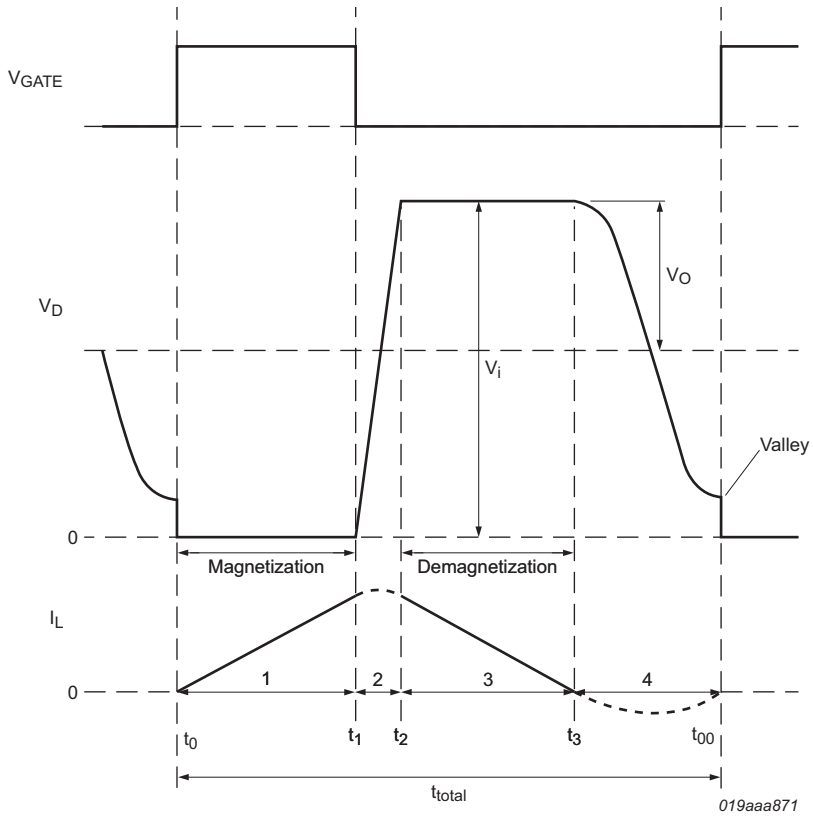


Fig 4. Valley detect waveforms

However, in order to reach the same LED current, the peak value must be adjusted, and this in turn will alter the converter frequency. The average current towards the output is given in Equation 10:

$$I_{led} = I_{peak} \times \frac{t_1 + t_2}{2 \times (t_1 + t_2 + t_3)} \quad (10)$$

$$\varphi = \frac{V_o}{V_i - V_o} \quad (11)$$

$$t_2 = \frac{I_{peak} \times L_3}{V_o} \quad (12)$$

$$t_1 = \frac{I_{peak} \times L_3}{V_i - V_o} \quad (13)$$

Combining Equation 10, Equation 11, Equation 12 and Equation 13 results in Equation 14:

$$2 \times I_{led} = \frac{\frac{I_{peak}^2 \times L_3}{V_o} \times (\varphi + 1)}{\frac{I_{peak} \times L_3}{V_o} \times (\varphi + 1) + t_3} \quad (14)$$

When Equation 14 is expounded, it gives Equation 15

$$) = L_3 \times (\varphi + 1) \times I_{peak}^2 - 2 \times I_{led} \times (\varphi + 1) \times L_3 \times I_{peak} - 2 \times I_{led} \times t_3 \times V_{} \quad (15)$$

This 2nd order function can be solved using the ABC formula:

$$a = L_3 \times (\varphi + 1) \quad (16)$$

$$b = -2 \times L_3 \times (\varphi + 1) \times I_{led} \quad (17)$$

$$c = -2 \times t_3 \times V_o \times I_{led} \quad (18)$$

$$I_{peak} = \frac{-b \pm \sqrt{b^2 - 4 \times a \times c}}{2 \times a} \quad (19)$$

Example: When φ = 1, I_{led} = 700 mA, t3 = 0.594 µs and V_o = 100 V, then a = 0.714 × 10^{-3}; b = –1 × 10^{-3} and c = –83.1 x 10^{-6} with the result that I_{peak} = 1.48 A.

Applying these values in the preceding formulas, results in t1 = 5.28 µs, t2 = 5.28 µs, t3 = 0.594 µs, f' = 89.6 kHz.

4.4 Peak current limit

In the example schematic (see Figure 3), resistor R5 limits the peak current. When the voltage level over this resistor reaches a threshold, the cycle will stop and the switch will stop conducting. This threshold can be used to control peak current. Using peak current control, the LED current is half the peak current in BCM mode. The tolerance on this detection is proportional to the tolerance on the LED current. The value of R5 is calculated using the threshold level V_{ocp} in Equation 20.

$$R_5 = \frac{V_{ocp}}{I_{peak}} \tag{20}$$

Example: If I_{peak} = 1.48 A and V_{ocp} = 0.52 V then R5 = 0.35 Ω.

4.5 Ripple current calculation

Capacitor C5 filters the current through the LEDs so that it will approach the average current through the inductor. The remaining variation is known as ripple and can be expressed as a percentage of the average current. If the current waveform is symmetrical, which is the case for buck converters, the ripple current is also symmetrical. Equation 21 provides an approximation of the ripple current.

$$C_5 = \frac{1}{2 \times \pi} \times \frac{1}{f \times Ripple_{\%} \times R_{dyn}} \tag{21}$$

In Equation 21, R_{dyn} is the differential resistance of the LED string at the average rated current. This value is derived by taking the tangent of the UI graph as provided in the data sheet for the LED. This must not be confused with the division between voltage and current at the point of operation of the LED.

Example: Ten LED's are used in series and are driven at 100 mA. Each LED has a dynamic resistance of 1 Ω, resulting in a total dynamic resistance of 10 Ω. With a ripple of 5 % and a frequency of 100 kHz, C5 will be 3.18 μF. Use 3.3 μF.

or, alternatively,

One LED is used at 1 A. It has a dynamic resistance of 0.1 Ω. With a ripple of 1% and a frequency of 100 kHz, C5 will be 1.6 mF.

The value calculated using this formula is intended to filter ripple current caused by converter operation. It is not intended to filter current variation due to input voltage fluctuations. The input voltage ripple often has an amplitude that does not allow the linear approximation as used in Equation 21, especially when rectifying and buffering 50 Hz or 60 Hz mains voltage. For mains buffer calculations, use Equation 22.

$$C3 + C4 = \frac{2 \times P_{tot} \times t_{dis}}{V_{mainspeak}^{\ 2} - V_{buff(min)}^{\ 2}} \tag{22}$$

where:

P_{tot} = P_{in} + IC losses. C3 + C4 is equal to the input buffer capacity

4.6 Inductor design parameters

In buck converter designs, the importance of the main inductor (L3) quality is often underestimated. To achieve a highly efficient solution, not only the inductance value, but also the resistive losses, saturation current, proximity losses, core losses, parasitic capacitance and stray magnetic fields are important. Not understanding the functionality and implementing without an optimized component, will result in either, inferior performance or an impractical design. Chapters Section 4.6.1 to Section 4.6.4 offer some guidelines concerning this.

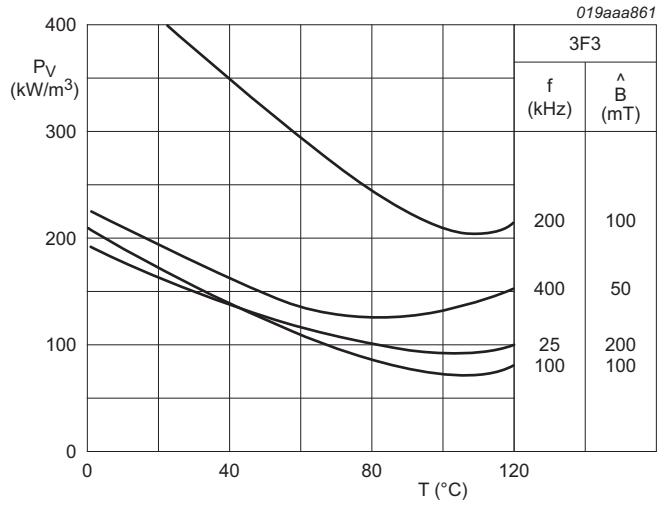


Fig 5. 3F3 specific power loss for several temperature/flux density combinations

Manufacturers generally have their own code for core material and for applications between 50 kHz and 200 kHz, 3F3 (Ferroxcube), N87 (Epcos) or TP4 (TDG), are recommended. Select the material that has the optimal lowest loss at working temperature. A core material not suitable for the effective frequency of the converter will give high core losses.

Table 2. Ferrite Core Comparative Geometry Considerations

Aspect	Pot Core; RM Core	Double slab core	E core	Ec; ETD Cores	PQ Core	EP Core	Toroid
core costs	high	high	low	medium	high	medium	very low
bobbin costs	low	low	low	medium	high	high	none
winding costs	low	low	low	low	low	low	high
winding flexibility	good	good	excellent	excellent	good	good	fair
assembly	simple	simple	simple	medium	simple	simple	None
mounting flexibility	good	Good	good	fair	fair	good	poor
heat dissipation	poor	good	excellent	good	good	poor	good
shielding	excellent	good	poor	poor	fair	excellent	good

4.6.1 Core type selection

Core geometry depends on several factors such as cost, flexibility, shielding and utilization factors. A core can have an inner core that may result in a round or square winding. The stray inductance can vary with core shape. Core size is determined by the maximum stored energy in the inductor together with the required air gap. A core with a large air gap can store more energy than a core with a small air gap. In practice, for discontinuous mode converters, an optimum design is reached when core losses and winding losses (proximity and skin losses) are balanced. A compromise has to be made between high storable energy levels, low leakage inductance and small tolerances on the inductance. Using Equation 23, the maximum energy stored in the inductor can be calculated.

$$E = \frac{1}{2} \times L_3 \times I_p^{\,2} \tag{23}$$

Example: If L_3 = 357 μH and I_p = 1.48 A, then E = 0.39 x 10^{-3} J.

Table 3 shows the RM core types that can be applied:

Table 3. Core selector

Core type	Material	Ag (μM)	Ue (N/A^2)	L_e (mm)	Al (nH)	Ae (mm^2)
RM4	3H3-A100	160	154	20.9	100	11.0
RM4/I	3F3-A160	110	215	23.3	160	13.8
RM5	3H3-A250	110	201	21.2	250	21.2
RM5/I	3F3-A250	130	186	23.1	250	24.8
RM6S	3H3-A315	120	221	26.8	315	31.4
RM7/I	3F3-A250	240	135	30.0	250	44.1
RM8	3H3-A630	90	342	35.6	630	52.0
RM10/I	3H3-A1000	110	367	44.6	1000	96.6

4.6.2 Calculate windings

A_l is often specified in the data sheet of the core material. It relates to the inductive value of a single turn on the selected core. Using this figure, and knowing the inductance, the calculation of winding number is quite straightforward, as shown in Equation 24:

$$N_{L3} = \sqrt{\frac{L_3}{A_l}} \tag{24}$$

Example: For core type RM8 3H3-A630 - if A_l = 630 nH and L_3 = 357 μH then N_{L3} = 24

A practical value for N_{L3} can be obtained by approximating the calculated value to its nearest integer. As a double check, the maximum magnetic B-field is determined by the magnetic material. Note that the peak value of B-field reached during operation, has a substantial impact on core losses. Core losses are discussed in Section 5.5.3, but as a general guideline, the B-field in the magnetic material should remain below the specified B_{max} of the material. The B-field can be estimated using Equation 25:

$$B_{max} = u_e \times \frac{N_{L3} \times I_p}{L_e} \tag{25}$$

Example: For core type RM8 3H3-A630 - if N_{L3} = 24, I_p = 1.48 A, u_e = 342 and L_e = 35.6 mm, B_{max} is calculated as follows:

$$B_{max} = 342 \times 24 \times \frac{1.48}{35.6} = 341\ mT \quad (26)$$

4.6.3 Auxiliary winding count

The auxiliary winding can be used for two purposes. It can sense demagnetization of the inductor and also generate the required voltage to power the controller. If the winding is used for demagnetization only, the voltage generated can be much smaller than when using the winding to supply the V_{cc}. This affects the winding ratio. For demagnetization detection, both the negative and positive voltage should be larger than the threshold level. For V_{cc} generation using a single diode rectifier, it is most efficient to take the longest time of $\delta 1$ and $\delta 2$ and dimension the winding accordingly. For interval $\delta 2$, Equation 27 applies:

$$V_{aux} = \frac{N_{aux}}{N_{L3}} \times V_{o(min)} \Rightarrow N_{aux} = \frac{V_{aux} \times N_{L3}}{V_{o(min)}} \quad (27)$$

Example: If $V_{o(min)}$ = 100 V, N_{L3} = 24 and V_{aux} = 14 V, then N_{aux} = 3.36 (rounded up to the closest higher integer, in this case 4)

Note that the voltage on the auxiliary winding should always be higher than the minimum V_{cc} voltage as required by the IC. There is voltage loss over the inductor and the rectifier diode, and there is ripple on the V_{cc} due to discharge. All these factors have to be taken into account. There is a direct relationship between the voltage on the auxiliary winding and the converter output voltage. The output voltage depends on the sum of the forward voltages of the attached LED's. Consequently, the minimum V_f should be taken as the starting point for checking if sufficient voltage is available on the auxiliary winding.

4.6.4 Wire diameter selection

Wire diameter selection is a trade-off between the available winding area, resistive losses, proximity losses and skin losses. When using wire sizes below 0.6 mm diameter at operating frequencies below 200 kHz, the skin losses are normally negligible. Above 0.6 mm diameter, it is recommended that Litze wire, or multiple strands, are used. Skin depth can be calculated using Equation 28:

$$\delta = \sqrt{\frac{2 \times \rho}{2 \times \pi \times f_{eff} \times u_r \times u_o}} \quad (28)$$

In which: $u_o = 0.4 \times \pi \times 10^{-6}$, ρ = resistivity = 17 X 10^{-9} (copper). U_r (copper) = 1.

Example: At 100 kHz sinusoidal current, using copper, the skin depth will be 0.21 mm.

The effective frequency does not correspond to the converter frequency, but to the harmonics of the applied waveform. For a triangular wave current, the amplitude and frequency of the waveforms can be deducted using Fourier analyses. The amplitude of the coefficients depends on the ratio between $\delta 1$ and $\delta 2$. as can be seen in Table 4.

Table 4. Harmonics amplitude coefficients

Ratio	1st	2nd	3rd	4th	5th	6th	7th
0.05	0.334	0.165	0.108	0.078	0.060	0.048	0.039
0.2	0.372	0.151	0.067	0.023	0	0.010	0.003
0.5.	0.405	0	0.045	0	0.016	0	0.008

A higher converter ratio will also give more high order harmonics, as well as increased core and proximity losses in the transformer. These harmonics must be filtered in order to be EMC compliant and this requires either more or improved input and output filtering. The resistive losses depend on the peak currents in the wires. They can be estimated by simply calculating the wire resistance, and calculating the average power dissipation in the wire. As an approximation, the current density should be between 300 and 500 Circular Mills(CM)/Amp. Table 5 shows wire sizes related to current:

Table 5. Wire selection table

Diameter (mm)	Nearest AWG	Area (mm^2)	Area (CM)	DC Res. (Ohm/m)	Typical Current I_I (A)
0.1	38	0.008	15	2.195	0.04
0.2	32	0.031	62	0.549	0.15
0.25	30	0.049	97	0.351	0.24
0.315	28	0.078	154	0.221	0.38
0.355	27	0.099	195	0.174	0.49
0.4	26	0.126	248	0.137	0.62
0.56	23	0.246	486	0.070	1.22
0.71	21	0.396	781	0.044	1.95
16 × 0.2	-	0.503	992	0.034	2.48
37 × 0.2	-	1.162	2294	0.015	5.73
61 × 0.2	-	1.916	3782	0.009	9.45

4.7 V_{cc} generation dimensioning.

When the auxiliary winding is also used for V_{cc} generation, the following aspects must be taken into account:

- At startup, the converter is not working and no voltage is generated in the auxiliary winding. There must always be a startup circuit present that is capable of providing sufficient current to the V_{cc} for the first few cycles.
- The voltage on the auxiliary winding depends on the output voltage. As a result, worst case situations should be used to calculate whether minimum power demands are met and if dissipation and current values are within limits.
- Voltage is only present during part of the cycle. The average current flowing towards the V_{cc} of the IC should be sufficient to drive the IC. Consequently, the peak current flowing should be higher than the average current that is required.

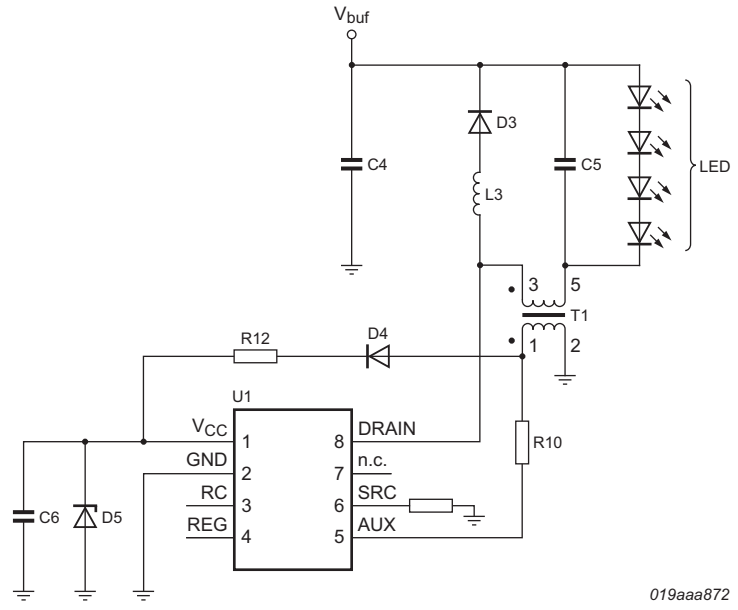


Fig 6. V_{CC} generation circuit

Example 1: At V_{aux} = 14 V, I_{cc} = 2 mA at 12 V, $\delta 2$ = 46 %. V(R12) = 14 – 12 – 0.7 = 1.3 V, I(R12) = 2 mA / 0.46 = 4.34 mA.

R12 = 1.3 V / 4.34 mA = 299 Ω. Round down gives 270 Ω.
P(R12) = $I^2 \times R \times \delta 2$ = 2.4 mW.

Example 2: At V_{aux} = 18 V, I_{cc} = 2 mA at 12 V, $\delta 2$ = 4 %. V(R12) = 18 – 12 – 0.7 = 5.3 V. I(R12) = 2 mA / 0.04 = 50 mA.

R12 = 5.3 V / 50 mA = 106 Ω. Rounding down gives 100 Ω. P(R12) = 10 mW.

If the circuit is dimmable, a recalculation must be made representing a worst case scenario. Some ICs, such as the SSL1523 and SSL2101, have internal HV generation. If sufficient drain voltage is available, the IC is capable of providing its own supply. Note that a smaller interval of current charge and a larger tolerance, leads to over-dimensioning of this circuit and increases the losses in the serial resistor (R12), diode (D4) and inductor. The margin might require additional protection against V_{cc} overvoltage and to accommodate this, a zener diode (D5) is included in the circuit.

4.7.1 Buffer capacitance C6 calculation:

When V_{cc} is generated, the incoming current must be buffered to provide a continuous and stable voltage. The voltage drop over C6 should be such that V_{cc} does not drop below the minimum voltage. Equation 29 can be applied to determine the capacitor value:

$$C_6 = \frac{I_{cc} \times \Delta t}{\Delta V} \quad (29)$$

Example: If ΔV = 1.3 V, I_{cc} = 2 mA and Δt = 6 μs, then C6 will be at least 9.23 nF.

In practice, the value chosen for C6 is much higher to reduce noise and capacitive coupling with the surroundings. Common values for C6 are between 1 μF and 4.7 μF.

4.8 Demagnetization detection dimensioning

Several Silergy ICs have demagnetization detection functionality that uses a pin with minimum and maximum threshold voltages. The Silergy range of LED drivers have levels that are set to −100 mV and +100 mV. There is also a negative and positive clamping diode with a threshold of 0.5 V. The clamping diodes have a maximum current level $I_{demag(max)}$. When using an auxiliary winding, the current should be limited to a level where the threshold voltages are reached and the maximum current not exceeded.

Example: If V_{aux} = 14 V and 100 μA < I_{aux} < 5 mA, then R_{aux} (R10) = 14 / 100 × 10^{-6} = 140 KΩ.

Note that the demagnetization detection is phase dependent and the winding direction should be opposite to the main inductor in order to start next cycle at low valley. Reversing the winding will result in switching at top detection.

5. Power calculations

The efficiency of a buck converter is one of the critical specifications for the design. One of the things to consider, is that efficiency is always relative. Some of the losses of a buck converter, such as the IC V_{CC} generation, are fixed and depend on the IC. Because of fixed losses, efficiency tends to deteriorate with lower output power. The variable losses consist of a number of factors, and these are discussed in next sub-chapters. The formulas in these chapters will give the designer insight into the parameters that determine the losses for each component.

5.1 Resistive switch dissipation

In addition to capacitive losses (see Equation 7), there are also resistive losses in the switch. The main parameters that determine these losses are the peak current and the resistance of the switch, which is expressed as R_{DSon} for MOSFET switches. There is a momentary peak dissipation and an average dissipation.

$$P_{peak} = I_{peak}^{2} \times R_{DSon} \tag{30}$$

For the duration of period t1, the total dissipation will be as shown in Equation 31

$$P = \frac{1}{3} \times I_{peak}^{2} \times R_{DSon} \tag{31}$$

For the total time period, the average resistive switch dissipation will be as shown in Equation 32:

$$P = \frac{1}{3} \times t_1 \times f \times I_{peak}^{2} \times R_{DSon} \tag{32}$$

Example: If f = 89.6 kHz, R_{DSon} = 2.2 Ω, I_{peak} = 1.48 A and t1 = 5.28 μs, then P = 0.76 W.

5.2 Capacitive switch dissipation

The capacitive switch losses have already been discussed in Section 4.3 Equation 7. It is important to note that these losses are independent of the peak current and subsequently the LED current. By using valley detection and an output voltage that is half the input voltage, these capacitive switching losses can be avoided.

Without this option, the balance between switch size causing lower R_{DSon} losses, and capacitive switch losses will shift. A larger switch will have lower R_{DSon}, but higher drain capacitance. In such a situation, the optimum has to be selected:

For the following examples, I_{peak} = 1.48 A, t1 = 5.28 μs, V_{sw1} = 100 V and f = 89.6 kHz.

1. If I_d = 1.5 A, R_{DSon} = 5.5 Ω, C = 300 pF, P_{RDSon} = 1.9 W and P_{csw} = 0.13 W, then P_{tot} = 2.03 W
2. If I_d = 3.5 A, R_{DSon} = 2.2 Ω, C = 550 pF, P_{RDSon} = 0.76 W and P_{csw} = 0.24 W, then P_{tot} = 1 W
3. If I_d = 13 A, R_{DSon} = 0.42 Ω, C = 3.1 nF, P_{RDSon} = 0.14 W and P_{csw} = 1.39 W, then P_{tot} = 1.53 W

Remark: Of the three previous examples, example 2 provides the best performance.

5.3 Switching losses

In addition to the capacitive losses, there are also losses due to hard switching. There is a switching slope time during which there is an overlap of the current and voltage, resulting in dissipation.

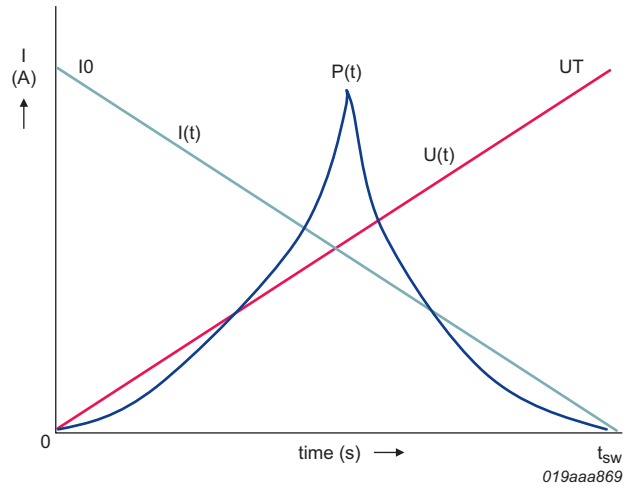


Fig 7. Switching loss graph

Assuming that the current drop and the voltage rise is linear, within a fixed time t_{sw}, the dissipation can be calculated as follows:

$$I(t) = I_0 - \frac{I_0}{t_{sw}} \times t = I_0 \times \left(1 - \frac{t}{t_{sw}}\right) \quad (33)$$

$$U(t) = U_{t_{sw}} \times \frac{t}{t_{sw}} \quad (34)$$

Using Equation 33 and Equation 34, results in Equation 35.

$$P(t) = I(t) \times U(t) = I_0 \times \left(1 - \frac{t}{t_{sw}}\right) \times U_{t_{sw}} \times \frac{t}{t_{sw}} \quad (35)$$

$$E = \int P(t)dt = \int_0^{t_{sw}} I_0 \times \left(1 - \frac{t}{t_{sw}}\right) \times U_{t_{sw}} \times \frac{t}{t_{sw}}\, dt \Leftrightarrow \quad (36)$$

$$E = \int_0^{t_{sw}} \frac{I_0 \times U_{t_{sw}}}{t_{sw}^2} \times t\, dt - \int_0^{t_{sw}} \frac{I_0 \times U_{t_{sw}}}{t_{sw}^2} \times t^2 dt \Leftrightarrow \quad (37)$$

$$E = \frac{1}{2} \times \frac{I_0 \times U_{t_{sw}}}{t_{sw}} \times t_{sw}^2 - \frac{1}{3} \times \frac{I_0 \times U_{t_{sw}}}{t_{sw}^2} \times t_{sw}^3 = \quad (38)$$

$$\times I_0 \times U_{t_{sw}} \times t_{sw} \qquad P_{eff} = \frac{1}{6} \times I_0 \times U_{t_{sw}} \times f \times t_{sw} \quad (39)$$

Example: t_{sw} = 100 nS, I_o = 1.5 A, U_{tsw} = 200 V, f = 88 kHz. P_{eff} = 0.44 W.

The dissipation increases with the switching time. When using valley detection, these losses are reduced at switch-on but they are still present at switch-off.

5.4 Freewheel diode losses

The freewheeling diode has two loss mechanisms, forward losses and the reverse charge losses. The forward, or conductive, losses can be estimated using the time with respect to current and voltage drop given in Equation 40: and Equation 41.

$$P_f = I_{led} \times V_f \times t2 \times f \quad (40)$$

$$P_{rev} = \frac{1}{2} \times V_I^2 \times C_{rev} \times f \quad (41)$$

Example: If f = 89.6 kHz, I_{led} = 0.7 A, t2 = 5.28 μs, V_f = 0.7 V, V_I = 200 V and C_{rev} = 10 pF then P_f = 230 mW and P_{rev} = 18 mW.

The forward voltage of the diode can be lowered using a Schottky diode, but these diodes are often difficult to obtain with reverse voltages above 100 V. Care should also be taken not to oversize this diode, as it does not appreciably lower the forward losses and the reverse charge is often directly related to the maximum current rating of the diode.

5.5 Inductor losses

The inductor has several loss mechanisms. The calculation of these losses is very complex and there is much debate on the way these losses contribute to the total inductor losses. Section 5.5 simply illustrates a number of the loss mechanisms within the inductor.

5.5.1 Resistive losses

The cause of resistive losses is a combination of wire length and its thickness. The calculation of the resistance and the losses can be derived from Equation 42 and Equation 43:

$$R_{DC} = \rho \times \frac{l}{A} \quad (42)$$

$$P_{DC} = \frac{1}{t_{sw}} \times \int_0^{t_{sw}} I^2 \times R_{DC}\, dt = \frac{1}{3} \times I_p^2 \times R_{DC} \quad (43)$$

Example: For a wire length of 1 m with a diameter of 0.56 mm:

If $\rho_{Cu} = 17.2 \times 10^{-9}$, $A = \pi \times R^2$ (= 0.246 x 10^{-6}), R_{DC}= 70 mΩ and I_p = 1.48 A, then P_{DC} = 51 mW.

5.5.2 Proximity losses

The full calculations for proximity losses are outside the scope of this application note. What should be made clear, however, it that they are closely related to the skin depth and number of windings. See Figure 8:

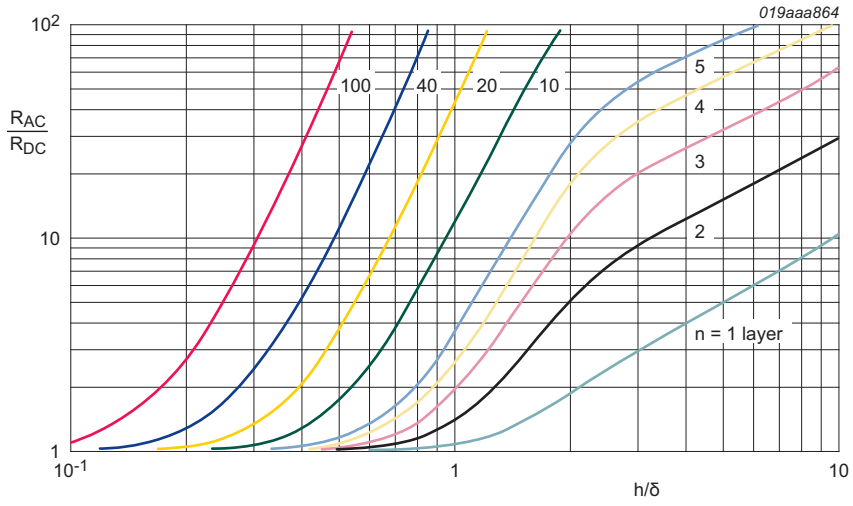


Fig 8. Proximity loss graph

Too many layers of wire with a radius that is close to, or below skin-depth, should be avoided. Normally, the proximity losses are calculated as a factor of the DC wire resistance: $R_{AC} = n \times R_{DC}$.

Maintaining low resistive losses helps to lower proximity losses which is another drawback of the CCM mode inductor. To achieve higher inductance, more windings are required, thereby increasing DC and AC resistance and countering the lower core losses.

5.5.3 Core losses

The core losses in the magnetic material are determined by the magnetization curve and frequencies. The magnetic field in the core material is excited by the magnetic flux density for each converter cycle. This produces a highly non-linear curve. It has hysteresis and it shows saturation level. The surface area enclosed by the variation in B-field strength at a certain frequency determines the losses. A bigger core, a higher B-field and higher frequency, increase these losses. The loss per unit of volume of the core material, for given frequencies, is shown in the core material data sheet. Figure 10 displays such a curve.

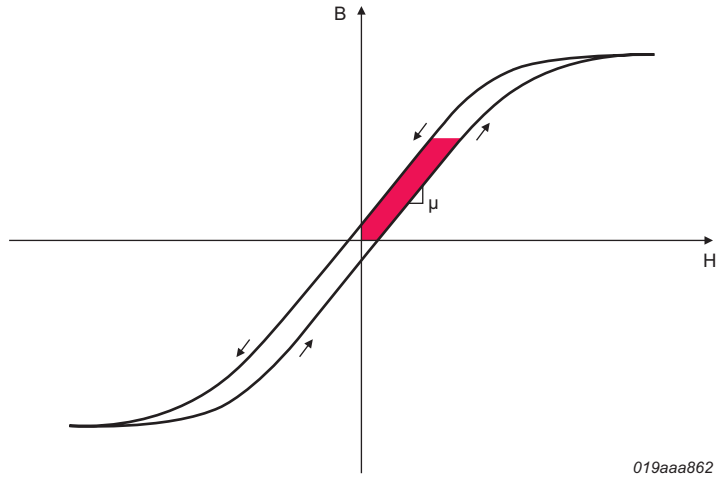


Fig 9. BH curve magnetic material

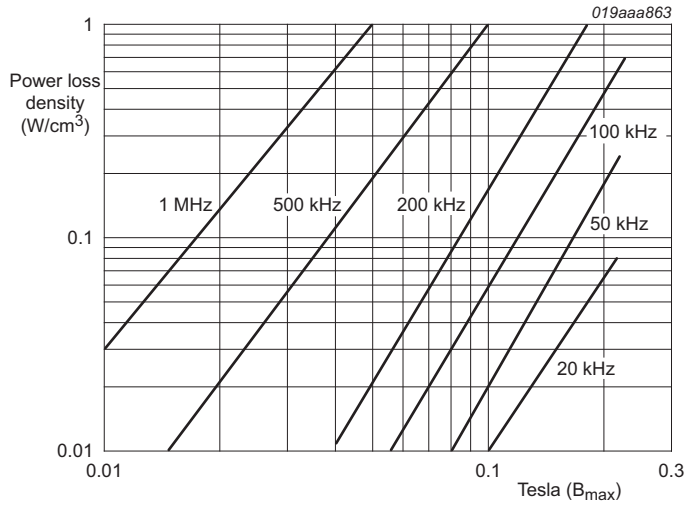


Fig 10. Material loss graph

A simple empirical formula that calculates core loss is the Steinmetz equation as shown in Equation 44:

$$P_h = K_h \times f^{\alpha} \times B_{max}{}^{\beta} \times V_{core} \quad (44)$$

K_h and α are dependent on core material. This formula can be improved by including the harmonics of a square waveform as shown in Equation 45:

$$P_{nse} = K_h \times (2f)^{\alpha} \times B_{max}{}^{\beta} \times (D^{1-\alpha} + (1-D)^{1-\alpha}) \times V_{core} \quad (45)$$

In Equation 45, D is duty cycle, B_{max} the peak flux density, 'f' is the frequency of the fundamental and V_{core} is the volume of the core. This demonstrates that a higher frequency, higher flux density, smaller duty-factor and bigger volume all increase core losses. A larger core might not always reduce core losses. If the B-field is already low, the increase in volume will counter the lower losses due to reduced flux density.

Example: At a duty cycle of 50 %, with K_h = 0.05, f = 80 (kHz), α = 1.8, B_{max} = 100 mT, β = 3 and V_{core} = 2.4 cm^3, the loss will be $0.05 \times (160\ k)^{1.8} \times (0.1)^3 \times 3.58 \times 2.4^{-6}$ = 1.36 W.

5.6 Sense resistor losses.

For the sense resistor losses, Equation 32 can be applied. R_{DSon} is replaced with sense resistor value.

Example: t_1 = 5.28 μs, f = 89.6 kHz, I_{peak} = 1.48 A, R_{sense} = 0.5 / 1.49 = 0.33 Ω, P_{sense} = 113 mW

5.7 Total system losses

When undertaking buck power calculations, it is vital to consider the impact of each individual loss on the total converter efficiency. This aspect is illustrated by taking a single driver with a set current, a 200 V input voltage, and varying the output voltage in steps. The relationship between the input voltage and the output voltage is plotted on the X-axis as a ratio. Each loss mechanism is calculated, and the resultant driver efficiency plotted.

Figure 11 illustrates the converter efficiency dropping at a low ratio. This is not caused by an excessive increase in losses, but by the relative decrease of useful output power. Some losses, such as the magnetic core losses and the resistive losses in the switch, are reduced. There is an increase in the forward losses in the freewheel diode, the capacitive switching losses and the losses due to hard switching. This is logical, as the conduction time t2 of the freewheel diode is large and the voltage drop over the switch is also large.

It demonstrates that a very low resistance switch will be more helpful for a large ratio, such as 50 % to 90 %. Low switch capacitance, low forward voltage of the freewheel diode and fast switching are more effective for a small ratio, 5 % to 20 % for example.

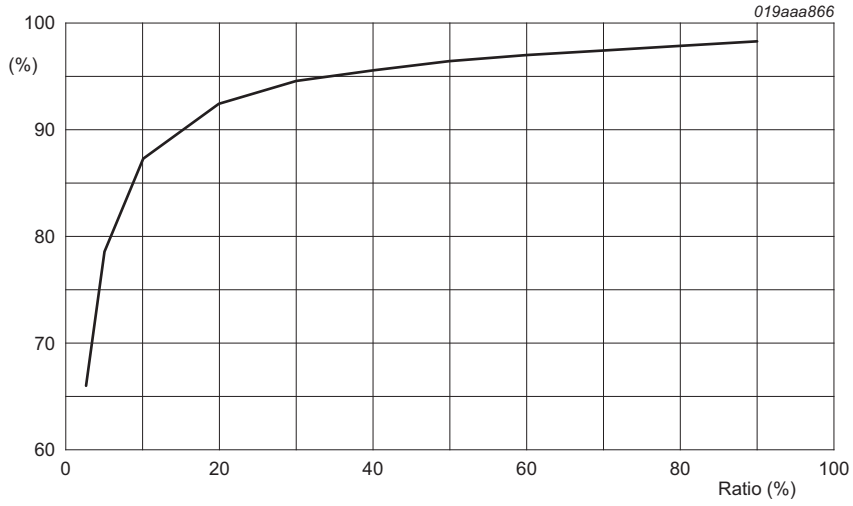
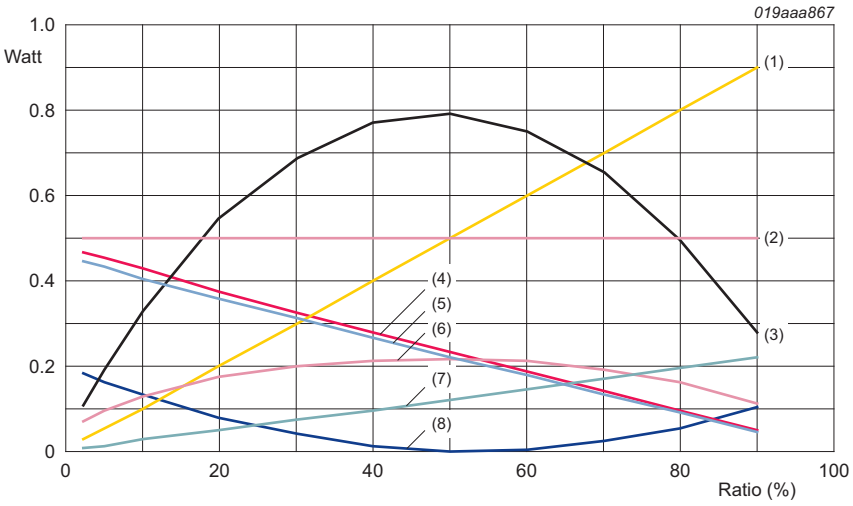


Fig 11. Buck converter efficiency



(1) = P_{rsw}
(2) = P_{csw}
(3) = P_{core}
(4) = P_{forw}
(5) = P_{fsw1}
(6) = P_{prox}
(7) = P_{Rsense}
(8) = P_{contr}

Fig 12. Buck converter losses

6. Current tolerance and stability

6.1 Current tolerance

In essence, there are only two main components that determine current tolerance. One is the spread on detection voltage and the second is the tolerance sense resistor. This can be derived from Equation 46:

$$\Delta I_{led} = \Delta I_{peak} = \Delta V_{ocp} + \Delta R_6 \quad (46)$$

Example: If $V_{ocp(min)}$ = 0.48 V, $V_{ocp(avg)}$ = 0.50 $V_{ocp(max)}$ = 0.52 V, ΔV_{ocp} = ±4 % and ΔR_6 = ±1 %, then ΔI_{led} = ±5 %.

There is the possibility that the variation of C_p and L_p with valley detection will have some influence, but in practice, the time influenced is much smaller then the total cycle time.

Example: If ΔL_p = 10 % and $\delta 3 / t_{total}$ = 0.052 then $\Delta I_{led} = 0.5 \times \Delta L_p \times 0.05$ = 0.25 %.

6.2 Current stability

For the buck converter using peak current control, stability is seldom an issue. This is because the current is controlled per cycle and it is intrinsically stable. If some other means is used to stabilize the current, such as current mirror detection, accuracy might increase but the loop response must be calculated. The main component that determines response at peak current control, is the output capacitor C5. It has to be charged and discharged. At switch-on, the discharged capacitor will have to reach working voltage before any current flows through the LED's and light is produced. This time is equal to the charge time of Equation 47.

$$\Delta t \geq \frac{\Delta V \times C5}{I_{CC}} \quad (47)$$

Example: With ΔV = 100 V, I_{CC} = 700 mA and C5 = 3.3 μF, then Δt will be at least 471 μs.

At turn-off, the diode characteristic of the LED will be effective. Instead of a sudden drop, there will be an exponential drop of current, starting with the nominal current. The LED current will slowly fade until it is no longer visible. In practice, this can take several seconds. Since the LED's are placed in a self-rectification loop with the freewheel diode, any capacitive coupling on the drain side, or inductive coupling over the loop with an AC source will induce a current through the LEDs. Even a current as small as 100 μA, could be visible. This can happen if large, ungrounded objects such as heat-sinks connected to phase, are in close proximity to the LEDs,

7. Summary

This document provides an overview of operations and calculation of the buck converter in discontinuous conduction mode. It explains why valley detection is a key feature, and it shows how a number of key components can be calculated. It closes with a description of loss mechanisms in the converter, and how they contribute to driver efficiency.

8. Abbreviations

Table 6. Abbreviations

Acronym	Description
BCM	Boundary Conduction Mode
CCM	Continuous Conduction Mode
CM	Circular Mills
EMC	ElectroMagnetic Compatibility
DCM	Discontinuous Conduction Mode
IC	Integrated Circuit
LED	Light Emitting Diode
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
SMPS	Switch Mode Power Supply
SSL	Solid State Lighting