AN10912

SMPS EMC and layout guidlines

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Document information

Info	Content
Keywords	EMC, EMI, IEC61000, AC/DC, DC/DC, SMPS, conducted emission, PCB.
Abstract	This application note is a guide to assist in the design and layout of a Switch Mode Power Supply (SMPS) Printed-Circuit Board (PCB) as used in adaptors and lighting applications. The SMPS is designed to be compatible with EMC/EMI standards.

Revision history

Rev	Date	Description
v.1	20110218	first issue

1. Introduction

SMPS converters operate on frequency bands where passive components (PCB, decoupling capacitors, PCB connections, packages) are not considered ideal because they contain parasitic elements e.g. inductance, resistance, etc. Because the impedances are frequency dependant, the emission levels generated by voltage, and current drops may not be compliant with certain EMC standards. Many different EMC standards are used throughout the world. In addition to the localized region or country standards applicable where the design will be utilized, the type of application might also require a specific set of standards to be met in order to pass EMC/EMI standards.

These standards are under copyright and must therefore be purchased through official sales channels.

For the USA market, FCC Part 15 covers radio frequency devices capable of emitting RF energy in the range of 9 kHz to 200 GHz. Conducted emissions are regulated by the FCC over the frequency range 450 kHz to 30 MHz, and the CISPR 22 conducted emissions limits extend from 150 kHz to 3 MHz. Testing should be carried out according to ANSI C63.4-1992. Part 18 covers industrial, scientific, and medical (ISM) equipment.

For the European market, EMC Directive 89/336/EEC sets out the legal requirements for principally all electric/electronic equipment to be placed or used in the common market and the whole european economic area. International standards concerning EMC are primarily developed by the International Electrotechnical Commission (IEC) and the International Special Committee on Radio Interference (Comite International Special des Perturbations Radioelectriques - CISPR).

For the new extensive series developed by the IEC, see Ref. 1 to Ref. 6.

Due to the fact that many EN standards are based on IEC and/or CISPR standards, international and European EMC standards are generally becoming harmonized. There are also some similarities between international and U.S. standards, although they are not interchangeable.

EMC standards are continuously being developed, revised and updated, and much confusion can arise regarding which standards are applicable to specific applications. It is therefore important to always be aware of the publication status for standards, to be aware if a new standard is to be expected in the near future and subsequently, when an old standard becomes invalid.

The following dates are important:

- Date Of Publication (DOP)
- Date Of Withdrawal (DOW) of a conflicting (earlier) standard

Draft standards are sometimes referred to as ‘preliminary’, for example prETS or prEN. Temporary EN standards are termed ENV.

Standards can be divided into two categories:

- Generic standards
- Product standards

If no product standard is applicable, the current generic standard must be followed.

A product standard covers all the EMC requirements for a certain product type. In some cases, product standards will also cover the electrical safety requirements. A product standard takes precedence over all other standards. Once it is determined that a product is within the scope of an applicable product family standard concerning emissions and/or immunity, then that standard should be followed. For some examples of family standards see Ref. 7 to Ref. 12.

More recent product family standards also tend to appear as complementary emissions and immunity standards, see Ref. 13 and Ref. 14.

For specific types of product family standards transferred into general standards see Ref. 15 to Ref. 18.

There are a limited number of pure product standards that cover all EMC requirements, consequently an appropriate product family standard must be used. An additional complication is that a product can simultaneously belong to different product family standards. For example, most household devices must meet emissions requirements according to Ref. 13, as well as Ref. 15 and Ref. 16 or Ref. 17 and Ref. 18.

It is impossible to accurately predict the EMC compliance of a given system, but by implementing specific rules and design techniques in the design of the application, it is possible to considerably reduce the risks. This application note lists the major points which can help to minimize EMI and improve EMC performance. It also demonstrates how some basic techniques can help to reduce emission levels and harden the electronic system.

2. Scope

This application note offers guidelines for the design and layout for the Printed-Circuit Board (PCB) of an EMC/EMI standards compatible Switch Mode Power Supply (SMPS). SMPS designs are typically used in power supply and lighting applications.

The document is laid out so that each chapter can be read with a minimum of cross references to other documents or data sheets. This will lead to some repetition as the information within this application note may also be available in other, more dedicated documents. Where possible, typical values are used to improve clarity.

- Section 1: provides a brief description of SMPS converters and introduces some international and european EMC standards
- Section 2: outlines the purpose and format of this application note
- Section 3: explains the topology
- Section 4: provides basic checklists for EMC compliance and necessary relevant processes
- Section 5: provides an extensive description of how to reduce HF signature
- Section 6: is a brief conclusion
- Section 7: offers additional information on capacitor marking and codes etc.

3. Topology of the EMC environment

Figure 1 shows the topology of an EMC environment. A noise source drives a current $i_{(t)}$. This current flows through the left coupling path (a PCB connection for example) and causes a voltage drop. This voltage perturbation is transmitted to the victim through the right coupling path and can cause a malfunction if the level is high enough.

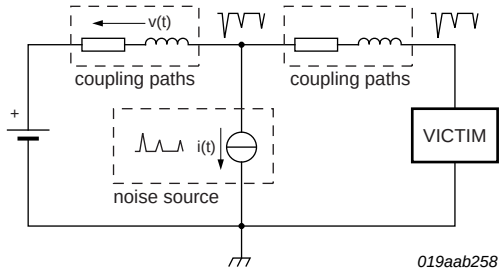


Fig 1. Elements of EMC environment

The EMC environment effecting these elements must be analyzed in order to significantly improve the EMC quality of the design.

4. Basic checklist for EMC compliance

The basic rules for minimizing the conducted and radiated emissions through the power supply, are given in the checklists provided in Section 4.1 to Section 4.6.

4.1 Reducing the HF signature of the system

- Slope and duty-factor control
- Filter and dampen at the noise source
- Adapt the converter frequency to fit EMC curve

4.2 Reducing the magnetic loops of the PCB

- Decrease the surface area of the magnetic loops
- Use a decoupling capacitor
- Maintain the signal trace close to the return path
- Prevent edge radiation
- Microstrip technology
- Reduce VCC/VSS network
- Shorten the loops around the oscillator

4.3 Cancelling the H field

- Opposite magnetic loops
- Complimentary magnetic loops
- Connect V_{CC} and ground close together
- Increase the PCB connection widths

4.4 Reducing the parasitics of all devices

- Select the proper PCB technology
- Utilize ground and power planes
- Grounding techniques
- Adapt the decoupling capacitors to the working frequency of the converter
- Shorten the capacitor connection lengths
- Choose COG and NPO dielectric types
- Bypass electrolytic capacitors
- Adapt inductors to the working frequency of the converter
- Prevent mutual coupling of inductors
- Increase distance between the noise source and the victim

4.5 Frequency domain analysis

- Differential and common mode noise
- X and Y type capacitors
- Dampen unwanted HF signals

4.6 Shielding

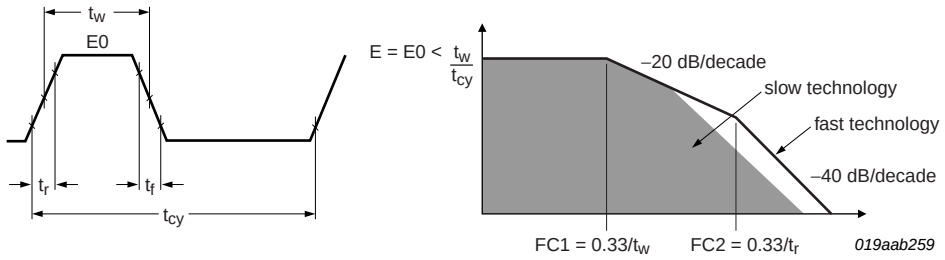
- Mount hot winding at inner layer
- Attach heatsink to clean potential
- Use component material and heatsink as shield
- Use capacitive shielding
- Decouple other floating potentials

Sub chapters Section 4.1 to Section 4.6 are detailed in Section 5

5. Reducing the HF signature of the system

5.1 Slope and duty factor control

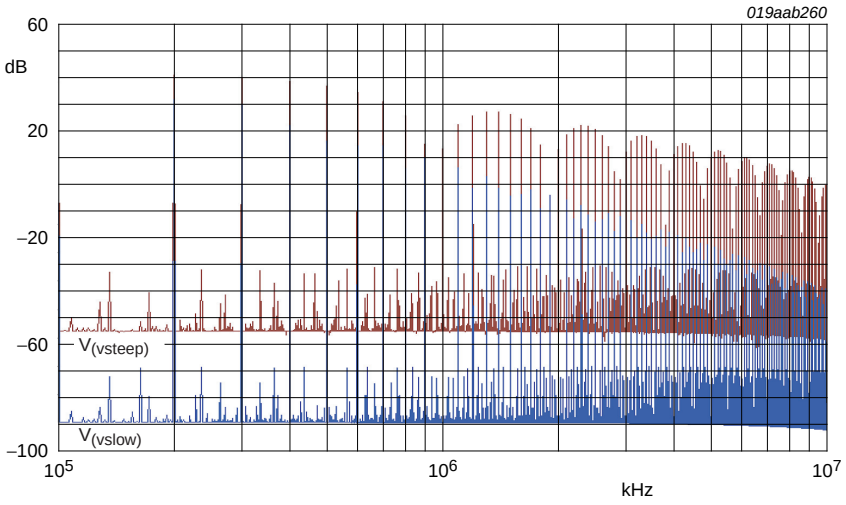
A key element in the reduction of EMI, is the selection of the slowest slope of voltage and current changes in time. This is especially applicable on the main inductors current waveforms and voltages on the switches. The spectral envelope of such a signal, has two cut-off frequencies and is shown in Figure 2. The first one (FC1), depends on the pulse width of the signal and the second one (FC2), depends on the sharpness of the transition mainly due to the technology used. A more gradual transition and a more even duty-factor, gives a lower EMI signature.



t_w = pulse width, t_r = rise time, t_f = fall time, t_{cy} = cycle time

Fig 2. Spectrum of the trapezoidal signal for a fast and slow technology

Theoretically, halving the maximum operating frequency limit, reduces the EMI by 12 dB. Figure 3 shows the spectrum of a 100 kHz pulsed source with both steep and slow slopes, and different duty factors.



$V_{(vsteep)}$ flanks by 50 nS, T_{on} = 1 µS

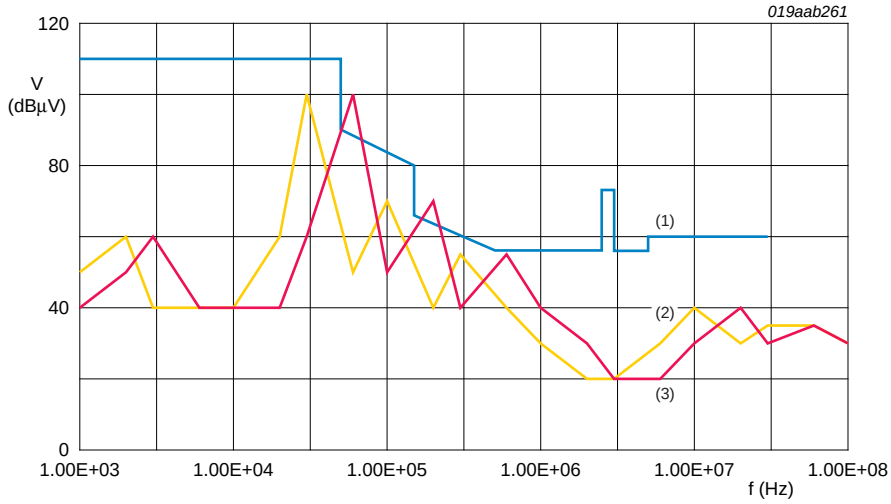
$V_{(vslow)}$ flanks by 2 µS, T_{on} = 3 µS

Fig 3. Spectrum of a 100 kHz pulse source

5.2 Filtering and damping at the noise source

One of the basic rules for preventing EMC, is to identify and locate possible noise source(s) and to apply counter-measures to them. They are most common where the largest voltage and current changes occur, e.g. switching elements. Components such as inductors and transformers, can also cause additional noise by oscillating at their resonant frequency when not being driven (ringing). Filtering can block the path from the noise source to the surroundings, but it does not decrease the noise energy. As a result, the signal will look for alternative paths by which it can propagate and damping dissipates the electrical or magnetic energy. A combination of damping and filtering provides the most effective solution.

5.3 Adapting converter frequency to an EMC curve



(1) Normal (reference)
(2) 30 kHz pass
(3) 60 kHz fail

Fig 4. Comparing two different converter frequencies with a reference

Another key parameter to pass EMI is to adapt the converter frequency to fit with test criteria. Figure 4 shows an example, where a converter at 60 kHz fails and when shifted to 30 kHz passes. The drawback of this method is that lowering the frequency also lowers the power output for a given inductor size. Alternatively, switching losses and filtering may be less. When selecting a converter working frequency, it is beneficial to consider the test requirements.

5.4 Reducing the PCB magnetic loops

5.4.1 Decreasing the surface area of the magnetic loops

A current flowing around a loop generates a magnetic field (H) proportional to the area of the loop. Equation 1 and Equation 2 give the mathematical expressions for when the observation distance is in both the near field and the far field conditions.

$$Hnear_{A/m} = I \times \frac{S}{4 \times \pi \times D^3} \quad (1)$$

$$Hfar_{A/m} = \pi \times I \times \frac{S}{\lambda^2 \times D} \quad (2)$$

where:

- I = loop current (A)
- S = loop surface (m^2)
- D = observation distance (m)
- λ = current wavelength (m)

The near field and far field conditions are expressed by Equation 3:

$$\frac{D}{\lambda} = \frac{1}{2 \times \pi} \quad (3)$$

This ratio indicates the transition at the point where the emission is in far field or in near field condition (see Figure 5). The far field condition is a specific distance where the electrical and magnetic fields are coupled and perpendicular. In this condition, the ratio E/H is the intrinsic impedance of free space equal to 300. In the near field condition the nature of the fields depends on the connection impedance. For a high impedance ($Z > 300$) the field is electric and for a low impedance ($Z < 300$) the field is magnetic.

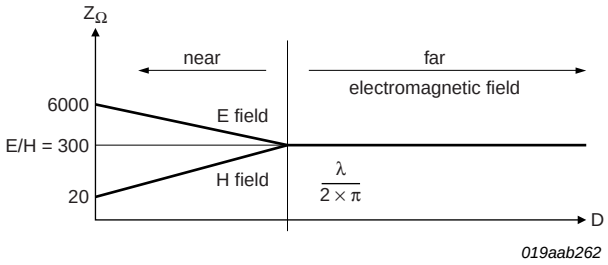


Fig 5. Near and far field conditions

Example:

At 3 meters, F = 30 MHz and I = 0.1 A, the magnetic field intensity is −19.6 dbμA for a 1 cm^2 surface loop and −13.6 dbμA when the loop surface is doubled. Reducing the surface area by a factor of two will decrease the H field by 6 dB. This can be achieved by carefully checking the PCB layout.

5.4.2 Magnetic loop and ohmic voltage drop

The decoupling capacitor reduces the magnetic loop and ohmic voltage drop. It supplies the fast transient currents locally and reduces the length of the current discharging path. It also contributes to the reduction of the closed contour taken by the current and the radiation surface as shown in Figure 6. Each fast analog and digital circuit part must be decoupled using a capacitor between power and ground. An additional serial ferrite bead is highly recommended to prevent line voltage oscillations.

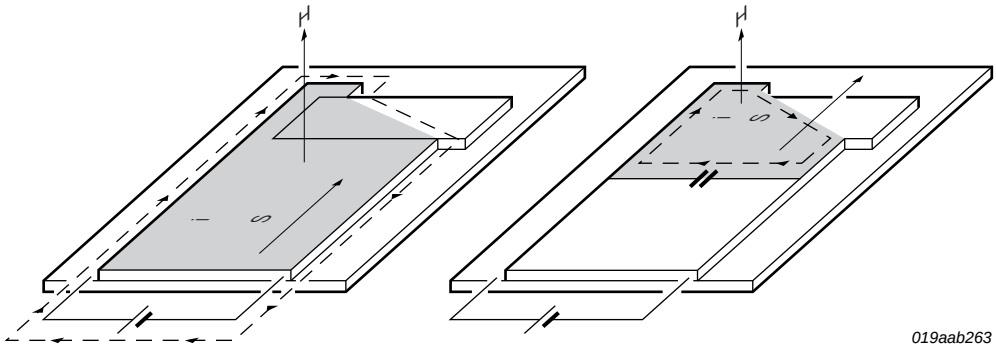


Fig 6. Decoupling capacitor reducing the magnetic field and the loop surface

5.4.3 Parasitic inductance

To maintain a low parasitic inductance of a signal trace, the distance to the ground has to be kept short. The parasitic inductance of two parallel conductors carrying uniform current in opposite directions consists of self-inductance and mutual inductance. Figure 7 shows the two types of parallel conductors and their equivalent electrical model.

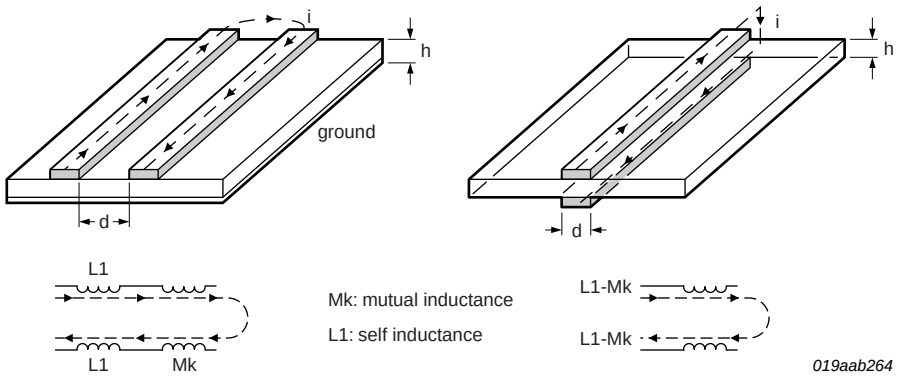


Fig 7. Structure of parasitic inductance

The total inductance for self-inductance (L1) is given in Equation 4 and for mutual inductance (Mk) in Equation 5.

$$LT = L1 + L2 - 2 \times Mk \tag{4}$$

$$Mk = k \times L1 \times L2 \tag{5}$$

L1 and L2 are the self-inductance of the individual conductors, and Mk is the mutual inductance between them. If the VCC and VSS are identical, LT is reduced as shown in Equation 6.

$$LT = 2 \times (L1 - Mk) \tag{6}$$

If the coefficient of magnetic coupling (Mk) between the two conductors is unity, the mutual inductance is equal to the self-inductance of one conductor, since Mk = L1 and the total inductance of the closed loop is zero. To minimize the total inductance of the

complete current path, the mutual inductance between the conductors is maximized. Therefore, the two conductors should be placed as close together as possible to minimize the area between them. Figure 8 shows the mutual inductance for different spacing.

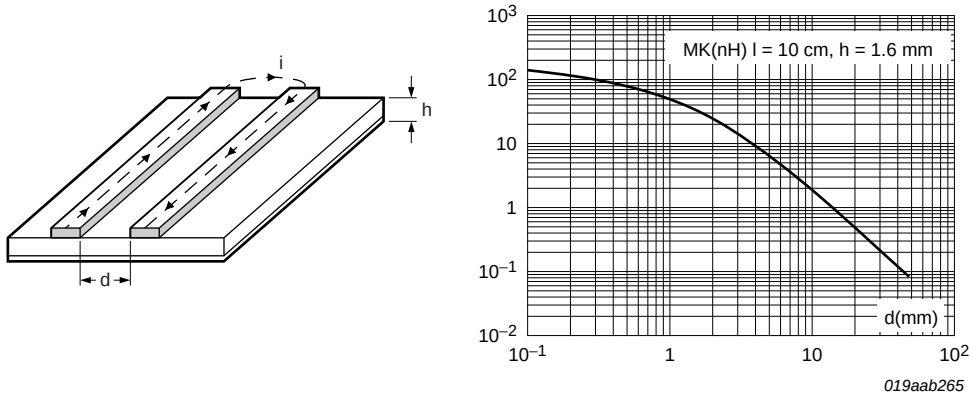


Fig 8. Mutual inductance for l = 10 cm and h = 1.6 mm

Parallel running traces with different signals generally have sufficient distance to prevent crosstalk. These traces should be separated by no less than twice the trace width (2W-rule).

For this configuration, the formula is only applicable if the forward and return currents flow through these two traces. Figure 9 plots different Mk values for various PCB trace dimensions.

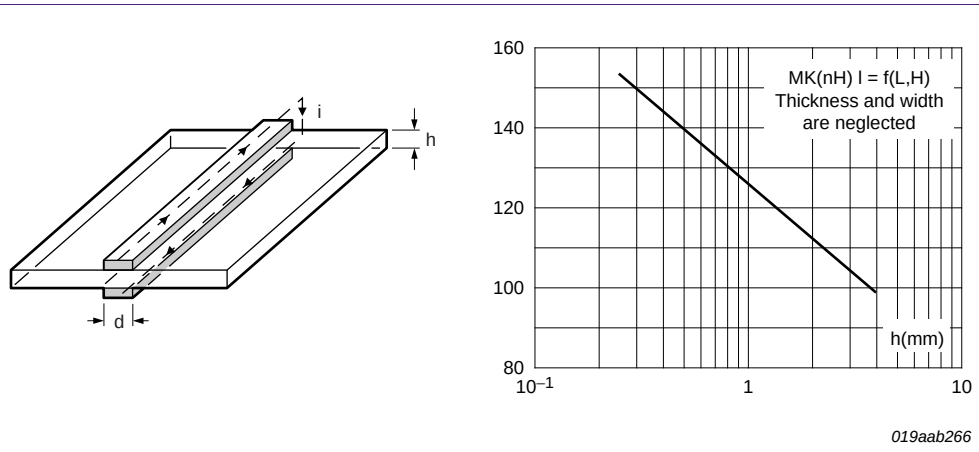


Fig 9. Mutual inductance and the length and height of the PCB traces

Figure 9 clearly shows that a smaller height of PCB trace will reduce inductance and therefore also reduce radiation and crosstalk.

5.4.4 Preventing edge radiation

On a PCB with a ground plane, a trace with a high frequency signal running close to the edge of the PCB will act as an antenna. The distance of these traces from the edge of the board should be 20 times the trace height (20 h-rule) i.e. for a PCB thickness of 1 mm, the trace should be 20 mm from the edge.

5.4.5 Microstrip topology

The total inductance of a loop (LT) is drastically reduced when using a ground plane because the equivalent inductance of the plane (L_{Plane}) is much lower than the PCB trace (L_{Trace}). This is mainly due to the contour taken by the H-field which is much larger than the contour taken around the signal trace. These two inductances are acceptably independent and so can be evaluated separately. The ground plane inductance is not affected by the PCB trace width and can be calculated using Equation 7.

$$L_{Plane}(nH/cm) = \frac{5 \times h}{W} \quad (7)$$

The PCB trace inductance can be calculated using Equation 8

$$L_{Trace}(nH/cm) = 10^{-9} \times In\left(1 + \frac{32 \times h^2}{wt^2} \times \left(1 + \sqrt{\pi \times \frac{wt}{8 \times h}}\right)\right) \quad (8)$$

This inductance is independent of the PCB ground width. For example a trace of 10 cm length and 1 mm width and separated from the ground plane by 1.6 mm presents an inductance of 51 nH. A plane with the same dimensions and 10 cm width presents an inductance of 0.8 nH. So the total inductance is the sum of the PCB trace and plane (51.8 nH). The same trace without the ground plane has an inductance equal to 115 nH. The trace inductance is reduced by a factor of 2.22 due to the plane.

5.4.6 Reducing VCC/VSS network

If there is no dedicated plane for the power, keeping the tracks as close as possible is recommended, in order to reduce the surface of loop and the parasitic inductance that supply power to the IC (see Figure 10).

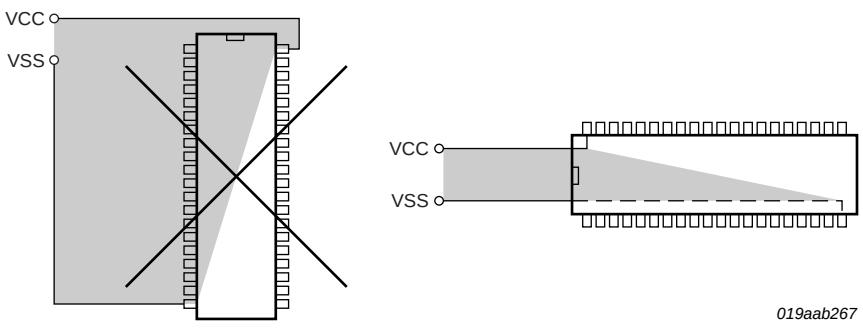


Fig 10. Reduced surface of the VCC and VSS network

This method not only reduces emitted fields caused by steep current changes into the IC, but also reduces the susceptibility of the IC to received disturbance.

5.4.7 Shortening the loops around the oscillator

Figure 11 shows the electrical model of a common oscillator implemented in an IC. At resonance, the fundamental currents i1 and i2 have the same amplitude. In the closed loop mode the oscillator is stabilized in the saturation region of the amplifier that

generates some harmonics in HF. Consequently, the output loop (X2, C2, and VSS) must be optimized first and then the input loop (X1, C1 and VSS). In both cases they must be as small as possible.

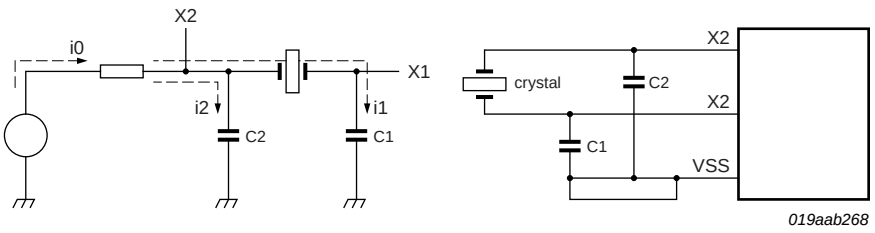


Fig 11. Reduced surface of the oscillator network

5.5 Cancelling the H field

5.5.1 Opposite magnetic loops

Identical circuits can be implemented as shown in Figure 12. In this type of implementation, the magnetic loop surface is the same and the H-field is generated on the opposite side. This tends to cancel them out if the coupling factor is sufficient and surface area and currents are the same.

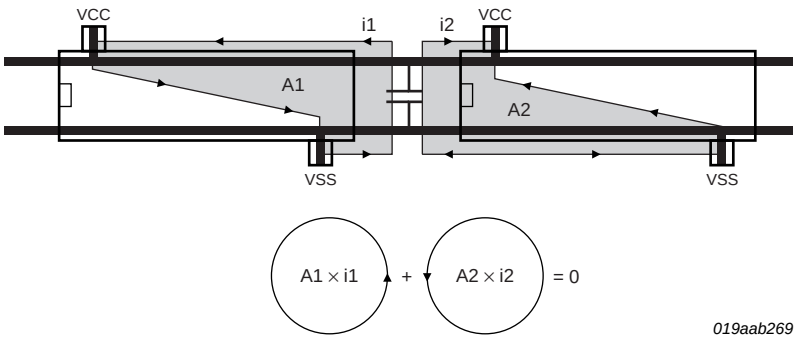


Fig 12. H field cancellation

5.5.2 Complementary magnetic loops

The voltage induced in a parasitic inductance is equal to the change in magnetic flux during the same period. This flux change can be limited by placing loops in close proximity (or overlapping them) where the product of surface area and current is the same. This solution can be used in several SMPS topologies.

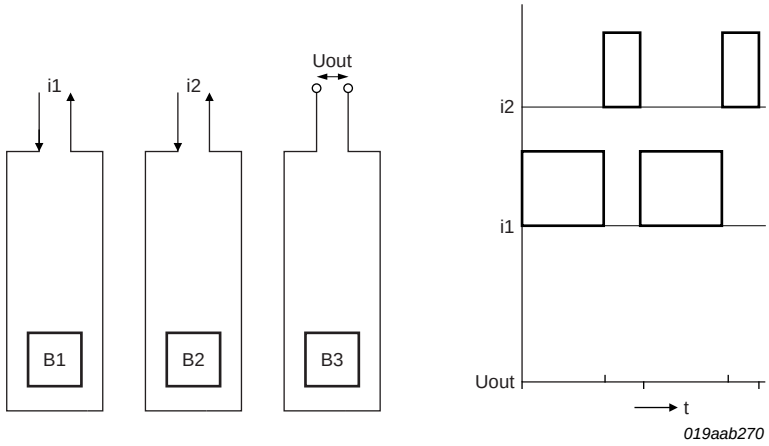


Fig 13. Complimentary H field

Figure 13 displays two current loops creating magnetic fields B1 and B2. Loop B3 represents the victim line over which the potential U_{out} is generated. Because the flux change in time is close to zero, there is only voltage over U_{out} when I2 and I1 take over. The difference in coupling between B1-B3 and B2-B3 causes small spikes.

5.5.3 Connecting VCC close to ground

When ground and VCC pins are close together, the magnetic coupling can be close to 0.8 and the mutual inductance can reach the self-inductance of one pin and cancel the magnetic field of the total inductance of the pins. This is true when ground current and supply current have the same magnitude and the same phase

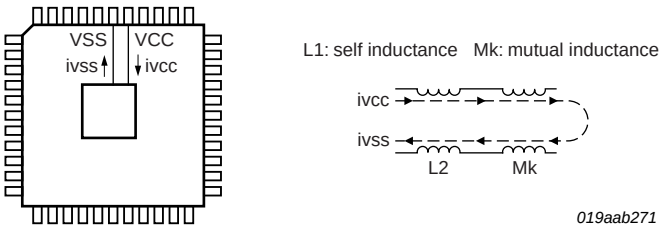
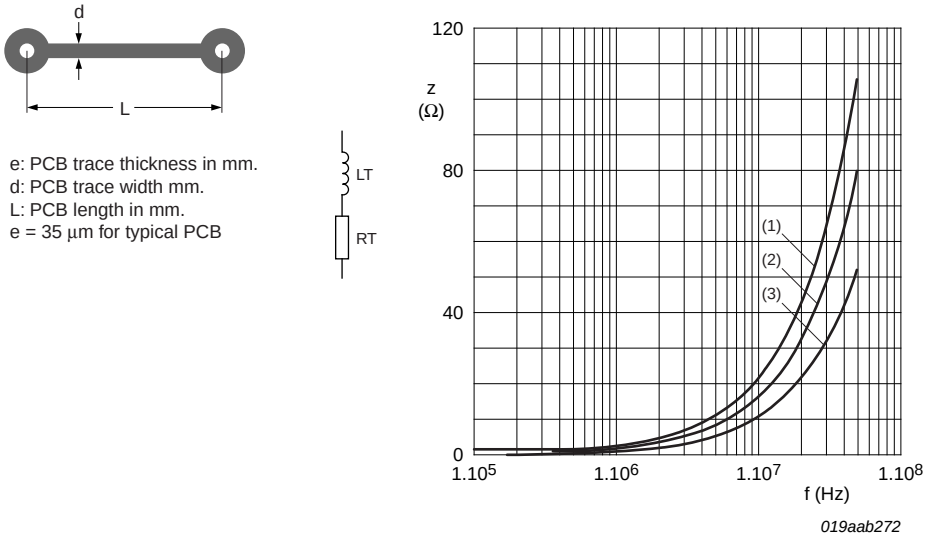


Fig 14. Ground and VCC pins close together can cancel the H field

5.5.4 Increasing the PCB connection widths

Realistically, a power-supply connection is not a pure short-circuit, but a trace with parasitic elements such as resistors and inductors.



(1) d = 0.1 mm
(2) d = 1 mm
(3) d = 1 cm

Fig 15. PCB trace model

This PCB trace is a complex impedance which varies with the frequency. Figure 15 shows the plot of the impedance versus the frequency for three different trace widths that have the same length of 10 cm and thickness of 36 µm. A PCB trace introduces voltage ripples and the width of PCB traces have to be large enough not to introduce a voltage drop which could be too high. For example, when a 0.1 A current at 30 MHz flows through a PCB trace with 10 cm length and 0.1 mm width, it causes a 0.62 V voltage drop. If the width is 1 cm (100 times the previous one), the voltage drop is reduced by a factor of two.

$$LT\ (\mu H) = 0.2 \times L \times \left[Ln\left(\left(\frac{2 \times L}{d+e}\right) + 0.5 + 0.22 \times \frac{d+e}{L}\right)\right] \quad (9)$$

$$RT\ (m\Omega) = 17 \times \frac{L}{d+e} \quad (10)$$

5.6 Reducing the parasitics of all devices

In addition to the magnetics fields that are a result of PCB traces, there are also a number of other parasitics such as ground impedances, capacitor serial resistances, inductor parasitic capacitances etc. There are a number of points that can improve EMC performance based on these parasitics.

5.6.1 Selecting the appropriate PCB technology

There are guidelines that determine the PCB technology to be applied at certain signal frequencies. Not complying with these guidelines will limit the possibilities for EMC reduction to a level where compliance is not possible without additional measures such as external shielding and additional filters. Table 1 shows which PCB technologies are commonly applied, depending on signal speed.

Table 1. PCB technology selection

Board type	Digital frequency	Signal rise/fall	Remarks
Single layer single-sided	<5 MHz	>6 nS	$10 \times F_{clock} = 1/(\pi \times T_{rise})$
Single layer double-sided Tracks on both sides	<10 MHz	>3 nS	realize ground grid
Single layer double-sided Ground plane on one side, wire jumpers	<20 Mhz	>1.5 nS	ground connectors/ICs
Single layer double-sided Ground plane on one side	<30 MHz	>1 nS	no long slots allowed in ground plane
Multilayer	-	-	-

5.6.2 Using the ground and power planes

Ground and power planes help to reduce parasitic inductance on the board thereby reducing inductive coupling. A ground or power plane will, however, increase the parasitic capacitance of tracks with high $^{dV}/_{dt}$, such as the drain of switching MOSFETs. Ground planes will reduce the ground lifting effect. A power plane must be adequately decoupled to ground in order to have a beneficial effect on EMC. Large uncoupled power planes will act as E-field radiator thereby worsening the EMC signature.

5.6.3 Grounding techniques

Due to stray currents in the ground circuit, there can be unwanted build-up of potential on other sensitive locations. This is referred to as “ground lifting”. To prevent ground lifting, a number of techniques can be applied, including the following:

- Do not route the signal trace return and power trace return over the same ground trace
- Separate the power ground and the signal ground [see Figure 16 (1)]
- Use the ground plane [see Figure 16 (2)]
- Apply a star configuration [see Figure 16 (3)]
- Use the ground bus [see Figure 16 (4)]

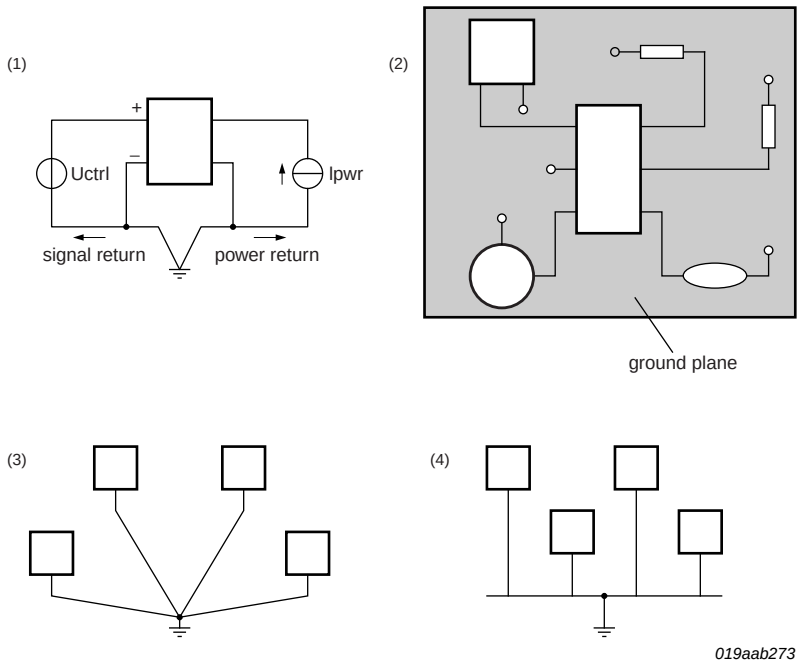


Fig 16. Grounding techniques

5.6.4 Adapting the decoupling capacitors to the working frequency of the converter

A capacitor is not pure, and can be modelled as an RLC circuit. Surface mounted devices (SMD) have the smallest internal and external inductances and this type must be selected to get the best results. Figure 17 shows the equivalent electrical model and plots the frequency response for a SMD 100 nF capacitor. The capacitor may act like a capacitor, a resistor or an inductor, depending on the frequency bands.

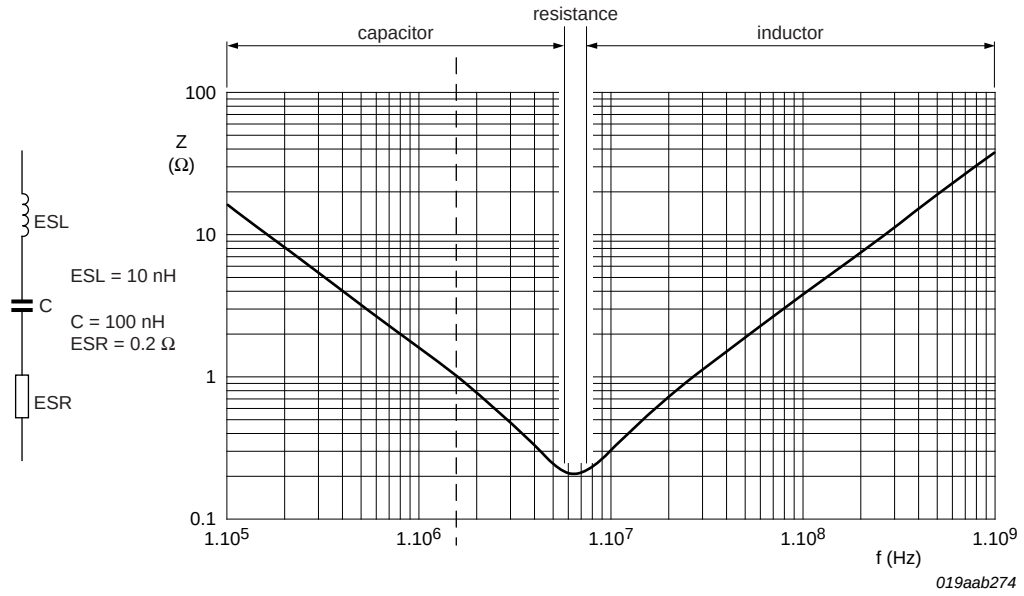


Fig 17. Self- resonance frequency of a real capacitor

The frequency behavior depends on the type of capacitor. Table 2 gives the electrical characteristics for different capacitors.

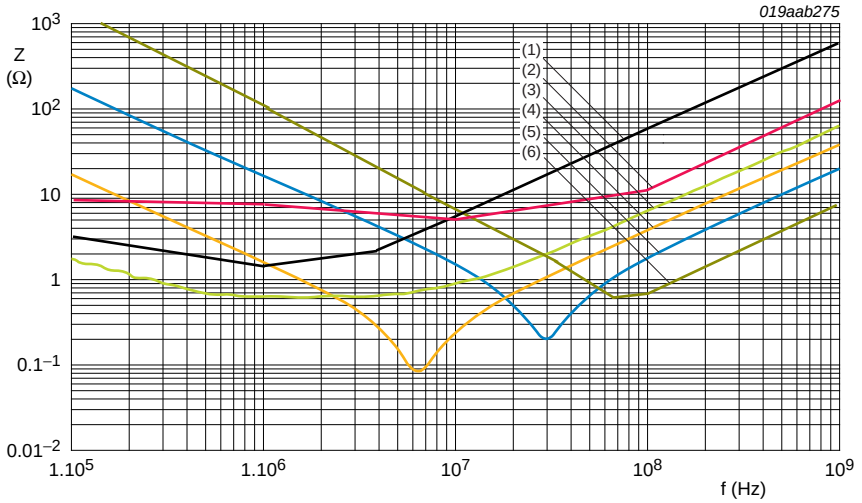
Table 2. Capacitor characteristics

Capacitor			Parameter		
Plot[1]	Value	Type	R (Ohm)	L (nH)	Fr (MHz)
1	1 μF	electrolytic	1.8	13	0.8[2]
2	10 μF	electrolytic	6.4	49	10[2]
3	1μF	tantalum	0.8	6	2[2]
4	100 nF	ceramic	0.08	3	7.1
5	10 nF	ceramic	0.2	3	29
6	1 nF	ceramic	0.7	3	22

[1] For the capacitor plots, refer to Figure 18

[2] Highly damped

Figure 18 shows the plots of the frequency response for different types of capacitors.

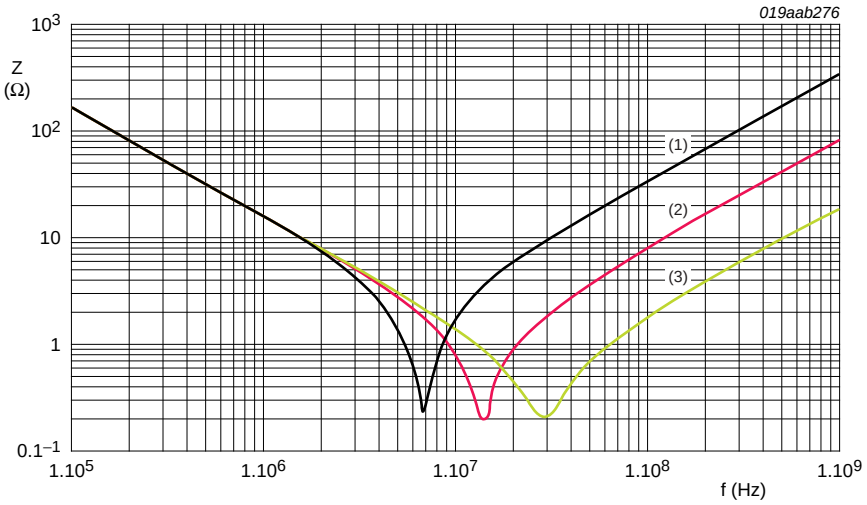


For details of the capacitor characteristics relating to the above plots, refer to Table 2

Fig 18. Impedance related to capacitor frequencies

5.6.5 Shortening the length of the capacitor connections

If the capacitor value is assumed to be constant, the resonance frequency depends on the inductance. The total inductance of the circuit consists of the intrinsic capacitor inductance and the inductance of the connections. A higher inductance value results in a lower resonance frequency. It is recommended to keep the length of the connections as short as possible.



(1) = l1

(2) = l2

(3) = l3

Note: l3 < l2 < l1

Fig 19. Impact of connection length from decoupling capacitor

5.6.6 Selecting suitable COG and NPO dielectric capacitor types

When selecting capacitors, the dielectric material determines ESR and subsequently the filtering function. Capacitors utilizing these dielectrics have the lowest ESR, good temperature stability and cover a wide range of values from low to high nF. Additional information relating to class I dielectrics can be found in Section 7.1.1 “Class I dielectrics”.

5.6.7 Selecting suitable by-pass electrolytic capacitors

Table 2 and Figure 18 demonstrate how electrolytic capacitors tend to have an ESR that is substantially higher than ceramic capacitors. A high ESR gives the following effects:

- It lowers effective damping of a filter at high frequency
- It increases dissipation within the components, causing self-heating, higher operating temperature and decreased lifetime of the electrolytic capacitor
- It dissipates high frequency energy in the system

The first two aspects are undesirable, but the last aspect can be exploited to reduce the EMC signature. If the electrolytic capacitor is placed parallel to a ceramic capacitor, the resulting ESR will be less. Care should be taken to position the bypassing capacitor towards the noise source, because trace inductances would otherwise hamper functionality.

5.6.8 Adapting the inductors to the working frequency of the converter

A situation similar to that mentioned in Section 5.6.4 for capacitors, is also valid for inductors. The inductor can be modeled using a series resistor Rs and a parallel capacitor Cp, resulting in a different network with an impedance curve. Figure 20 plots the inductance of a 4.7 mH Toko inductor. It has a resonance frequency at 979 kHz, a series resistor of 26 Ω and a parallel capacitance of 5.5 pF. Again, three frequency bands can be seen as follows:

- Low frequency band: 0 Hz to 980 kHz - the inductor is a combination of inductance and DC resistance
- Resonance frequency: 980 kHz - the inductor is an isolator (545 kΩ)
- Medium frequency: > 980 kHz - the inductor acts as a pure capacitance

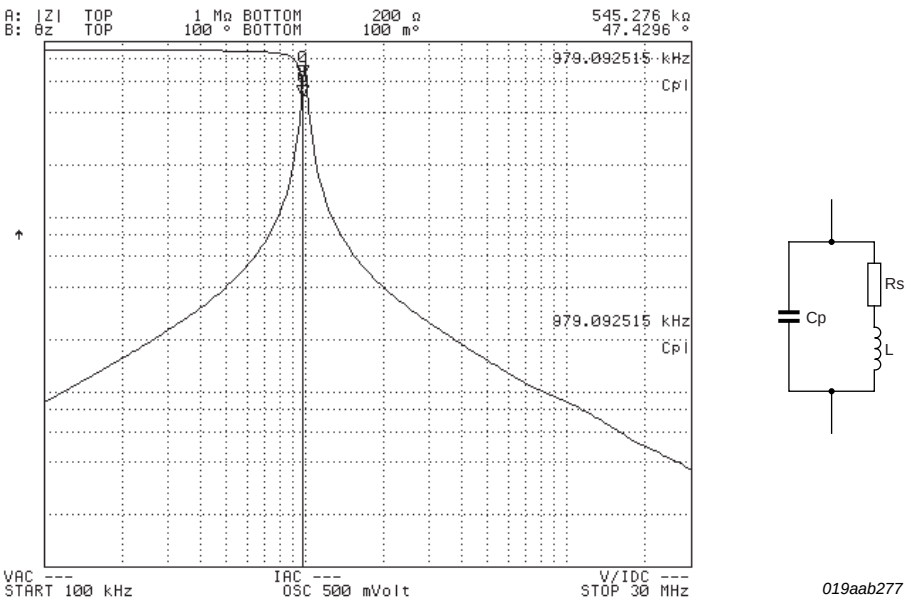


Fig 20. Self resonance frequency of real inductor

Figure 20, shows that this inductor will not be applicable at frequencies above 980 kHz. As a comparison, in Figure 21 a 68 μH inductor and a 100 E ferrite bead are plotted. Notice that the ferrite bead displays resistive behavior that increases logarithmically with frequency. A ferrite bead has a completely different functionality compared to an inductor, it will dampen high frequency signals. The 68 μH inductor has a self resonance frequency at 8.35 MHz and can be used to filter frequencies higher than the 4.7 mH inductor can. The ferrite bead can be used up to 30 MHz, and has little effect at low frequencies such as 10 kHz. It should be stated that the desired impedance is achieved only when the inductor is operated within the specifications. An inductor that reaches saturation looses its functionality and will not posses its original value at all. This situation often happens with inrush currents or repetitive peak currents.

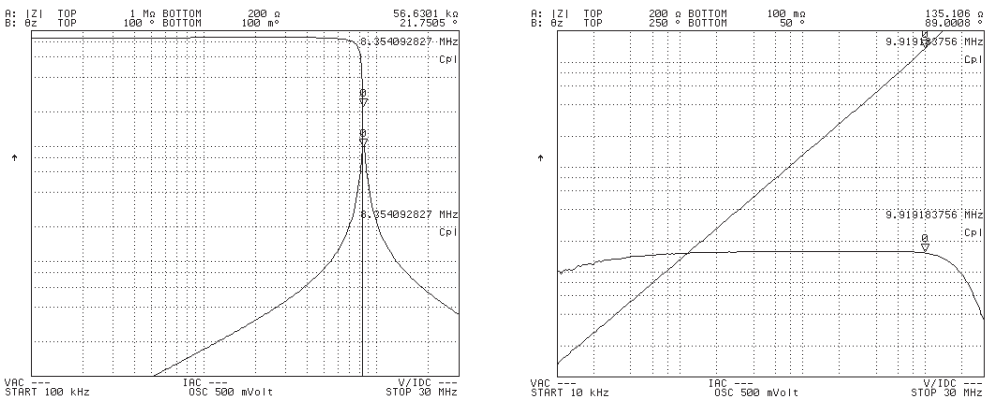


Fig 21. Impedance characteristic of 68 μH inductor and 100 E ferrite bead

5.6.9 Prevention of mutual coupling between the inductors

Inductors and transformers have stray magnetic fields that affect the surroundings. When two inductors are placed in close proximity, the stray magnetic field of one inductor will induce a voltage over the other. This can bypass filter function.

The following three measures are employed to prevent this:

- Increase the distance between the inductors. In the near field, the H-field will decrease with $\frac{1}{3}$ rd power of distance. Doubling the distance will reduce the induced voltage to $\frac{1}{9}$ th.
- Set the inductor's perpendicular. If the directions of the magnetic fields do not coincide, mutual inductance is reduced.
- Use shielded inductors. Shielded inductors have less stray field

5.6.10 Increase the distance

Both capacitive and inductive coupling are influenced by the distance between source and victim. Increasing the distance will reduce the risk of the unwanted bypassing of filter networks or crosstalk. See Figure 22

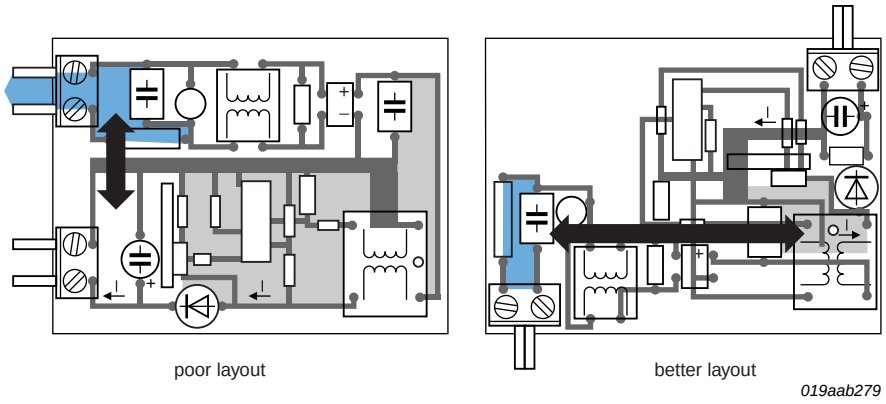


Fig 22. Examples of EMC layouts showing high risk and improved crosstalk configurations

5.7 Frequency domain analysis

When EMC problems are analyzed, it is often possible to find a link between the problems and the solution by looking at the frequency band. If a converter operates at 100 kHz, harmonics will occur at 200 kHz, 300 kHz etc. A signal at 5 MHz will not be caused by the converter harmonics, but more likely as the result of ringing or steep switching flanks.

5.7.1 Differential and common mode noise

For conducted emission, two modes are classified:

- **Differential mode** - noise is conducted on the signal (L) line and neutral (N) line in the opposite direction to each other. This type of noise is suppressed by installing a filter on the hot (VCC) side on the signal line or power supply line, as mentioned in the preceding chapter
- **Common mode** - noise appears equally (with respect to local circuit common) on both lines of a 2-wire cable not connected to earth, shield, or local common. Common mode noise can be suppressed either by using a coupled inductor in the signal path over both lines, or by using shielding with capacitive grounding

Figure 23 and Figure 24 show the resultant signals.

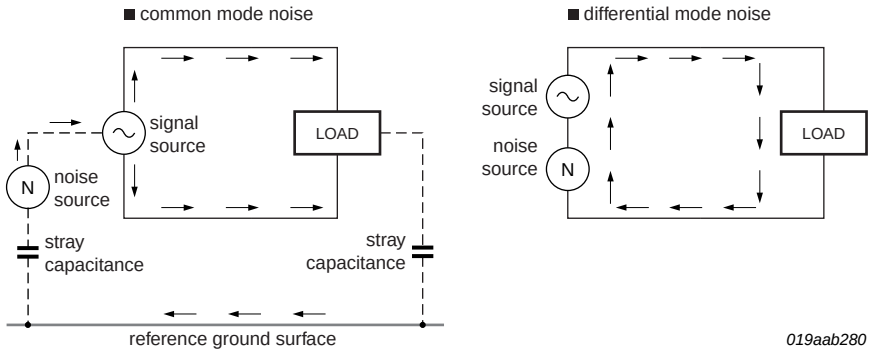


Fig 23. Common mode and differential mode currents

During EMI testing, it is possible to detect whether there is common mode or differential mode noise. With this information, the appropriate countermeasures can be taken.

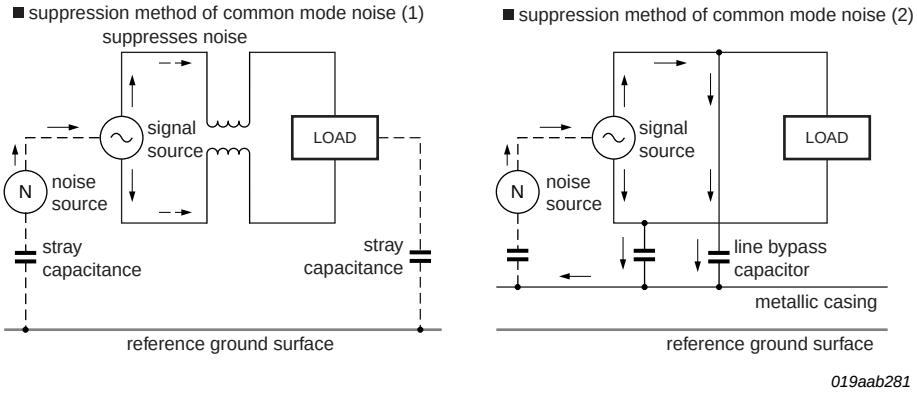


Fig 24. Common mode filtering methods

As common mode noise can be caused by stray capacitance to ground, it can be seen as frequency dependent. The reactance of a capacitor is calculated using Equation 11.

$$X_c = \frac{1}{-j \times \omega \times C} \tag{11}$$

Where $\omega = 2 \times \pi \times f$.
If the impedance is estimated to be equal to 100 Ω (line impedance), and the stray capacitance at 10 pF, the cut-off frequency is calculated using Equation 12.

$$f = \frac{1}{2 \times \pi \times 100 \times 10\mathrm{E}-12} = 159\ MHz \tag{12}$$

This is obviously a high frequency phenomenon. However, low frequency conducted emission is more likely differential mode by nature, and can best be filtered with a differential mode filter such as a symmetrical π filter.

5.7.2 X and Y type capacitors

A line-to-line capacitor (designated as type X) properly applied is effective for differential mode filtering. A line to ground capacitor (type Y) provides filtering for common mode noise. While X capacitor may be of any practical value, Y capacitors generally need to be kept to small values to limit the 50 Hz to 60 Hz leakage current to ground. A typical value for a Y capacitor is 4700 pF. Common X capacitor values are from 0.1 μF up to1.0 μF. Sometimes even higher values are required depending on the interference frequencies. Improved printed-circuit layout practices will result in smaller capacitor values being required. Also, two X capacitors of smaller value are generally better, especially in the π-configuration with a choke.

Due to their placement on the AC line, a failed RFI suppression capacitor is capable of causing injury either by shock or fire. The problem is exacerbated by conditions on the line. The line conducts voltage surges and transients on a daily basis and these often attain amplitudes of several kilovolts. Because of the potential for injury the various safety agencies provide testing and recognition for X and Y capacitors. The European standard for RFI capacitors (IEC384-14) is EN132400. The USA standard is UL1414.

5.7.3 Damping any unwanted HF signals

HF noise is often caused by resonance of a particular circuit. This resonance is typical for an LC combination without load. Because there is a short wavelength and steep dV/dt, these signals are much more prone to parasitic coupling and radiation to the surroundings. Filtering will increase impedance of the resonant circuit. This will in turn increase the amplitude of the resonance and increase leakage into parasitics. As a result, the noise will find another way to leak. It is therefore necessary to damp these signals. This can be achieved by either using parallel damping with a resistor and capacitor in series, serial damping using a ferrite bead, or a combination of the two. The combination of filtering and damping will isolate the signal and provide better power transfer to the damping element. Figure 25 shows this process.

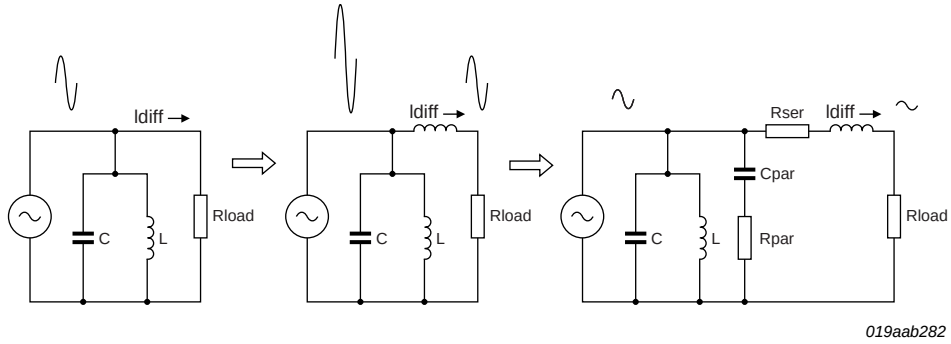


Fig 25. HF damping process

5.8 Shielding

5.8.1 Mount the hot windings at the inner layer

The outer windings of inductors and transformers can act as a shield when connected to a stable potential. This is capacitive shielding as the area having most dV/dt is covered by conductive material. Although the dot shown in Figure 26 only indicates current flow and winding direction, it is also often interpreted as the location of the first winding (see Figure 26).

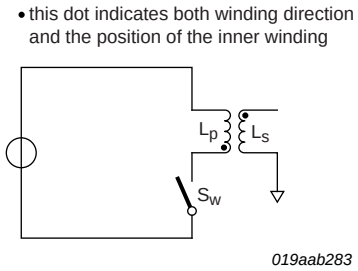


Fig 26. Hot windings at inner layer

5.8.2 Attach a heatsink to the clean potential

Heat-sinks distribute heat away from dissipative elements. In SMPS systems, these dissipative element are usually the components that carry high currents and voltages, switches for example. Because of the close proximity of the heat-sinks to these devices, capacitive coupling always occurs. This results in the complete heat-sink becoming a capacitive radiator to its surroundings. This is particularly evident where common mode noise is present. It is therefore recommended that heat-sinks are connected either directly to a clean potential, such as a clean ground signal, or the use of a decoupling capacitor to conduct noise toward a clean potential.

5.8.3 Use the component material and heatsink as a shield

Some components, including grounded heat-sinks, can act as shielding for capacitive conducted noise. One of the constructional methods often encountered in power supplies, is the use of a heatsink to disperse heat, act as shield and also to provide a mechanical housing. Because the functionality is combined, it is an economical solution. Another

option would be to use components, such as decoupling capacitors, in such a way that they are positioned between the noise source and the victim. The internal conductive material acts as a shield again. The outer area of the component must be connected to a clean potential.

5.8.4 Using capacitive shielding

To reduce parasitic coupling to susceptible lines, capacitive shielding can be implemented by putting a trace with fixed potential between the lines. A fixed clean potential, such as a ground, is essential for this. Conductive material that is not connected, gives a larger resultant capacitance and therefore more parasitic coupling, which will make the problem worse.

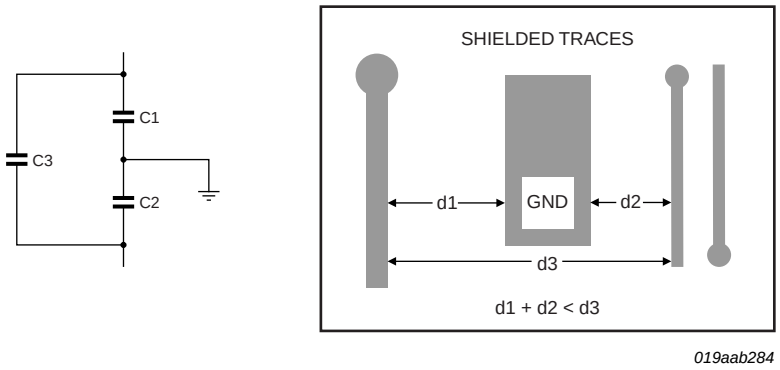


Fig 27. Capacitive shielding

5.8.5 De-couple other floating potentials

It is usual to de-couple other floating potentials, such as a metal housing, towards a clean fixed potential, such as the mains neutral or safety earth. This avoids capacitive coupling towards the surroundings that will generate a common mode noise conductive path. If this decoupling is done over a safety barrier, (isolation between mains and a low voltage secondary side of the SMPS), the decoupling capacitor should be selected to withstand the required voltage. Type Y capacitors have been approved for this purpose. Care should be taken that 50 Hz to 60 Hz leakage current to ground is not exceeded, by combining multiple type Y capacitors.

6. Conclusion

Most of the EMC improvements detailed in this application note are already known but not always applied. There is not one specific solution for improving the EMC of a system, but a number of individual precautions contribute to a cumulative improvement. Designers must keep in mind these mechanisms, and apply them early in the conceptual phase of a system to ensure EMC compliance. The more that these considerations and countermeasures are used during early design stages, the more that cost and effort will be reduced and delays prevented during more final development stages.

7. Additional information

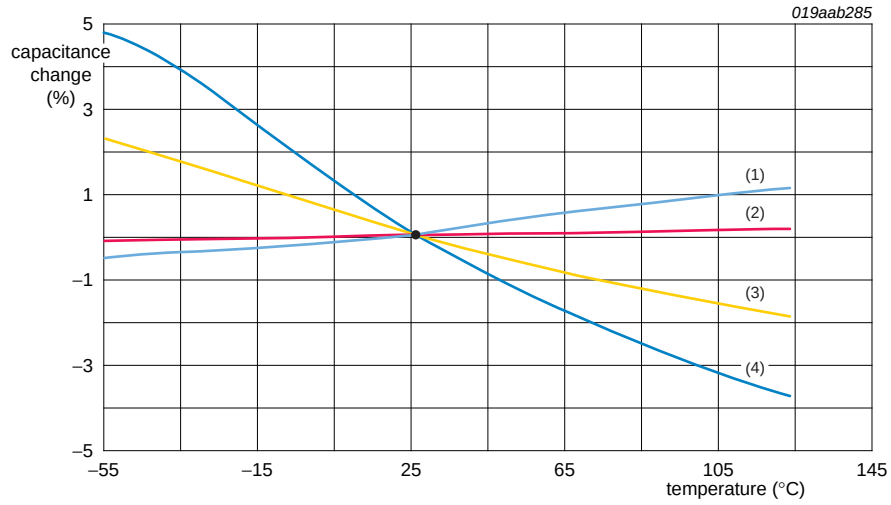
7.1 Industry ceramic capacitor markings

7.1.1 Class I dielectrics

The electronics industry has defined several classes of ceramic dielectric capacitors. Class I ceramics have dielectric constants below 150, and are the most stable ceramic capacitors. The basic ceramic is the para-electric oxide TiO2. By adding small amounts of ferro-electric oxides such as CaTiO3 or SrTiO, extended temperature compensating ceramics are created.

These ceramics have linear and predictable temperature characteristics and dielectric constants up to approximately 500. Class I dielectric capacitors have typical tolerances of 5 % and values within the range 4.7 pF to 0.047 μF. Their capacitance is highly stable over time, and they have a small dissipation factor over a wide range of frequencies. Figure 28 shows the typical variation in capacitance for a selection of Class 1 ceramic capacitors.

The variation in capacitance with temperature is clearly not perfectly linear, but close enough so that a linear approximation is reasonable and a temperature coefficient can be defined.



(1) P100
(2) NPO
(3) N220
(4) N470

Fig 28. Typical temperature characteristics of selected Class 1 ceramic capacitors

The unofficial, colloquial temperature coefficient designations for the capacitors are indicated in Figure 28. The temperature coefficient is given as “P” for positive, “N”, for negative, followed by a 3-digit value of the temperature coefficient in ppm/°C. For example “N220”, is -200 ppm/°C, and “P100” is +100 ppm/°C. The one exception to this system is “NPO” (where an “O” instead of “0” is used) which means stable with temperature.

7.1.2 EIA capacitor codes

The EIA three character code, for the material capacitance/temperature slope, is derived from the high and low temperature limits, and the range of capacitance change.

Table 3. EIA codes

ppm/°C	Multiplier	Tolerance in ppm/°C (25°C to 85°C)
C: 0.0	0: –1	G: ±30
B: 0.3	1: –10	H: ±60
L: 0.8	2: –100	J: ±120
A: 0.9	3: –1000	K: ±250
M: 1.0	4: +1	L: ±500
P: 1.5	6: +10	M: ±1000
R: 2.2	7: +100	N: ±2500
S: 3.3	8: +1000	
T: 4.7		
V: 5.6		
U: 7.5		

7.1.3 dB and mV

During EMC measurements, the interference level is often expressed in dBμV. The relation is expressed in Equation 13. Equation 14 and Equation 15

$$U\,(dB\mu V) = 20 \times {}^{10}\log U(\mu V) \tag{13}$$

$$120\,(dB\mu V) = 10^{6}\ \mu V = 1\ V \tag{14}$$

$$U\,(\mu V) = 10^{\frac{dB\mu V}{20}} \tag{15}$$

The advantages of this are as follows:

- Small numbers with many orders of magnitudes
- Divisions become subtractions
- Multiplications become additions

8. Abbreviations

Table 4. Abbreviations

Acronym	Description
PCB	Printed-Circuit Board
ESR	Equivalent Series Resistor
HF	High Frequency
AC	Alternating Current
RFI	Radio Frequency Interference
SMD	Surface Mounted Device

9. Glossary

SMPS ? Switch Mode Power Supply

EMC ? ElectroMagnetic Compatibility: the ability of a product to coexist in its intended electromagnetic environment without causing or suffering functional degradation or damage.

EMI ? ElectroMagnetic Interference: a process by which disruptive electromagnetic energy is transmitted from one electronic device to another via radiated or conducted paths (or both).

Radiated emission ? Energy transmitted by the air via antenna or loops.

Conducted emission ? Energy transmitted via solid medium cables, PCB connections, packages etc.

Noise source ? A source that generates an electromagnetic perturbation.

Victim ? An electronic device that receives a perturbation which causes dysfunction.

Coupling path ? A medium that transmits energy from the noise source to the victim.

COG ? EIA three character code for the material capacitance-temperature slope.

NPO ? Industry code for capacitor material with lowest temperature coefficient.