SY22650B

Single-Stage Flyback and PFC Controller with CV Control

General Description

The SY22650B is a single-stage flyback and PFC controller designed for constant voltage (CV) applications. It uses primary-side control to reduce the total solution cost, constant on-time control to achieve a high power factor, and drives the flyback converter in quasi-resonant mode for high efficiency. The device also employs adaptive PWM/PFM control for improved light-load efficiency.

The SY22650B provides reliable protections including short-circuit protection (SCP), open-LED protection (OLP), overtemperature protection (OTP), transformer shorted protection, and power diode shorted protection.

The SY22650B is available in a compact SO8 package.

Features

- 9V to 22V Input Voltage Range
- 0.45mA (typ.) Quiescent Current I_Q
- Primary-Side Constant Voltage Control Eliminates the Optocoupler
- Valley Turn-On of the Primary MOSFET for Low Switching Losses
- Internal High Current MOSFET Driver: 0.1A Sourcing and 0.5A Sinking
- Power Factor >0.90 with Single-Stage Conversion
- 100kHz Maximum Switching Frequency
- Quick Startup: <500ms
- Output Current Limit of Approximately 1.2x the Rated Current
- RoHS-Compliant and Halogen-Free
- Compact Package: SO8

Applications

- AC/DC Adapters
- Battery Chargers
- LED Lighting

Typical Application

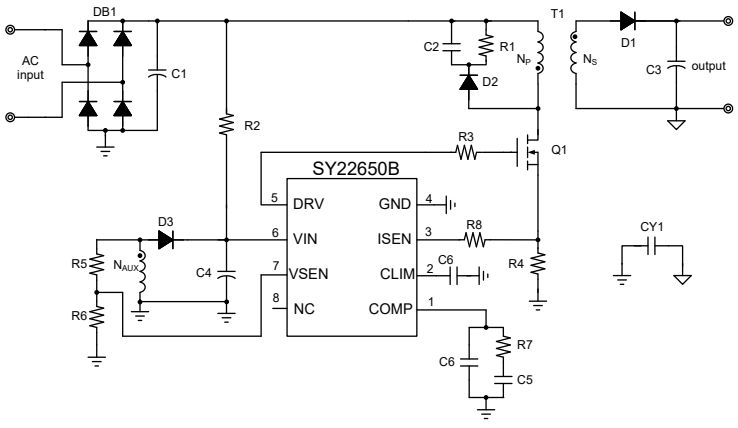


Figure 1. Schematic Diagram

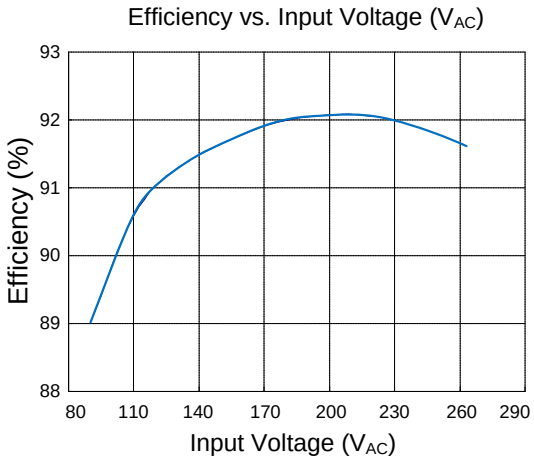


Figure 2. Efficiency vs. Load Current

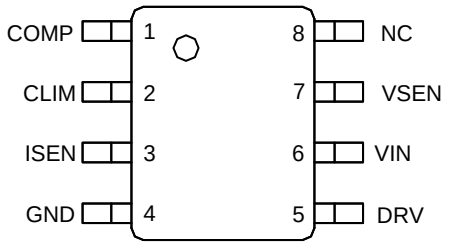
Ordering Information

SY22650 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Part Number	Package Type	Top Mark
SY22650BFAC	SO8 RoHS-Compliant and Halogen-Free	***BEVxyz***

x = year code, y = week code, z = lot number code

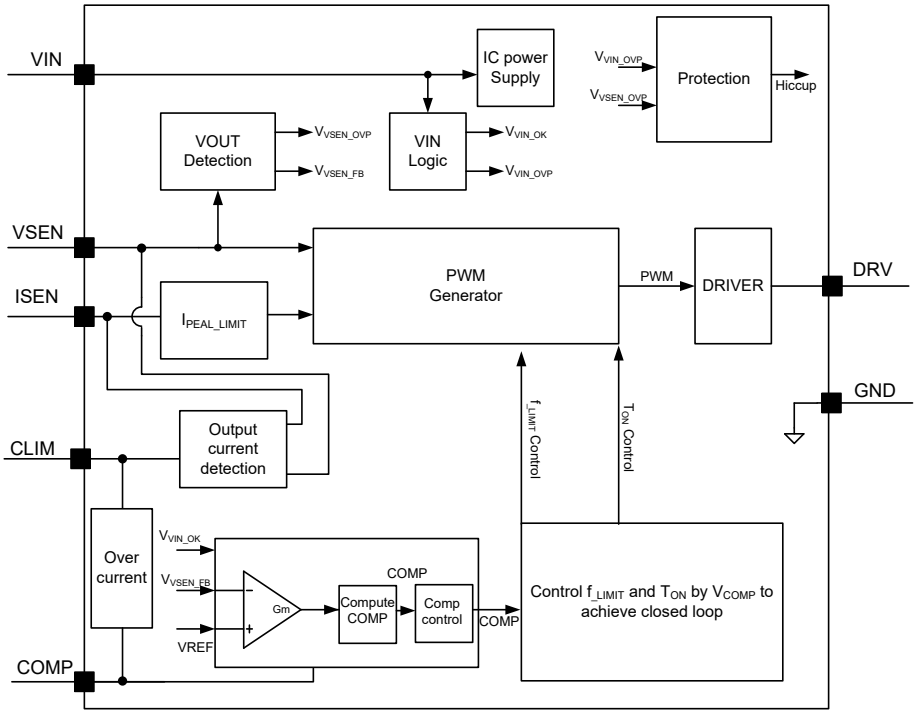
Pinout (top view)



Pin Description

Pin Number	Pin Name	Pin Description
1	COMP	Loop compensation pin. Connect an RC network between this pin and ground.
2	C_{LIM}	Current limit pin. Add a 220nF ceramic capacitor to GND; output current will be limited to approximately 1.2x the rated current. If this function is not needed, connect the CLIM pin to GND.
3	I_{SEN}	Current limit pin
4	GND	Ground pin
5	DRV	Gate driver pin. Connect this pin to the gate of primary MOSFET with a resistor.
6	V_{IN}	Power supply pin.
7	V_{SEN}	Output voltage and inductor current zero detection. This pin receives the auxiliary winding voltage through a resistor divider.

Functional Block Diagram



Absolute Maximum Ratings

Parameter (Note 1)	Min	Typ	Max	Unit
V_{IN}, DRV	-0.3		36	V
V_{SEN}	-0.3		V_{IN} + 0.3V	
I_{SEN}, COMP, C_{LIM}		3.6		
Supply Current I_{VIN}		20		mA
Lead Temperature (Soldering, 10 sec.)			260	°C
Junction Temperature, Operating	-40		150	
Storage Temperature	-65		150	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	88	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	45	
P_D Power Dissipation T_A = 25°C	1.1	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
V_{IN}, DRV	9	22	V
Junction Temperature, Operating	-40	125	°C

Electrical Characteristics

(V_{OUT} = 12V (Note 3), T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{VIN}		9		22	V
V_{IN} Turn-On Threshold	V_{VIN_ON}		18.5	21.5	23.5	V
V_{IN} Turn-Off Threshold	V_{VIN_OFF}		6.5	7.5	8.5	V
V_{IN} OVP voltage	V_{VIN_OVP}		22	24.5	27	V
Startup Current	I_{ST}	$V_{VIN} < V_{VIN\_OFF}$	0.75	1.85	3	μA
Quiescent Current	I_Q		0.3	0.45	0.6	mA
Shunt Current in OVP Mode	I_{VIN_OVP}	$V_{VIN} > V_{VIN\_OVP}$		15		mA
Current Limit Voltage	V_{ISEN_LIMIT}	1.0V > V_{SEN} > 0.2V	0.9	1.0	1.1	V
Protect Current Limit Voltage	V_{ISEN_OCP}		1.2	1.5	1.8	V
V_{FB} at Fast Startup	V_{FB_LOW}		1.04	1.10	1.14	V
Internal Reference Voltage	V_{REF}		1.225	1.250	1.275	V
Threshold Value of Maximum V_{FB}	V_{FB_HIGH}		1.33	1.40	1.45	V
OVP Voltage Threshold	V_{FB_OVP}			V_{FB_HIGH} + 0.1		V
Blanking Time for Off-Time	t_{OFF_MIN1}	V_{ISEN_HOLD} = 0.15V	1.4	1.7	2.1	μs
	t_{OFF_MIN2}	V_{ISEN_HOLD} = 0.40V	1.9	2.6	3.4	μs
Gate Driver Voltage	V_{GATE}		10	12	13.5	V
Typical Source Current	I_{SOURCE}		60	75	90	mA
Typical Sink Current	I_{SINK}		300	400	500	mA
Maximum On-Time	t_{ON_MAX}	V_{COMP} = 2.5V	6.5	10	13.5	μs
Minimum On-Time	t_{ON_MIN}		0.15	0.3	0.45	μs
Maximum Switching Frequency	f_{MAX}		75	100	125	kHz
Output Current Limit	V_{CLIM}		0.30	0.33	0.36	V
Thermal Shutdown Temperature	T_{SD}			155		°C

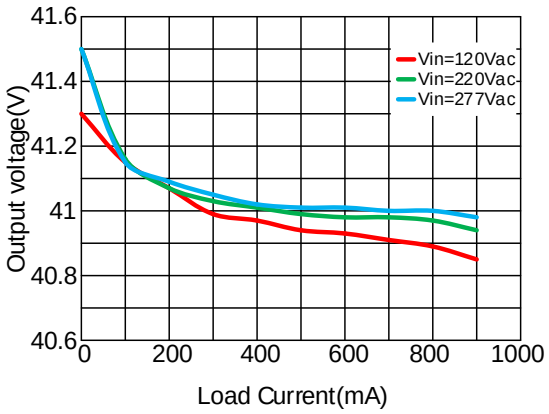
Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2” x 2” FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

Note 3: Increase V_{IN} pin voltage gradually higher than $V_{VIN,ON}$ voltage then turn down to 12V.

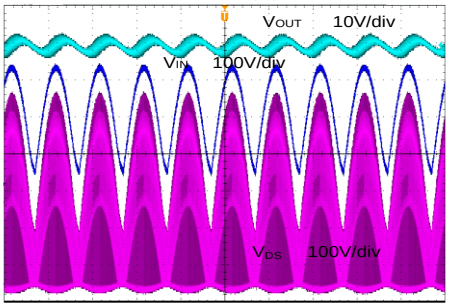
Typical Performance Characteristics

Load Regulation



Steady State

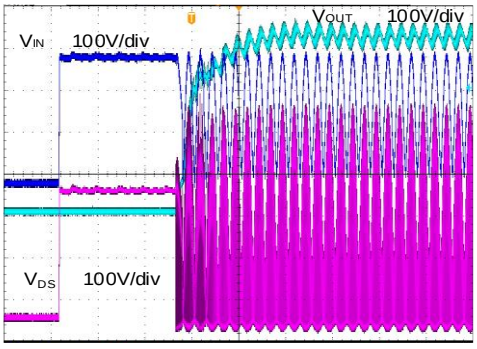
(V_{IN}=220$V_{(AC)}$)



Time (10ms/div)

Startup

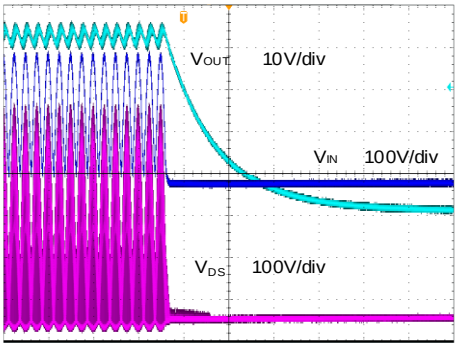
(V_{IN}=220$V_{(AC)}$)



Time (40ms/div)

Shutdown

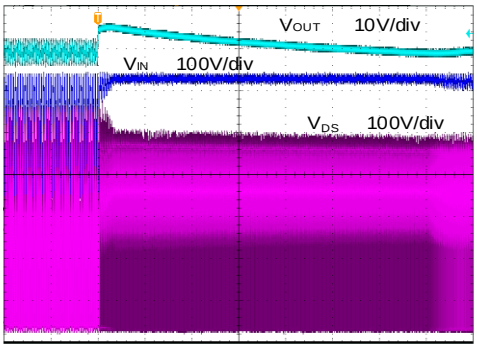
(V_{IN}=220$V_{(AC)}$)



Time (40ms/div)

Open Load Protection

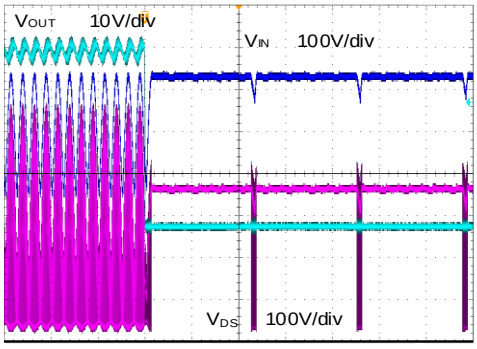
(V_{IN}=220$V_{(AC)}$)



Time (200ms/div)

Short Circuit Protection

(V_{IN}=220$V_{(AC)}$)



Time (40ms/div)

Operation

The SY22650B is a single-stage flyback and PFC controller designed for constant voltage (CV) applications. It uses primary-side control to eliminate optocouplers and reduce feedback circuit cost, and constant on-time control to achieve a high-power factor.

In order to reduce switching losses and improve EMI performance, the SY22650B uses quasi-resonant switching mode, in which the power MOSFET is turned on at the voltage valley. The relatively small (5μA typ.) startup current further reduces the standby power loss. The maximum switching frequency is clamped to 100kHz to reduce switching losses and improve EMI performance. The SY22650B is specifically designed to ensure good transition performance, and it also employs adaptive PWM/PFM control for improved average efficiency.

The SY22650B startup process is optimized internally, and quick startup (<500ms) is achieved with no additional circuits.

The SY22650B provides reliable protections including short-circuit protection (SCP), open-LED protection (OLP), overtemperature protection (OTP), transformer shorted protection, and power diode shorted protection.

The SY22650B is available in an SO8 package.

Application Information

Quick Startup

After the AC supply or DC bus is powered on, capacitor C_{VIN} (across the V_{IN} and GND pins) is charged up by bus voltage through the startup resistor R_{ST}. When V_{VIN} rises above $V_{VIN,ON}$, the internal blocks turn on and the PWM output is enabled.

The output voltage is fed back through the V_{SEN} pin, which is used as feedback control signal, V_{FB}. If V_{FB} is lower than the threshold $V_{FB,LOW}$, which means that the output voltage didn't reach the target, V_{COMP} is pulled up and clamped high; if V_{FB} is higher than $V_{FB,LOW}$, V_{COMP} is controlled by the internal gain modulator.

This operation is aimed to build up enough output voltage for auxiliary winding bias supply as quickly as possible. It is enabled only one time, when V_{VIN} is greater than $V_{VIN,ON}$.

V_{COMP} is pre-charged by an internal current source to $V_{COMP,IC}$ and held at this level until the quick startup process is complete.

The startup resistor R_{ST} and capacitor C_{VIN} are selected using the following steps:

1. Ensure that the current through R_{ST} is larger than I_{ST} and smaller than I_{VIN_OVP}:

$$\frac{V_{BUS}}{I_{VIN\_OVP}} < R_{ST} < \frac{V_{BUS}}{I_{ST}}$$

   where V_{BUS} is the bus line voltage.

2. Select C_{VIN} to obtain a desired startup time t_{ST}, and ensure the output voltage can ramp up to the target voltage during this time.

$$C_{VIN} = \frac{(\frac{V_{BUS}}{R_{ST}} - I_{ST}) \times t_{ST}}{V_{VIN\_ON}}$$

3. If C_{VIN} is too small to build up the output voltage, increase C_{VIN} and decrease R_{ST}, then repeat the design from Step 1 until an optimal startup sequence is obtained.

4. When $V_{FB} < 0.2V$, V_{ISEN} will be limited to 0.4V. When $1.0V \geq V_{FB} \geq 0.2V$, V_{ISEN} will be limited to 1.0V.

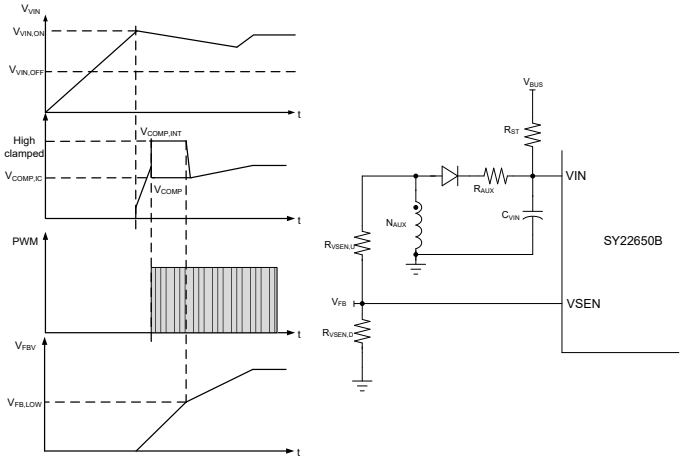


Figure 3. Startup

Shutdown

After the AC supply or DC bus is powered off, the energy stored in the bus capacitor will be discharged. When the auxiliary winding of the flyback transformer cannot supply enough energy to the V_{IN} pin, V_{VIN} will drop. Once V_{VIN} is below $V_{VIN,OFF}$, the device will stop working and V_{COMP} will be discharged to zero.

Quasi-Resonant (QR) Operation

QR operation provides low turn-on switching losses for the flyback converter. The voltage across the drain and source of the primary MOSFET is reflected by the auxiliary winding of the flyback transformer. The V_{SEN} pin detects the voltage across the auxiliary winding through a resistor divider. The MOSFET is turned on when the voltage across the drain and source of the primary MOSFET is in a valley.

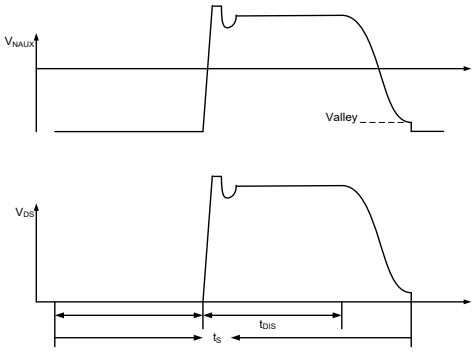


Figure 4. QR Operation

Output Voltage Control

In order to achieve primary-side constant voltage control, the output voltage is monitored using the auxiliary winding voltage.

As shown in Figure 5, the voltage across the auxiliary winding during off-time is:

$$V_{AUX} = (V_{OUT} + V_{D,F}) \times \frac{N_{AUX}}{N_S}$$

where N_{AUX} is the number of turns of auxiliary winding; N_S is the number of turns of secondary winding; $V_{D,F}$ is the forward voltage of the power diode.

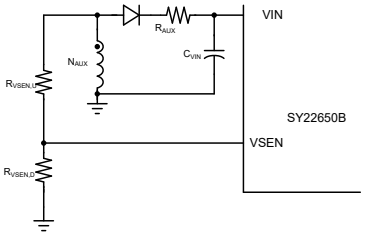


Figure 5. V_{SEN} Pin Connection

At the current zero-crossing point, $V_{D,F}$ is nearly zero, so V_{OUT} is directly proportional to V_{AUX}. The voltage at this time is sampled by the IC as the output voltage feedback. The resistor divider is designed using the following equation:

$$V_{OUT} = \frac{V_{REF}}{\frac{R_{VSEN,D}}{R_{VSEN,U} + R_{VSEN,D}} \times \frac{N_{AUX}}{N_S}}$$

where V_{REF} is the internal voltage reference.

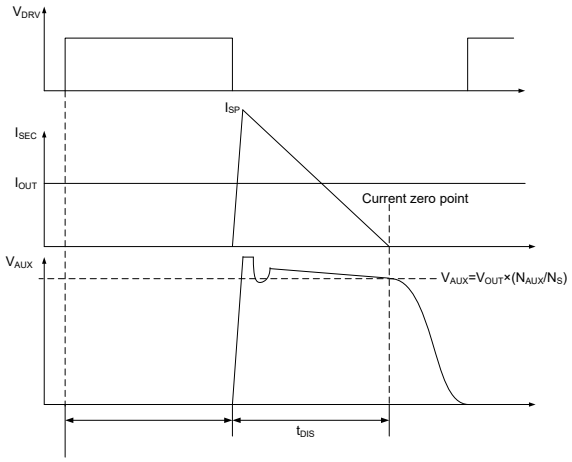


Figure 6. Auxiliary Winding Voltage Waveforms

Output Current Limit

Capacitor C_{LIM} limits the maximum output current. When setting $V_{ISEN} \approx 0.9V$ at minimum input voltage and full load, the output current will be limited to approximately 1.2x the rated current.

$$I_{OUT} = \frac{I_{PEAK} \times N_P \times T_{DIS}}{2 \times N_S \times T_S}$$

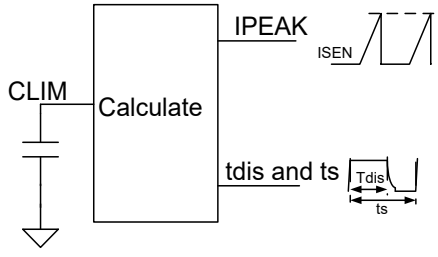


Figure 7. Current Sense

Load Transient Performance

The SY22650B is specifically designed to ensure good load transient performance.

When V_{SEN} reaches $V_{FB,HIGH}$, the IC operates in maximum t_{OFF} (Typ.=500us)mode to decrease the output energy, and COMP is pulled down to decrease the energy output, as shown in Figure 8.

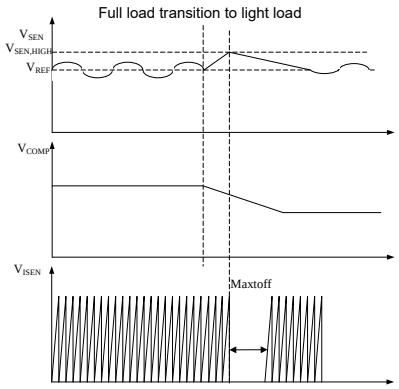


Figure 8. Full Load Transition to Light Load

When V_{SEN} reaches $V_{FB,LOW}$, the IC operates in maximum I_{PEAK} mode (V_{ISEN_LIMIT}) to increase output energy, and COMP is charged to increase the energy output, as shown in Figure 9.

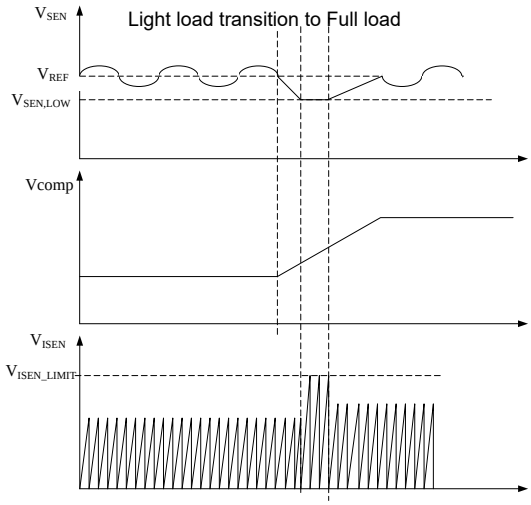


Figure 9. Light Load Transition to Full Load

R_{ISEN} Design

The maximum power inductor current ($I_{P\_PK\_MAX}$) occurs at minimum input voltage under full load. Select R_{ISEN} as follows:

$$R_{ISEN} = \frac{90\% \times V_{ISEN,LIMIT}}{I_{P\_PK\_MAX}}$$

where $V_{ISEN,LIMIT}$ protects the transformer (if V_{ISEN} reaches this voltage, the gate will turn off), and $I_{P\_PK\_MAX}$ is the maximum current in steady state.

Short-Circuit Protection (SCP)

When the output is shorted to ground, the output voltage is clamped to zero. The voltage of the auxiliary winding is proportional to the output winding, so the valley signal cannot be detected by V_{SEN}. Without valley detection, the MOSFET cannot be turned on until the maximum off-time $t_{OFF,MAX}$ (64us Typ.) expires. If the MOSFET is turned on by $t_{OFF,MAX}$ 64 times consecutively, the device will enter hiccup mode.

The hiccup time is determined by the parameters in Figure 1:

$$t_{hiccup} \approx \frac{(V_{VIN\_ON} - V_{VIN\_OFF}) \times C_{VIN}}{\frac{V_{BUS}}{R_{ST}} - I_{ST}}$$

Single-Fault Design

If the V_{SEN} pin is shorted to the GND pin or floating, the valley signal cannot be detected, which is similar to SCP. If this occurs, the system will operate in hiccup mode.

If the transformer is shorted, V_{ISEN} will exceed V_{ISEN_OCP}, which will also trigger hiccup mode operation. This also protects against a secondary diode short.

Power Devices Design

MOSFET and Diode

The MOSFET and secondary power diode have to be rated to sustain the applied voltage when operating with maximum input voltage under full load, as shown by the following equations:

$$V_{MOS\_DS\_MAX} = \sqrt{2}V_{AC\_MAX} + N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S$$

$$V_{D\_R\_MAX} = \frac{\sqrt{2}V_{AC\_MAX}}{N_{PS}} + V_{OUT}$$

where $V_{AC,MAX}$ is the maximum input AC RMS voltage; N_{PS} is the turns ratio of the flyback transformer; V_{OUT} is the rated

output voltage; $V_{D,F}$ is the forward voltage of secondary power diode; ΔV_S is the overshoot voltage clamped by the RCD snubber during off-time.

The current rating for the MOSFET and power diode is calculated for the minimum input voltage under full load using the following equations:

$$I_{MOS\_PK\_MAX} = I_{P\_PK\_MAX}$$

$$I_{MOS\_RMS\_MAX} = I_{P\_RMS\_MAX}$$

$$I_{D\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX}$$

$$I_{D\_AVG} = I_{OUT}$$

where $I_{P\text{-}PK\text{-}MAX}$ and $I_{P\text{-}RMS\text{-}MAX}$ are maximum primary peak current and RMS current, which are discussed in later sections.

Transformer (N_{PS} and L_M)

N_{PS} is limited by the voltage rating of the power MOSFET:

$$N_{PS} \le \frac{V_{MOS\_(BR)DS} \times 90\% - \sqrt{2} V_{AC\_MAX} - \Delta V_S}{V_{OUT} + V_{D\_F}}$$

where $V_{MOS,(BR)DS}$ is the breakdown voltage of the power MOSFET.

In quasi-resonant mode, each switching period cycle t_S consists of three parts: current rising time t_1, current falling time t_2, and quasi-resonant time t_3, as shown in Figure10.

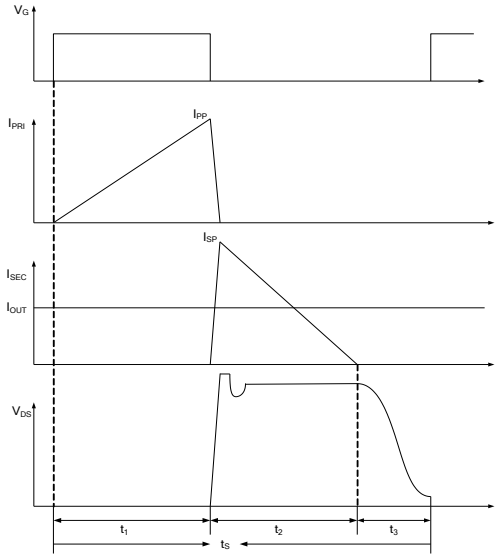


Figure 10. Switching Waveforms

The SY22650B operates in constant on-time mode to achieve a high power factor. The on-time increases with the input AC RMS voltage decreasing and the load increasing. When operating with minimum input AC RMS voltage under full load, the on-time reaches its maximum value. Conversely, when the input voltage is at the peak value, the off-time reaches it maximum value. Therefore, the minimum switching frequency $f_{S\text{-}MIN}$ occurs at the peak value of input voltage with minimum input AC RMS voltage and maximum load, which is also the condition for the maximum peak current through the MOSFET and the transformer ($I_{P\_PK\_MAX}$).

With the minimum frequency $f_{S\text{-}MIN}$ being set, the inductance of the transformer windings can be calculated based on the following design flow:

1. Select N_{PS}:

$$N_{PS} \le \frac{V_{MOS\_(BR)DS} \times 90\% - \sqrt{2} V_{AC\_MAX} - \Delta V_S}{V_{OUT} + V_{D\_F}}$$

2. Preset minimum frequency $f_{S\text{-}MIN}$. Generally, f_{S_MIN} higher than 70kHz is not recommended with full-range input voltage.

3. Compute relative t_S and t_1 (t_3 is omitted to simplify the design here):

$$t_S = \frac{1}{f_{S\_MIN}}$$

$$t_1 = \frac{t_S \times N_{PS} \times (V_{OUT} + V_{D\_F})}{\sqrt{2} V_{AC\_MIN} + N_{PS} \times (V_{OUT} + V_{D\_F})}$$

4. Compute inductance L_M:

$$L_M = \frac{V_{AC\_MIN}^2 \times t_1^2 \times \eta}{2 P_{OUT} \times t_S}$$

5. Compute t_3:

$$t_3 = \pi \times \sqrt{L_M \times C_{Drain}}$$

where C_{DRAIN} is the parasitic capacitance at the MOSFET drain.

6. Compute primary maximum peak current $I_{P\text{-}PK\text{-}MAX}$ and RMS current $I_{P\text{-}RMS\text{-}MAX}$ for the transformer fabrication:

$$I_{P\_PK\_MAX} = \frac{2 P_{OUT} \times \left[\frac{L_M}{\sqrt{2} V_{AC\_MIN}} + \frac{L_M}{N_{PS} \times (V_{OUT} + V_{D\_F})} \right]}{L_M \times \eta} + \frac{\sqrt{4 P_{OUT}^2 \times \left[\frac{L_M}{\sqrt{2} V_{AC\_MIN}} + \frac{L_M}{N_{PS} \times (V_{OUT} + V_{D\_F})} \right]^2 + 4 L_M \times \eta \times P_{OUT} \times t_3}}{L_M \times \eta}$$

where η is the efficiency; P_{OUT} is the rated full load power.

7. Adjust t_1 and t_S to t_1' and t_S' considering the effect of t_3:

$$t_S' = \frac{\eta \times L_M \times I_{P\_PK\_MAX}^2}{4P_{OUT}}$$

$$t_1' = \frac{L_M \times I_{P\_PK\_MAX}}{\sqrt{2}V_{AC\_MIN}}$$

$$I_{P\_RMS\_MAX} \approx \sqrt{\frac{t_1'}{6t_S'}} \times I_{P\_PK\_MAX}$$

8. Compute secondary maximum peak current $I_{S\text{-}PK\text{-}MAX}$ and RMS current $I_{S\text{-}RMS\text{-}MAX}$ for the transformer fabrication:

$$I_{S\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX}$$

$$t_2' = t_S' - t_1' - t_3$$

$$I_{S\_RMS\_MAX} \approx \sqrt{\frac{t_2'}{6t_S'}} \times I_{S\_PK\_MAX}$$

Transformer Design (N_P, N_S, N_{AUX})

The design of the transformer is similar to a typical flyback transformer, with the required parameters shown in Table 1.

Table 1. Required Transformer Parameters

Parameter	Symbol
Turns ratio	N_{PS}
Inductance	L_M
Primary maximum current	$I_{P\text{-}PK\text{-}MAX}$
Primary maximum RMS current	$I_{P\text{-}RMS\text{-}MAX}$
Secondary maximum RMS current	$I_{S\text{-}RMS\text{-}MAX}$

The transformer construction parameters can be determined using the following steps:

1. Select the magnetic core style and identify the effective area A_e.
2. Select the maximum magnetic flux ΔB:

$$\Delta B = 0.22 \sim 0.26T$$

3. Compute primary turns N_P:

$$N_P = \frac{L_M \times I_{P\_PK\_MAX}}{\Delta B \times A_e}$$

4. Compute secondary turns N_S:

$$N_S = \frac{N_P}{N_{PS}}$$

5. Compute auxiliary turns N_{AUX}:

$$N_{AUX} = N_S \times \frac{V_{VIN}}{V_{OUT}}$$

where V_{VIN} is the working voltage of the V_{IN} pin (a value of 10V–20V is recommended).

6. With $I_{P\text{-}RMS\text{-}MAX}$ and $I_{S\text{-}RMS\text{-}MAX}$, select an appropriate wire diameter to make sure the current density ranges from 4A/mm² to 10A/mm².
7. If the winding area of the core and bobbin is insufficient, reselect the core style and repeat from Step 1 until the optimal transformer design is achieved.

RCD Snubber for MOSFET

The power loss of the snubber P_{RCD} is evaluated first:

$$P_{RCD} = \frac{N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S}{\Delta V_S} \times \frac{L_K}{L_M} \times P_{OUT}$$

where N_{PS} is the turns ratio of the flyback transformer; V_{OUT} is the output voltage; $V_{D\text{-}F}$ is the forward voltage of the power diode; ΔV_S is the overshoot voltage clamped by the RCD snubber; L_K is the leakage inductance; L_M is the flyback transformer inductance; P_{OUT} is the output power.

R_{RCD} can be calculated using the following equation:

$$R_{RCD} = \frac{(N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S)^2}{P_{RCD}}$$

C_{RCD} is related to the snubber $\Delta V_{C\text{-}RCD}$ voltage ripple as follows:

$$C_{RCD} = \frac{N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S}{R_{RCD} f_S \Delta V_{C\_RCD}}$$

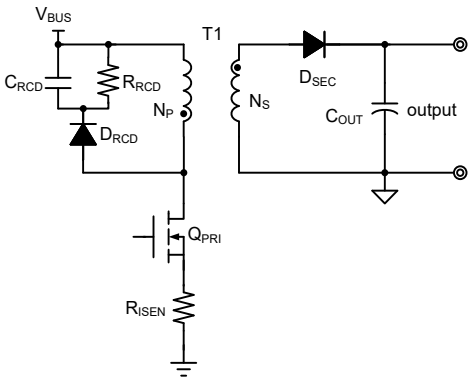


Figure 11. RCD Snubber

Typ Application Schematic

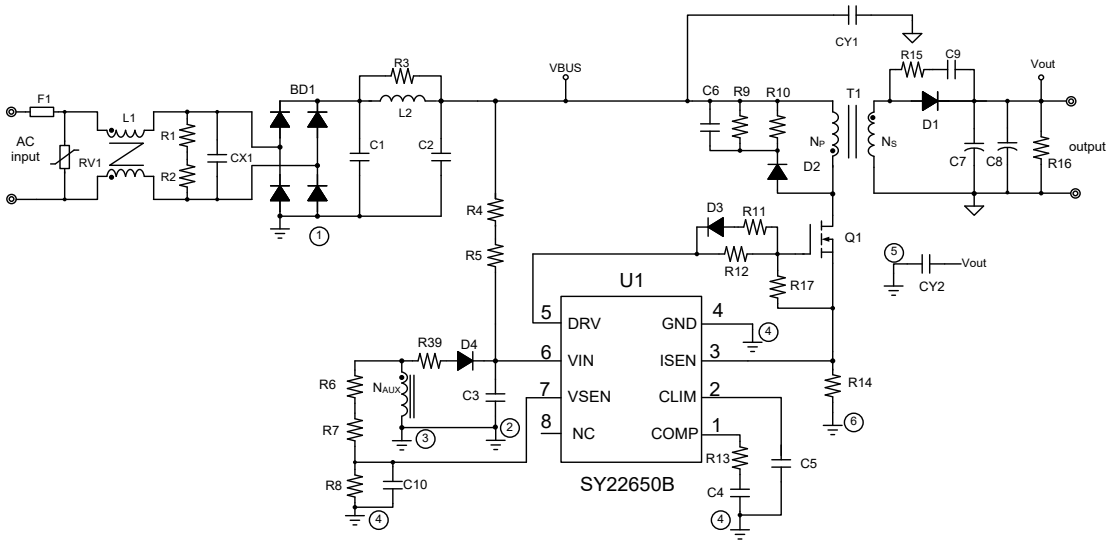


Figure 12. Typ Application Schematic

Recommended PCB Layout

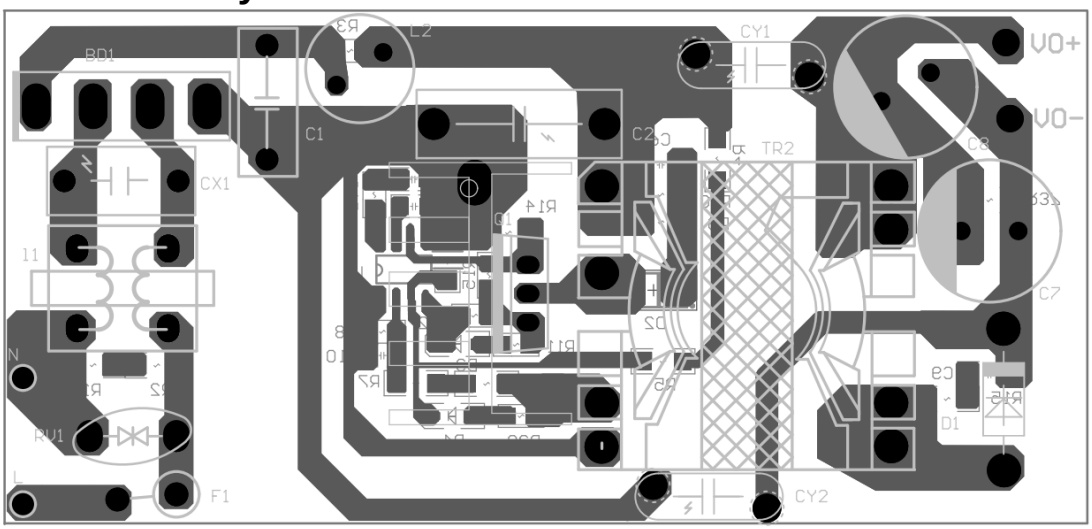
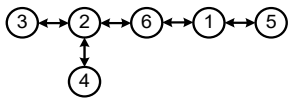


Figure 13. EVB Layout

Connect the primary ground as follows:

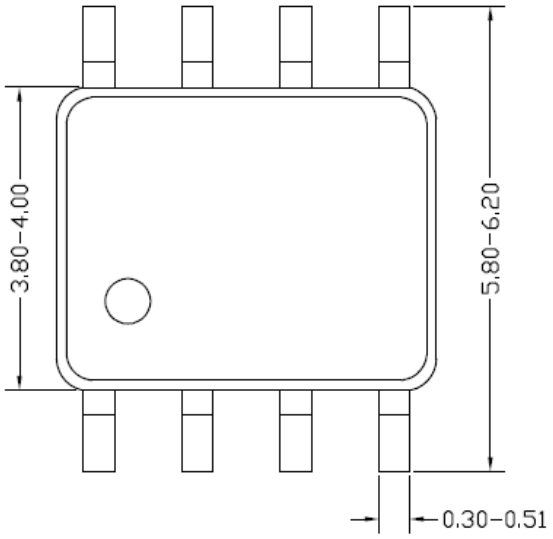


- Ground ①: ground of bus line capacitor
- Ground ②: ground of bias supply capacitor
- Ground ③: ground node of auxiliary winding
- Ground ④: ground of signal trace
- Ground ⑤: primary ground node of Y capacitor
- Ground ⑥: ground node of current sample resistor

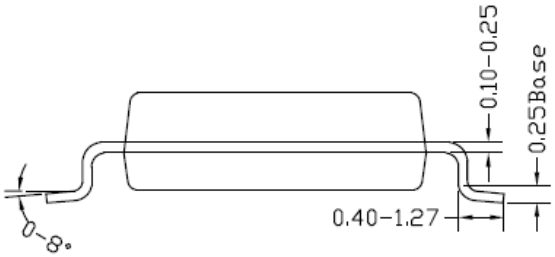
BOM List

Ref Des	Value/Type	Manufacturer	Part Number	comment
F1	250V/2A	Littelfuse	40012000000	Fuse
RV11	471K/D10	Brightking	471KD10	Varistor
L1	UF9.8/10mH			Common choke
CX1	220nF/CX2	Jimson	MKP224K310A01	X2
CY1	222M	TDK	CD45-E2GA222M-AKA	Y1
CY2	102M	TDK	CD45-E2GA102M-VKA	Y1
C1	100nF/CBB/450V	PANISONIC	MPP104K5130508LC	CBB
C2	330nF/CBB/400V	SRD	MPP334J5130512LC	CBB
BD1	4A/600V	MDD	KBL406	Diode bridge
L2	Φ10/1mH			Inductor
T1	PQ2620/360uH			Transformer
D1	MUR460	ON	MUR460RLG	Diode
C7,C8	470uF/63V	Rubycon	63YXJ470MG412.5X25	E-CAP
Q1	10A/650V/TO-220	SILAN	SVF10N65F	MOSFET
R4,R5	300K/1206	YAGEO	AC1206FR-07300KL	Resistor
R9,R10	150K/1206	YAGEO	RT1206FRE07150KL	Resistor
R16	12K/1206	YAGEO	AC1206FR-0712KL	Resistor
R39	200R/1206	YAGEO	RC1206FR-07200RL	Resistor
R1,R2	1M/1206	YAGEO	AC1206JR-071ML	Resistor
R14	0.33/1206	YAGEO	RL1206FR-070R33L	Resistor
R6	39K/0805	YAGEO	RC0805FR-0739KL	Resistor
R7	110k/0805	YAGEO	AC0805FR-07110KL	Resistor
R8	9.1K/0805	YAGEO	AC0805FR-079K1L	Resistor
R13	20K/0805	YAGEO	RC0805FR-0720KL	Resistor
R11	33R/0805	YAGEO	RC0805FR-0733RL	Resistor
R12	100R/0805	YAGEO	RC0805FR-07100RL	Resistor
R15	10R/1206	YAGEO	RL1206FR-07010L	Resistor
R3, R17	10K/0805	YAGEO	RC0805FR-0710KL	Resistor
C6	1nF/1KV/1206	MURATA	GCM31C7U3A102JX03L	CAP
C9	47pF/1KV/1206	MURATA	GRM31A5C3A470JW01D	CAP
C3	4.7uF/50V/1206	MURATA	GRM319R61H475KA12D	CAP
C5	220nF/50V/0805	MURATA	GCM21BR71H224KA37L	CAP
C4	470nF/50V/0805	MURATA	GCJ21BR71H474KA12L	CAP
D3	1N4148/SOD-123	VISHAY	1N4148W-E3-08	Diode
D1, D2	RS1M/SMA	PANJIT	RS1MW_R1_00001	Diode
U1	SY22650B/SO8	SILERGY	SY22650BFAC	IC

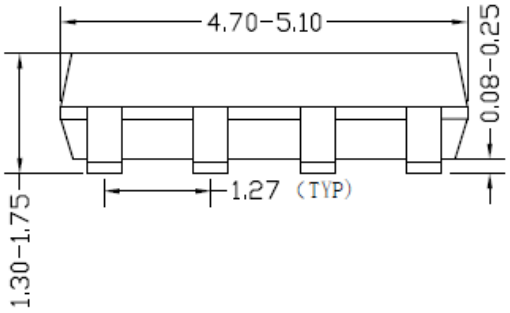
SO8 Package Outline Drawing



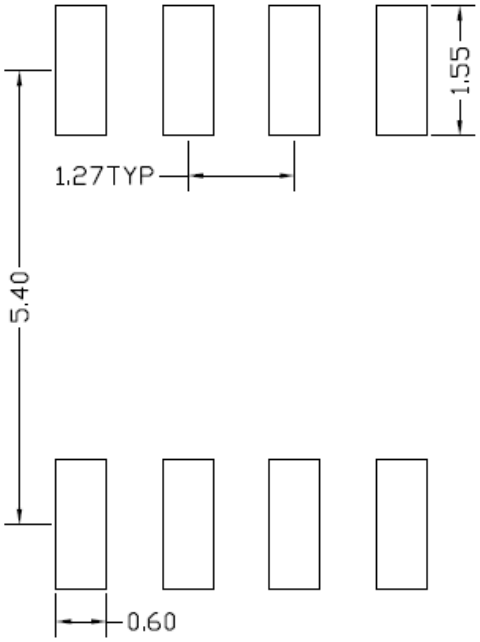
Top view



Side view



Front view



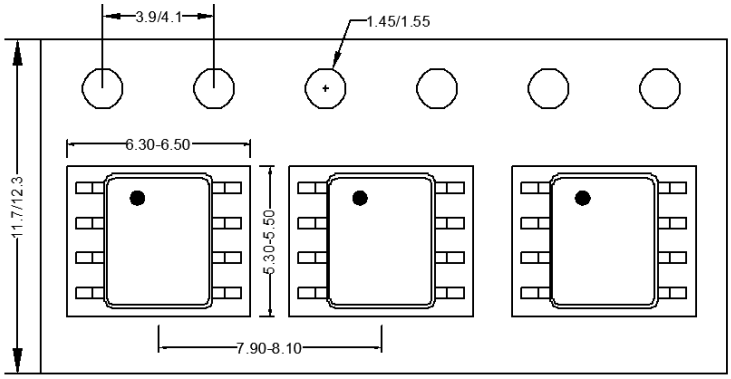
Recommended Pad Layout

(Reference only)

***Notes**: All dimension in millimeter and exclude mold flash & metal burr.*

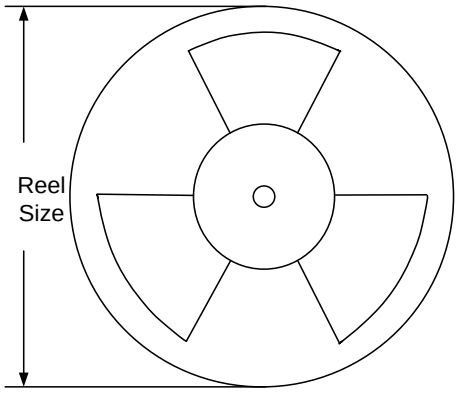
Taping and Reel Specification

SO8 taping orientation



Feeding direction →

Carrier tape and reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel (pcs)
SO8	12	8	13"	400	400	2500

Others: NA

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