SY20716D1

Highly Integrated USB Compliant Single Li-Ion Cell Switching Charger with USB-OTG Function

General Description

The SY20716 is a highly efficient, buck-mode switching charger designed for single-cell Li-ion and Li-polymer batteries. This device enables a comprehensive solution for portable devices by integrating essential components such as the blocking MOSFET, power MOSFETs, input current sensing circuits, and the charger controller. It is fully USB compliant, ensuring minimized charging times when powered via a USB port. Additionally, the SY20716 supports USB on-the-go (OTG) functionality through its built-in boost regulator.

The device employs three internal digital-to-analog converters (DACs) to set and regulate the battery voltage, battery charging current, and adapter input current limit. These parameters are programmable via I^2C by the host controller. The SY20716 features an adaptive input current limit, which optimizes the charging current to reduce charging time while preventing overloading of the input source.

The SY20716 is available in a compact CSP 1.93mm x 2.05mm – 20 pin package.

Applications

- PADs
- Smartphones
- Portable Equipment with Rechargeable Batteries
- Battery Back-Up Systems

Features

- Up to 18V Absolute Maximum Input Voltage
- 6V Maximum Operating Input Voltage
- Up to 1.25A Charge Current (68mΩ R_{SEN})
- Up to 1.55A Charge Current (55mΩ R_{SEN})
- Adaptive Input Current Limit
- ±5% Input Current Limit Accuracy at 500mA
- ±0.5% Charge Voltage Accuracy
- I^2C Controls (Up to 3.4Mbps):
  - Battery Charge Voltage (3.5V – 4.44V)
  - Battery Charge Current (550mA – 1.25A)
  - Termination Current (50mA – 400mA)
  - Battery Weak Voltage (3.4V – 3.7V)
  - Input Current Limit
  - VBUS Threshold for Adaptive Input Current
  - Low Charge Current Mode Enable And Disable
  - Termination Enable and Disable
- Integrated Loop Compensation
- Internal Soft-Start
- Bad Adapter Detection and Rejection
- 3MHz Switching Frequency
- Automatic High Impedance Mode for Reduced Power Consumption
- 5V,1A Boost Mode for USB OTG
- Spread Spectrum Control for Improved EMI Performance
- Factory Test Mode for GSM Calibration Without a Battery
- CSP1.93x2.05-20 Package

Typical Application

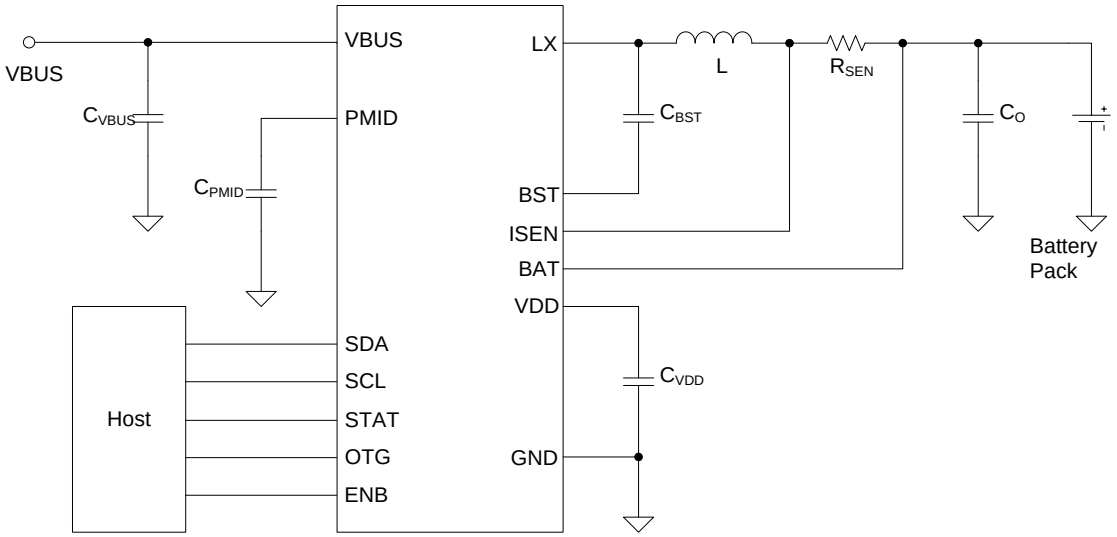


Figure 1. SY20716D1 Schematic Diagram

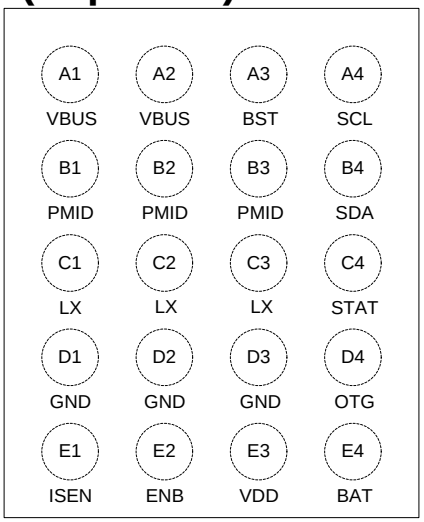
Ordering Information

SY20716□(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package Type	Top Mark
SY20716D1PPC	CSP1.93x2.05-20	BOT xyz

Device code: **BOT**
x=year code, y=week code, z= lot number code

Pinout (Top View)



(CSP1.93x2.05-20)

Pin Name	Pin Number	Pin Description
VBUS	A1,A2	Charger input voltage.
BST	A3	High side power MOSFET driver power supply.
SCL	A4	I^2C clock input. Connect an external pull-up resistor according to I^2C specifications.
PMID	B1,B2,B3	Buck converter input point. Bypass it with a minimum of 4.7μF ceramic capacitor to GND.
SDA	B4	I^2C data I/O. Open-drain output. Connect an external pull-up resistor according to I^2C specifications.
LX	C1,C2,C3	Switching node.
STAT	C4	Open drain output for charge status indicator. Driven low during charging.
GND	D1,D2,D3	Ground pins.
OTG	D4	Enable boost regulator with OTG_Enable and OTG_Level_Select bits. During faults, a 128μs pulse is sent out. On VBUS POR, this pin sets the input current limit in default mode.
ISEN	E1	Battery charging current sense positive input.
ENB	E2	Charge enable pin. Active low enables the charger.
VDD	E3	LDO output for converter power MOSFETs driver. Connect at least 1μF ceramic capacitor to GND.
BAT	E4	Battery charging current sense negative input and battery voltage sense input.

Absolute Maximum Ratings (Note 1)

VBUS, PMID, STAT, SCL, SDA, OTG, ENB, ISEN, BAT ---------- -0.3V to +18V
LX ---------- -2V to +18V
VDD, BST-LX ---------- -0.3V to 3.6V
ISEN-BAT ---------- -0.5V to +0.5V
Package Thermal Resistance (Notes 2)
CSP1.93x2.05, θ_{JA} ---------- 85 °C/W
Junction Temperature Range ---------- -40°C to +150°C
Storage Temperature ---------- -60°C to +150°C
Lead Temperature (Soldering, 10s) ---------- +260°C

Recommended Operating Conditions (Note 3)

VBUS, PMID, STAT, SCL, SDA, OTG, ENB, ISEN, BAT, LX---------- -0.3V to 6V
VDD, BST-LX ---------- -0.3V to 3.3V
ISEN-BAT---------- -0.5V to 0.5V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(T_J=25°C, V_{VBUS} = 5V, ENB=0, R_{SENSE}=68mΩ, , unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Charge Operating Conditions						
VBUS Input Voltage Range	V_{VBUS}		4		6	V
VBUS Under Voltage Lockout	V_{VBUSUV}	VBUS rising edge	3.05	3.3	3.55	V
VBUS Under Voltage Lockout Hysteresis	V_{VBUSUV_HYS}	VBUS falling edge		150		mV
Input Over Voltage	V_{INOV}	VBUS rising edge		6.5		V
Input Over Voltage Hysteresis	V_{INOV_HYS}	VBUS falling edge		170		mV
VBUS Supply Current Control	I_{VBUS}	V_{VBUS} = 5V, PWM not switching			1.5	mA
Charge Regulation Range and Accuracy						
Charge Voltage Regulation Range	V_{BAT_REG}	BAT voltage	3.5		4.44	V
Charge Voltage Regulation Accuracy	$V_{BAT\_REG\_ACC}$	T_A=25ºC	-0.5		0.5	%
Charge Current Regulation Range	I_{CHG_REG}	V_{ISEN} –V_{BAT}, 68mΩ sense resistor	550		1250	mA
		V_{ISEN} –V_{BAT},55mΩ sense resistor	608		1550	mA
Low Charge Current	I_{CC_LOW}	V_{SHORT}≤V_{BAT}≤V_{CV}, Low_Charge=1		325	350	mA
Charge Current Reference Voltage	V_{CHG}	Low_Charge=0, I_{CHG}_Reference=000	36.8		39.4	mV
		Low_Charge=0, I_{CHG}_Reference=011	57.2		60.5	mV
Battery Voltage Drop for Recharge Threshold	V_{RCH}	V_{RCH} =V_{CV_REG}-V_{BAT}	90	120	150	mV
Recharge Deglitch Time	t_{RCH}	V_{BAT} falls below threshold		130		ms
Input Current Limit Accuracy	I_{IN_LIM}	USB 100mA	83		97	mA
		USB 500mA	450	475	500	mA
VBUS Range for Adaptive Input Current Limit	V_{IIN_LIM}		4.2		4.76	V
VBUS Voltage Regulation Accuracy	$V_{IIN\_LIM\_ACC}$	Adaptive_IIN_Threshold=100	4.4		4.58	V
Charge Termination						
Termination Charge Current Range	I_{TERM}	V_{BAT}>V_{RCH}, V_{BUS}-V_{BAT}>V_{ASD}	50		400	mA
Deglitch Time for Charge Termination	t_{TERM}			30		ms
Termination Current Accuracy	I_{TERM_ACC}	I_{TERM}=100mA	-15		15	%
		I_{TERM}=250mA	-10		10	%
Weak Battery Detection						
Weak Battery Voltage Threshold Range	V_{LOWV}		3.4		3.7	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Weak Battery Voltage Accuracy	V_{LOWV_ACC}		-5		5	%
Weak Battery Voltage Hysteresis	V_{LOWV_HYS}	Battery voltage falling edge		100		mV
Input Source Qualification						
Poor Input Source Voltage	V_{INUV}	VBUS falling edge	3.6	3.8	4.0	V
Poor Input Source Voltage Hysteresis	V_{INUV_HYS}	VBUS rising edge		200		mV
Current Source to GND for Input Source Qualification	I_{IN_QUA}	During input source qualification		30		mA
Qualification Interval	t_{IN_QUA}	During input source qualification		2		s
Battery Detection						
Battery Detection Current Before Charge Done	I_{BAT_DET}	Begins after termination detected		-0.5		mA
Battery Detection Time	t_{BAT_DET}			260		ms
Auto Shutdown						
Auto Shutdown Threshold	V_{ASD}	V_{VBUS}-V_{BAT} falling edge	0	80	100	mV
Exit Auto Shutdown Threshold	V_{ASD_EXIT}	V_{VBUS}-V_{BAT} rising edge	120	200	280	mV
VDD						
Internal Bias LDO Output	V_{VDD}	I_{VREF}=1mA, C_{VREF}=1μF		3.3		V
VDD Short Circuit Current Limit	I_{VDD}			100		mA
PWM Converter						
Blocking FET $R_{DS(ON)}$	$R_{ON(BLKFET)}$			180	250	mΩ
High Side FET $R_{DS(ON)}$	$R_{ON(HSFET)}$			120	250	mΩ
Low Side FET $R_{DS(ON)}$	$R_{ON(LSFET)}$			110	210	mΩ
Swtching Frequency	f_{SW}			3.0		MHz
Charge Mode Protection						
Battery OVP	V_{BAT_OVP}	VBAT rising edge	110	117	121	%
Battery OVP Hysteresis	$V_{BAT\_OVP\_HYS}$	VBAT falling edge		11		%
Cycle-by-cycle Current Limit	I_{LIM}			2.7		A
Battery Short Threshold	V_{SHORT}	VBAT falling edge	1.85	1.95	2.05	V
Battery Short Hysteresis	V_{SHORT_HYS}	VBAT rising edge		100		mV
Short Mode Charge Current	I_{SHORT}	V_{BAT}<V_{SHORT}		30		mA
Boost Regulation and Accuracy						
OTG Output on VBUS	V_{VBUS_OTG}		4.90	5.05	5.20	V
Maximum OTG Output Current	I_{VBUS_OTG}	V_{VBUS_OTG}=5.05V	350			mA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Cycle-By-Cycle Current Limit	I_{OTG_LIM}	V_{VBUS_OTG}=5.05V, 3V<V_{BAT}<4.5V		1		A
OTG Output OVP	V_{OTG_OVP}	VBUS rising edge	5.60	5.75	5.90	V
OTG Output OVP Hysteresis	$V_{OTG\_OVP\_HYS}$	VBUS falling edge		160		mV
Battery Voltage Input OVP	V_{BAT_OVP}	VBAT rising edge	4.75	4.9	5.05	V
Battery Voltage Input OVP Hysteresis	$V_{BAT\_OVP\_HYS}$	VBAT falling edge		200		mV
Battery Voltage Input UVP	V_{BAT_UVP}	VBAT rising edge		2.9	3.05	V
Battery Voltage Input UVP Hysteresis	V_{BAT_UVP}	VBAT falling edge		400		mV
Boost Output Resistance at HI-Z Mode		ENB=1 or HZ_Mode=1	300			kΩ
Thermal Regulation and Thermal Shutdown						
Thermal Shutdown Temperature	T_{SD}	Junction temperature rising edge		155		ºC
Thermal Shutdown Temperature Hysteresis	T_{SD_HYS}	Junction temperature falling edge		20		ºC
Thermal Regulation Threshold	T_{REG}			120		ºC
STAT Output						
Low-Level Output Voltage		Sink 10mA current			0.55	V
Leakage Current		5V on STAT pin			1	μA
Logic Level and Timing						
ENB, OTG, SCL, SDA Low Level Threshold	V_{LOW}				0.4	V
ENB, OTG, SCL, SDA High Level Threshold	V_{HIGH}		1.2			V
I^2C Operating Frequency	f_{SCL}				3.4	MHz

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

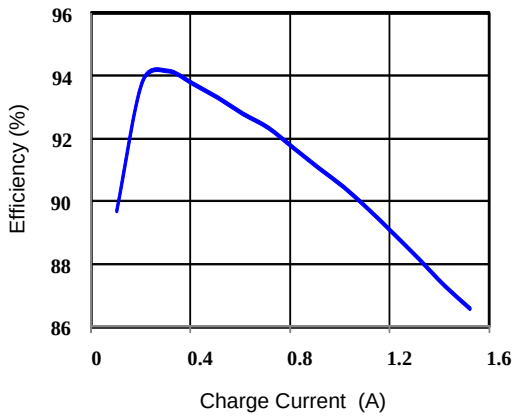
Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective four-layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions.

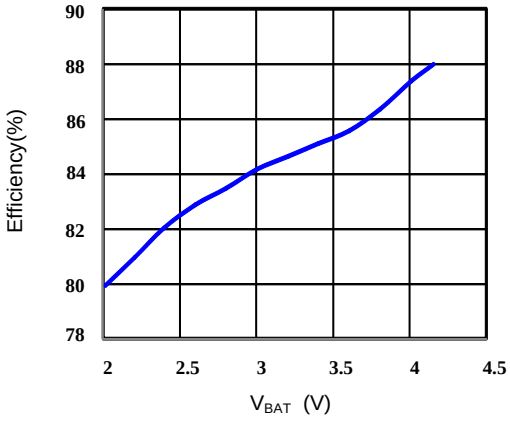
Typical Performance Characteristics

(T_A=25°C, V_{IN}=5V, R_{SEN}=55mΩ, 1cell battery, unless otherwise specified.)

Efficiency vs. Charge Current (CV mode)

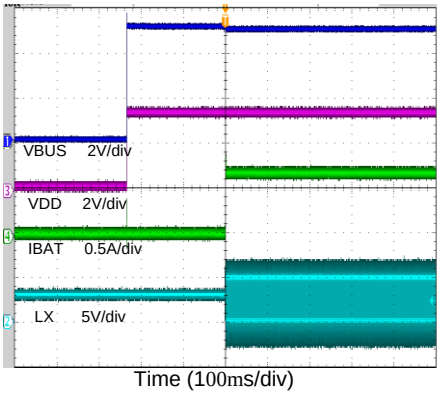


Efficiency vs. Charge Voltage (CC mode)



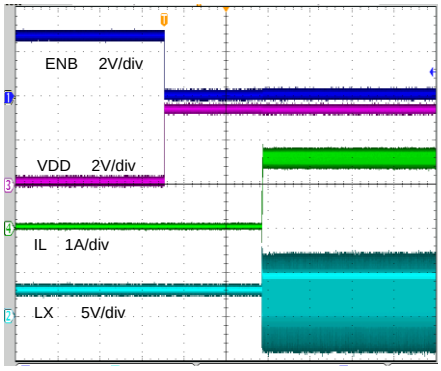
Power On

（VBUS=5V VBAT=3.4V host Mode）



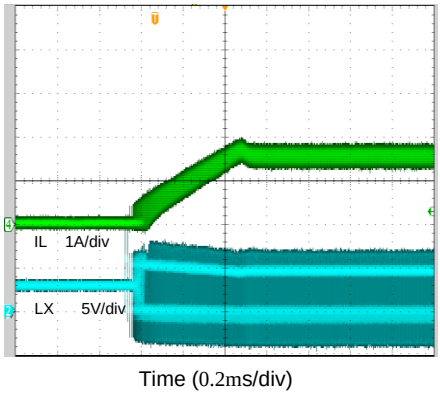
ENB On

（VBUS=5V VBAT=3.4V host Mode）



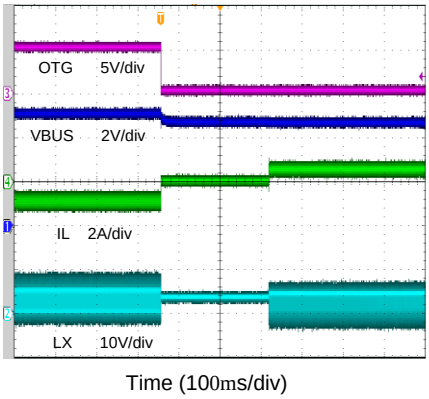
Charger Soft Start

（VBUS=5V VBAT=3.4V ICHG=1.55A host Mode）



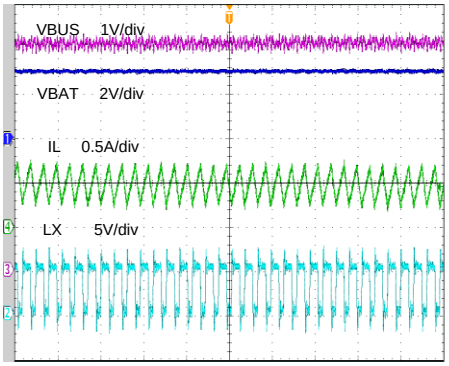
Boost To Charge Mode Transition

（VBUS connects 4.5V power supply, VBAT=3.6V OTG Control）



Constant Current Charge State

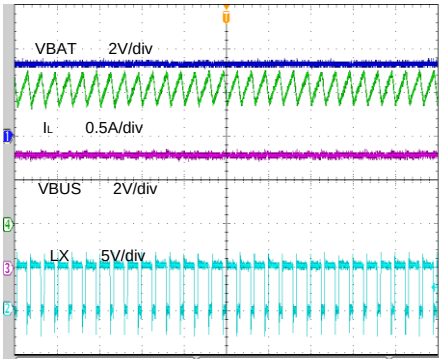
（VBUS=5V VBAT=3.2V Low charge 402mA）



Time (1μs/div)

Constant Current Charge State

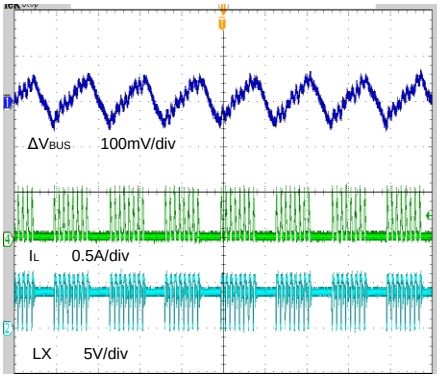
(VBUS=5V VBAT=3.2V ICHG=1.55A)



Time (1μs/div)

Boost Mode Light Load State

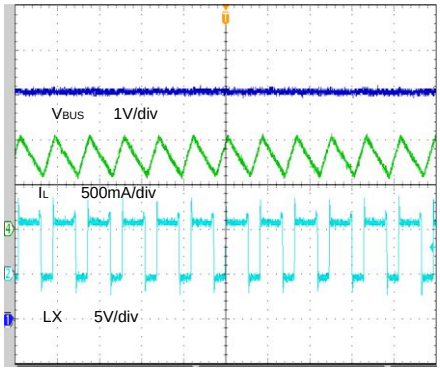
(VBAT=3.6V IBUS=0.05A)



Time (10μs/div)

Boost Mode Full Load State

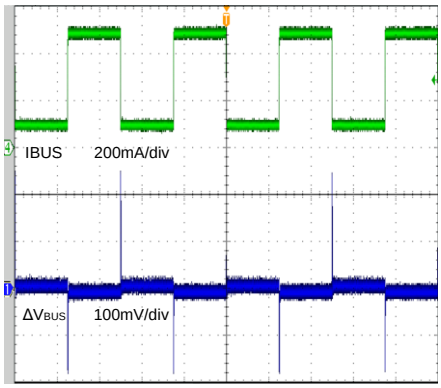
(VBAT=3.6V IBUS=0.5A)



Time (0.4μs/div)

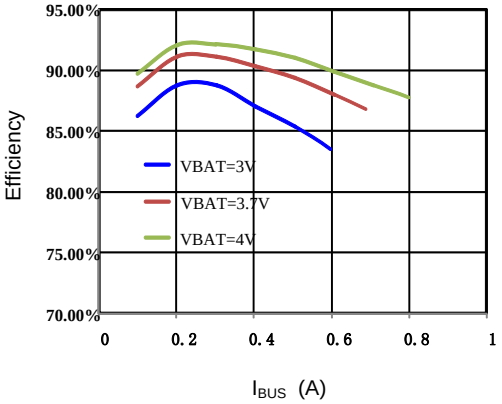
Boost Mode Load transient

(VBAT=3.6V IBUS=0.1A~0.5A)



Time (4ms/div)

Efficiency vs. Load current (Boost mode)



Functional Description

The SY20716D1 includes multiple functions essential for charging 1-cell Li-Ion and Li-polymer batteries. It features a high-efficiency 3MHz synchronous buck converter to control the charge voltage from 3.5V to 4.44V and supports a charge current of up to 1.55A. The SY20716D1 also incorporates an input current limit to prevent USB overloading. The input current limit, charge current limit, and charge voltage limit are adjustable through internal registers, which are programmed using I^2C. Additionally, the SY20716D1 supports an OTG function, enabling it to power a USB port via its internal boost regulator.

The SY20716D1 has three operation modes:

1. Charging mode.
2. Boost mode: Provides 5V power to the USB using the internal boost regulator from the battery input.
3. High-impedance mode: The boost and charger are turned off in this mode. The charger enters a low quiescent current state to save power.

VBUS Detection:

The SY20716D1 can be connected to either an adapter or USB as its input. The VBUS pin is the source input for input voltage sensing. When VBUS (VVBUS) voltage exceeds the undervoltage (UV) threshold, the input source is verified using a 30mA current source. Once the input is successfully qualified, the SY20716D1 initiates charging. If during the qualification phase VVBUS falls below 3.8V, the device deactivates the current source and sets the 'Bad Source Fault' flag in the 00H register.

Auto-Shutdown:

The device will automatically shut down and enter low-power mode if the V_{VBUS} falls below the auto-shutdown threshold and above the UV threshold. During auto-shutdown, VDD, the blocking FET, and PWM are turned off.

Input Current Limit:

The input current limit can be programmed through the 01H register and is sensed by built-in current sensing circuits. The device will automatically reduce the charge current when the input current exceeds the programmed value.

Battery Voltage, Battery Current, and Adapter Input Voltage Regulation:

The battery voltage regulation is configured via the 02H register, programmed by the host microcontroller through the I^2C interface.

Battery current regulation is determined by the 04H register and is sensed through a resistor connected between the ISEN and BAT pins. With a 68mΩ sense resistor, the maximum current is set to 1.25A; with a 55mΩ sense resistor, the maximum current is 1.55A. The charge voltage and current cannot exceed the safety limit values specified in the 06H register.

The input voltage regulation is controlled by the 05H register and monitored by built-in voltage sensing circuits. The device automatically reduces the charge current when VVBUS falls below the Adaptive_IIN_Threshold (default set at 4.52V).

Battery Detection:

The SY20716D1 is capable of detecting the battery. Once termination occurs, the device enables a discharge current, IBAT_DET, for a duration of tBAT_DET (262ms) and then checks the battery voltage. If the battery voltage falls below the recharge threshold after tBAT_DET, it is determined that the battery is absent. In this case, the device sets the 'no battery fault' flag in the 00H register and resets the charge parameter registers. This battery detection feature ensures that specific charge parameters are reset whenever the battery is replaced.

USB Friendly Power-Up:

If the battery voltage is above the BAT_Weak threshold while in default mode, the charger enters a high impedance state. As a safety measure, the default control bits set both the charge current and regulation voltage low to prevent USB specification violations and overcharging of any Li-Ion chemistries, especially in cases where the host has lost communication.

In default mode, the logic level of the OTG pin determines the input current limit, setting it to 100mA for a logic low and 500mA for a logic high. In host mode, the input current limit is set by the 01H register.

Charge Mode Operation:

When a good battery with a voltage below the recharge threshold is inserted, and a suitable adapter is connected, the device enters charge mode. In this mode, the device manages five control loops to regulate input voltage, input current, charge current, charge voltage, and device junction temperature. During charging, all five loops are active, and the dominant loop takes control. The device supports a precision Li-ion or Li-polymer charging system for single-cell applications.

During normal charging under host control, termination is detected if the voltage at the BAT pin remains above the battery recharge threshold for a 30ms deglitch period and the charge current falls below the I_{TERM} threshold. The device then turns off the PWM charging and enables battery detection.

The termination current level is programmable. To disable charge current termination, the host can set the charge termination bit (Termination_Enable) in the charge control register to 0.

A new charge cycle will initiate under any of the following conditions:

- The battery voltage drops below the recharge threshold.
- VBUS Power-on reset (POR) occurs, if the battery voltage is below the weak battery threshold.
- The ENB bit is toggled, or the RESET bit is set (as controlled by the host).

Battery Protection in Charge Mode:

Battery overvoltage protection safeguards the device, the battery, and system components from damage in case of excessively high battery voltage, particularly when the battery is removed suddenly. If overvoltage protection (OVP) is triggered, the device will shut off the PWM and set fault flag bits. The charger will resume normal operation once the fault condition is resolved.

When the battery voltage falls below the V_{SHORT} threshold, the device will turn off the PWM, charging the battery with a 30mA current.

Boost Mode Operation:

In host mode, when the OTG pin is high (and the OTG_Enable bit is set to enable OTG functionality) or the operation mode bit (OPA_MODE) is set to 1, the device operates in boost mode, supplying power to VBUS from the battery. In normal boost mode, the device converts the battery voltage to approximately 5.05V (V_{VBUS_OTG}) and delivers a current of up to 1A (I_{BUS_OTG}) to power USB OTG devices connected to the USB connector.

Different from the charging mode operation, in boost mode, the device uses an integrated, fixed 3 MHz frequency controller to regulate the output voltage at the PMID pin (VPMID). The blocking FET in boost mode prevents battery discharge when the VBUS pin is overloaded.

Soft-start control is applied during the boost mode startup to prevent inductor saturation and limit inrush current.

Protection in Boost Mode:

The device includes built-in overvoltage protection to protect itself and other components from damage if the VBUS voltage is excessively high. When an overvoltage condition is detected, the device will shut off the PWM converter, reset the OPA_MODE bit to 0, set fault status bits, and drive a fault pulse on the STAT pin. Once VVBUS returns to normal, the boost mode will reactivate after the host sets OPA_MODE to '1' or the OTG pin remains active.

The device also features built-in overload protection to prevent damage to itself and the battery when VBUS is overloaded. If an overload condition is detected, Q1 will operate in linear mode to limit the output current. An overload fault is registered if this condition persists for more than 30ms. Upon detecting an overload fault, the device will turn off the PWM converter, reset the OPA_MODE bit to 0, set fault status bits, and emit a fault pulse from the STAT pin.

In boost mode, if the battery voltage exceeds the overvoltage threshold (V_{BAT_MAX}) or falls below the minimum battery voltage threshold (V_{BAT_MIN}), the device will shut off the PWM converter, reset the OPA_MODE bit to 0, set fault status bits, and drive a fault pulse on the STAT pin. The boost mode will restart once the battery voltage rises above VBAT_MIN and falls below VBAT_MAX, either when the host sets OPA_MODE to '1' or the OTG pin remains in active status.

PFM:

The device will automatically decrease the switching frequency at light load conditions to achieve high efficiency.

Spread Spectrum:

The spread spectrum mode can only be enabled in charging mode. The spread spectrum clock modulation's purpose is to reduce EMI during operation. In charging mode, the 3MHz switching frequency changes by +/-10% in a 1ms time interval. As a result, the EMI energy of the switching converter is distributed over a wider range of frequencies, lowering the magnitude of EMI in the 3MHz +/-10% range and its harmonic frequencies.

Factory Test Mode:

The factory mode can only be enabled in charging mode, whether the battery is present or not. It can be set through I^2C Reg05, bit 6. Setting the factory mode bit enables the following changes:

- The output current limit is disabled, while Idpm still continues to function unless disabled by the host.
- The charging mode cycle-by-cycle peak current limit threshold is increased to double its standard value.

High Impedance (Hi-Z) Mode:

Driving the ENB pin high causes the charger to enter high-impedance (Hi-Z) mode. In default mode, when the ENB pin is low, the charger automatically transitions to Hi-Z mode under the following conditions:

1. $V_{VBUS} > V_{VBUS\_UVLO}$ and a battery with $V_{BAT} > V_{LOWV}$ is inserted.
2. V_{VBUS} falls below V_{VBUS_UVLO}.

In host mode, with the ENB pin low, the charger can be switched to Hi-Z mode if the Hi-Z mode control bit is set to '1' and the OTG pin is not in an active state.

In order to exit Hi-Z mode, the ENB pin must be set low, V_{VBUS} must be higher than the V_{VBUS_UVLO} threshold, and the host must write a '0' to the Hi-Z-mode control bit.

Thermal Shutdown Protection (TSD)

When the junction temperature exceeds 155°C, thermal shutdown is enabled, and PWM is turned off. Charging will restart when T_J falls below 135 °C.

Status Output:

The STAT pin is used to indicate operation status. When the STAT_Enable bit in the control register (00H) is set to '1', STAT will be pulled low during charging. In all other situations, the STAT pin functions as a high impedance (open-drain) output. In the event of a fault, a 128-microsecond pulse is generated on this pin to alert the host. The behavior of the STAT pin under various operational conditions is outlined in the table below. This pin can be utilized for driving an LED or for communication with the host processor.

Charge Status	STAT
Charge in progress and STAT_Enable = 1	Low
Other normal conditions	Open-drain
Charge mode faults: Auto shutdown, VBUS or battery overvoltage, poor input source, VBUS UVLO, no battery, thermal shutdown	128μs pulse, then open-drain
Boost mode faults: Overload, VBUS or battery overvoltage, low battery voltage, thermal shutdown	128μs pulse, then open-drain

I²C Interface

The SY20716D1 uses an I²C-compatible interface for flexible charging parameter programming and instantaneous device status reporting. Only two bus lines are required: a serial data line (SDA) and a serial clock line (SCL). Devices can be considered masters or slaves when performing data transfers. A master is the device that initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device responding to the data transfer is considered a slave.

The SY20716D1 operates as a slave device with address 6AH, receiving control inputs from the master device like a microcontroller or a digital signal processor. The I²C interface supports both standard mode (up to 100kbps), fast mode (up to 400kbps), and high speed mode (up to 3.4Mbps in write mode).

Both SDA and SCL are bi-directional lines connecting to the positive supply voltage via a current source or pull-up resistor. When the bus is idle, both lines will be HIGH. The SDA and SCL pins are open-drain.

F/S Mode Protocol:

Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit to transfer.

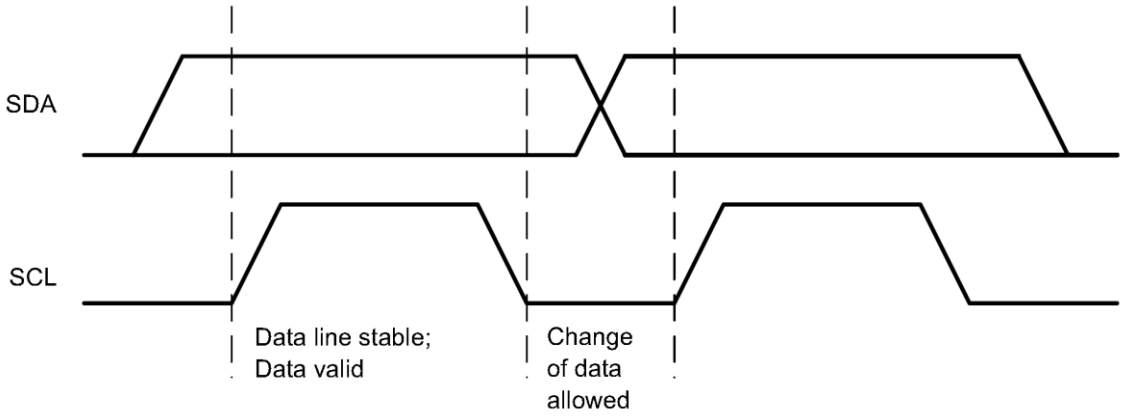


Figure 2. Bit Transfer on the I²C Bus

START and STOP Conditions

All transactions begin with a START (S) and can be terminated by a STOP (P). A HIGH to LOW transition on the SDA line, while SCL is HIGH, defines a START condition. A LOW to HIGH transition on the SDA line, when the SCL is HIGH, defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered busy after the START condition and free after the STOP condition.

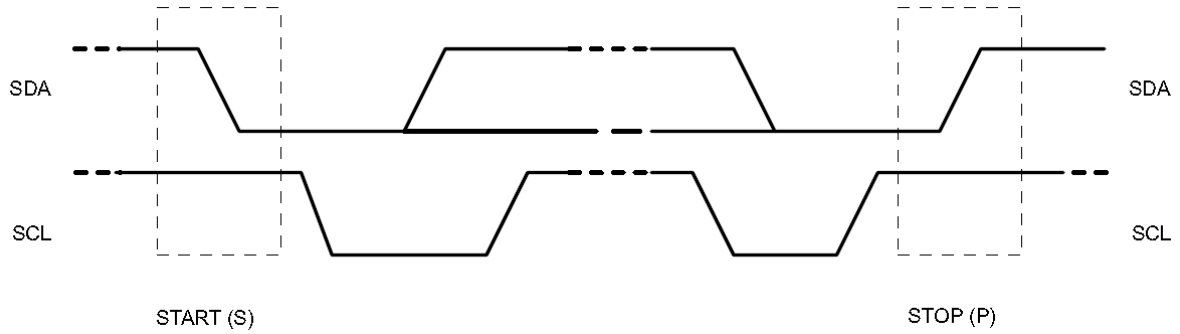


Figure 3. START and STOP Conditions

Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first.

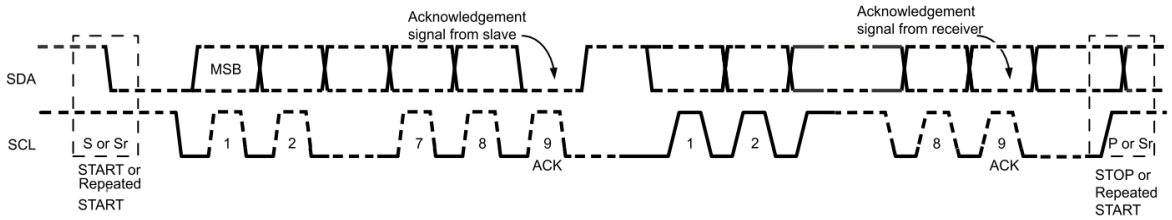


Figure 4. Data Transfer on the I²C Bus

Acknowledge (ACK) and Not Acknowledge (NACK)

In the I²C communication protocol, an acknowledgement (ACK) occurs after every byte transmitted. The ACK bit enables the receiver to inform the transmitter that the byte has been successfully received, signaling that the next byte can be sent. The master device generates all clock pulses, including the 9th clock pulse used for the ACK.

During the ACK clock pulse, the transmitter releases the SDA (Serial Data) line, allowing the receiver to pull this line LOW. The SDA line should remain stable and LOW throughout the HIGH period of this 9th clock pulse.

If the SDA line stays HIGH during this 9th clock pulse, it indicates a not acknowledge (NACK) signal. Following a NACK, the master has two options: generate a STOP condition to abort the current transfer or issue a repeated START condition to initiate a new transfer.

Slave Address and Data Direction Bit

After initiating a START condition in the **I²C** communication protocol, a 7-bit slave address is transmitted. This is followed by an eighth bit, which serves as the data direction bit (R/W bit). A zero in this position indicates a transmission (WRITE operation), whereas a one signifies a request for data (READ operation).

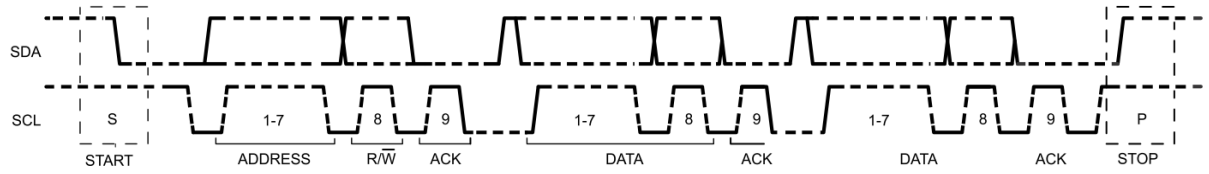


Figure 5. Complete Data Transfer

H/S Mode Protocol:

When the I²C bus is idle, pull-up resistors hold both the SDA and SCL lines high.

To enter HS mode, the master first generates a START condition and then sends a valid serial byte containing the HS master code '00001XXX'. This initial transmission occurs in F/S mode at a speed not exceeding 400Kbps. Although no device acknowledges the HS master code, all devices on the bus must recognize it and prepare for 3.4Mbps operation by adjusting their internal settings.

Following this, the master generates a repeated START condition, which has the same timing as the initial START condition. After this repeated START, the communication protocol remains the same as in F/S mode but now allows transmission speeds of up to 3.4Mbps. The HS mode is terminated by a STOP condition, which signals all slave devices to revert their internal settings to F/S mode. To maintain the bus in HS-mode, repeated START conditions should be used instead of a STOP condition. If a transaction is terminated prematurely, the master must send a STOP condition to prevent the slave devices' I²C logic from becoming stuck in a bad state.

Note that attempting to read data from register addresses not specified in this section will result in 'FFh' being read out.

I²C Update Sequence:

For a single update, the device requires a START condition, a valid I²C address, a register address byte, and a data byte. After receiving each byte, the device acknowledges the transmission by pulling the SDA (Serial Data) line low during the high period of a single clock pulse. The device is selected with a valid I²C address and performs an update on the falling edge of the acknowledge signal that follows the least significant byte (LSB).

For the initial update, the device requires a START condition, a valid I²C address, a register address byte, and a data byte. All subsequent updates only need a new register address byte and a data byte.

Once a STOP condition is received, the device will release the I²C bus and await a new START condition.

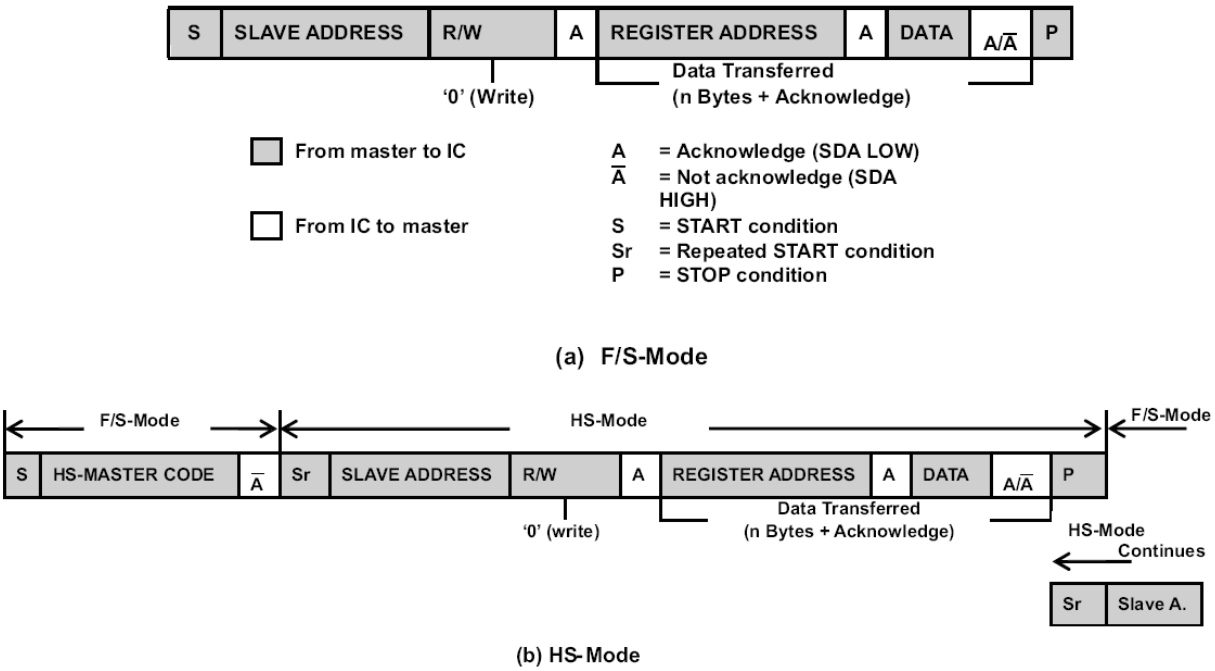


Figure 6. Bus Protocol

Register Description

Battery Charger Registers:

The SY20716D1 supports seven battery-charger registers that use either Write-Word or Read-Word protocols, as summarized in Table 1. The register at 03H is "read only" and can be used to identify the SY20716D1.

Table 1. Battery Charger Register Summary

Register Address	Register Name	Read/Write	Default
00H	Status/Control Register	Read or Write	x1xx 0xxx
01H	Control Register	Read or Write	0011 0000
02H	Control/Battery Voltage Register	Read or Write	0000 1010
03H	Vendor/Part Number/Rev Register	Read-only	0101 0xxx
04H	Constant/Termination Charge Current Register	Read or Write	0000 0001
05H	Adaptive IIN Threshold /ENB Pin Status Register	Read or Write	000x x100
06H	Safety Limit Register	Read or Write	0100 0000

Table 2. Status/Control Register (00H)

Bit	Bit Name	R/W	Description
7	OTG	R	OTG status, 0: OTG pin is low, 1: OTG pin is high
6	STAT_Enable	R/W	0: Disable STAT pin function 1: Enable STAT pin function (default)
5:4	Status	R	00: Ready 01: Charge in progress 10: Charge done 11: Fault
3	Boost	R	1: In Boost mode 0: Not in Boost mode
2:0	Fault	R	Charge mode 000: Normal, 001: VBUS OVP, 010: Auto Shutdown, 011: Bad Input Source or VBUS UVLO 100: Output OVP, 101: Thermal shutdown, 110: NA, 111: No battery Boost mode 000: Normal, 001: VBUS OVP, 010: Over load, 011: Battery voltage is too low, 100: Battery OVP, 101: Thermal shutdown, 110: NA, 111: NA

Table 3. Control Register (01H)

Bit	Bit Name	R/W	Description
7:6	IIN_Limit	R/W	00: USB input with 100mA current limit (default) 01: USB input with 500mA current limit 10: USB input or Adapter with 800mA current limit

Bit	Bit Name	R/W	Description
			11: No input current limit
5:4	BAT_Weak	R/W	00: 3.4V battery weak threshold 01: 3.5V battery weak threshold 10: 3.6V battery weak threshold 11: 3.7V battery weak threshold (default)
3	Termination_Enable	R/w	0: Disable charge current termination (default) 1: Enable charge current termination
2	Charge_Disable	R/W	0: Enable charger (default) 1: Disable charger
1	HZ_Mode	R/W	0: Not high impedance mode (default) 1: High impedance mode
0	OPA_Mode	R/W	0: Charger mode (default) 1: Boost mode

Table 4. Control/Battery Voltage Register (02H)

Bit	Bit Name	R/W	Description
7:2	Charge_Voltage	R/W	000000: 3.50V charge voltage (step is 20mV) 000001: 3.52V charge voltage 000010: 3.54V charge voltage (default) 000011: 3.56V charge voltage …… 101111: 4.44V charge voltage …… 111111: 4.44V charge voltage
1	OTG_Level_Select	R/W	0: OTG pin active low 1: OTG pin active high (default) Not applicable to OTG pin control of current limit at POR in host mode.
0	OTG_Enable	R/W	0: Disable OTG (default) 1: Enable OTG Not applicable to OTG pin control of current limit at POR in host mode.

Table 5. Vendor/PN/Rev Register (03H)

Bit	Bit Name	R/W	Description
7:5	Vendor_Code	R	010: Identifes a Silergy device
4:3	PN	R	10: SY20716
2:0	Revision	R	001: Revision 0.0 010-111: Future Revisions

Table 6. Constant/Termination Charge Current Register (04H)

Bit	Bit Name	R/W	Description
7	Reset	R/W	W: write 1 to reset the configurable charge parameters.
6:4	ICHG_Reference	R/W	000: 37.4mV for charge current regulation (default) (step is 6.8mV) 001: 44.2mV for charge current regulation 010: 51.0mV for charge current regulation …… 111: 85mV for charge current regulation
3	NA	R/W	Not used, 1 default
2:0	ITERM_Reference	R/W	000: 3.4mV for termination current (step is 3.4mV) 001: 6.8mV for termination current (default) 010: 10.2mV for termination current …… 111: 27.2mV for termination current

Table 7. Adaptive IIN Threshold/ENB Pin Status Register (05H)

Bit	Bit Name	R/W	Description
7	NA	R/W	Not used, 0 default
6	FAC_MODE	R/W	0:Disable factory test mode(default) 1:Enable factory test mode
5	Low_Charge	R/W	0: Normal charge current reference at 04H(default) 1: 22.1mV low charge current reference
4	Adaptive_IIN_Limit	R	0: Adaptive current limit or input current limit is not active 1: Adaptive current limit or input current limit is active
3	ENB_Status	R	0: ENB Pin is low 1: ENB Pin is high
2:0	Adaptive_IIN_Threshold	R/W	000: 4.20V special charge voltage 001: 4.28V special charge voltage …… 100: 4.52V special charge voltage (default) …… 111: 4.76V special charge voltage

Table 8. Safety Limit Register (06H)

Bit	Bit Name	R/W	Description
7:4	MAX_Charge_Current	R/W	0000: 37.4mV for max charge current reference (step is 6.8mV) 0001: 44.2mV for max charge current reference …… 0100: 64.6mV for max charge current reference (default) …… 1010: 105.4mV for max charge current reference …… 1111: 105.4mV for max charge current reference
3:0	MAX_Charge_Voltage	R/W	0000: 4.20V maximum charge voltage (default) (step is 20mV) 0001: 4.22V maximum charge voltage

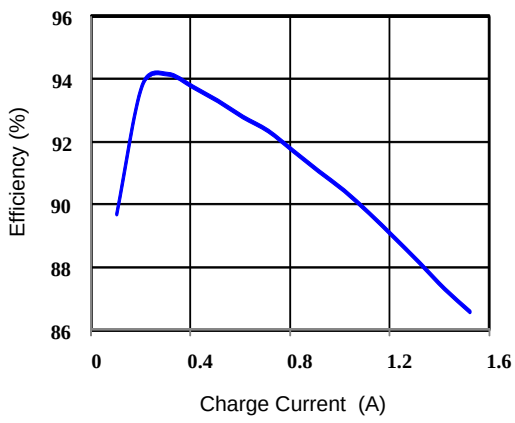
Bit	Bit Name	R/W	Description
			…… 1100: 4.44V maximum charge voltage …… 1111: 4.44V maximum charge voltage

The safety limit register resets when the battery voltage (VBAT) falls below the VSHORT threshold. After this reset, the limit values can be reprogrammed. However, any subsequent writing to other registers will lock these safety limits. Values in the 02H register (charge voltage) and the 04H register (charge current) that exceed these safety limits will be disregarded.

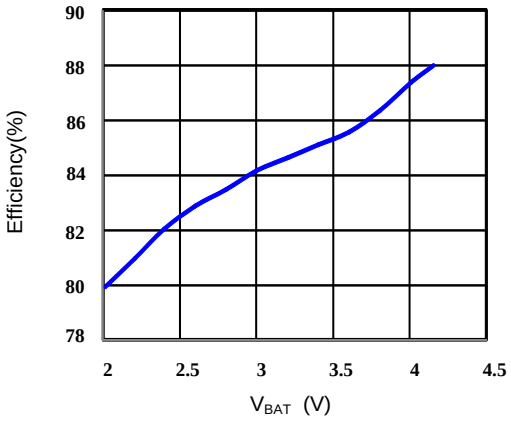
Typical Performance Characteristics

(T_A=25°C, V_{IN}=5V, R_{SEN}=55mΩ, 1cell battery, unless otherwise specified.)

Efficiency vs. Charge Current (CV mode)

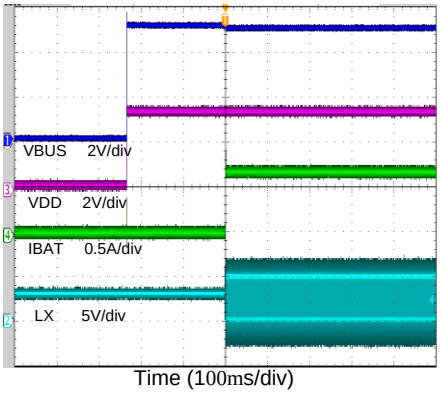


Efficiency vs. Charge Voltage (CC mode)



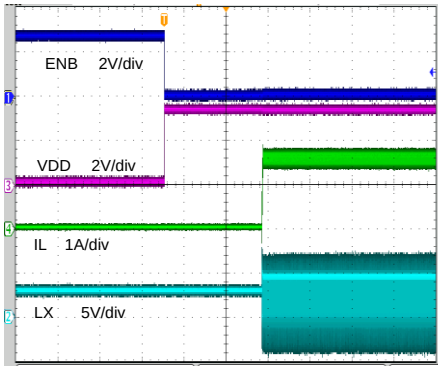
Power On

（VBUS=5V VBAT=3.4V host Mode）



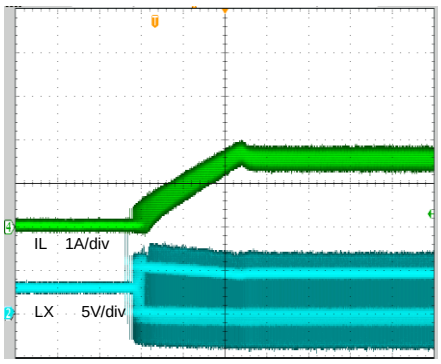
ENB On

（VBUS=5V VBAT=3.4V host Mode）



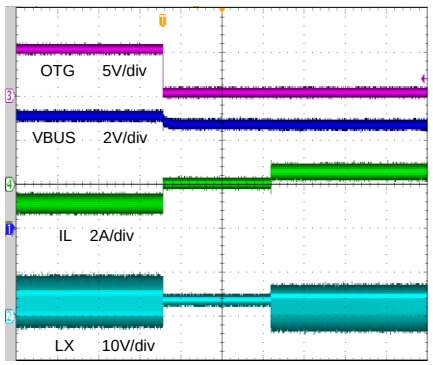
Charger Soft Start

（VBUS=5V VBAT=3.4V ICHG=1.55A host Mode）



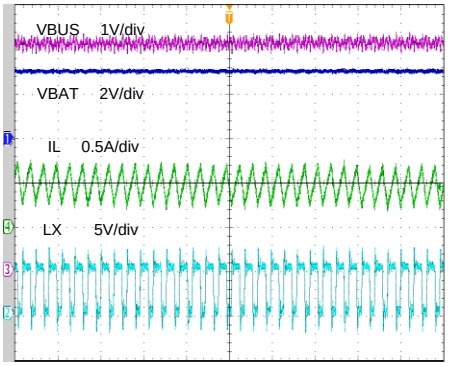
Boost To Charge Mode Transition

（VBUS connects 4.5V power supply, VBAT=3.6V OTG Control）



Constant Current Charge State

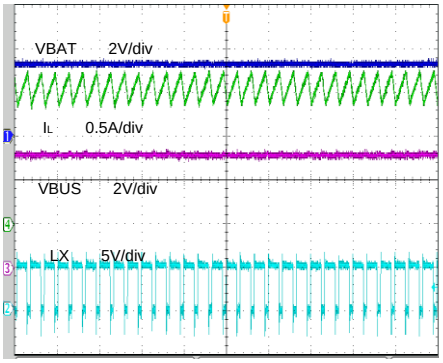
（VBUS=5V VBAT=3.2V Low charge 402mA）



Time (1μs/div)

Constant Current Charge State

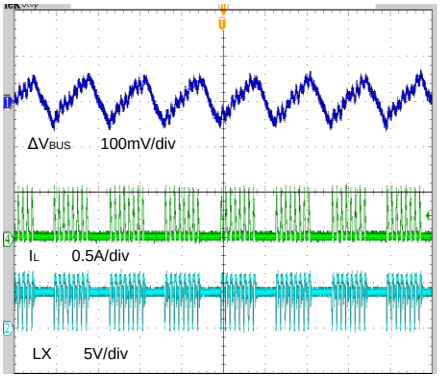
(VBUS=5V VBAT=3.2V ICHG=1.55A)



Time (1μs/div)

Boost Mode Light Load State

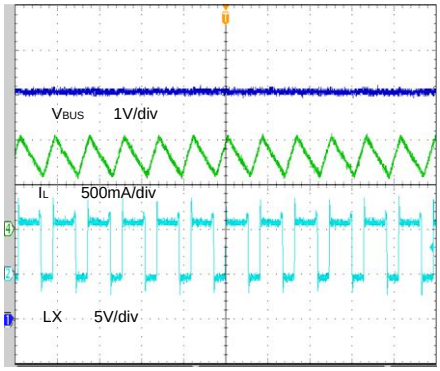
(VBAT=3.6V IBUS=0.05A)



Time (10μs/div)

Boost Mode Full Load State

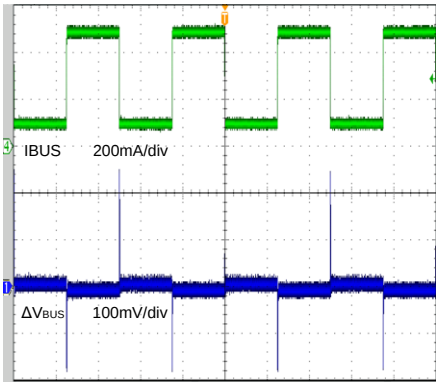
(VBAT=3.6V IBUS=0.5A)



Time (0.4μs/div)

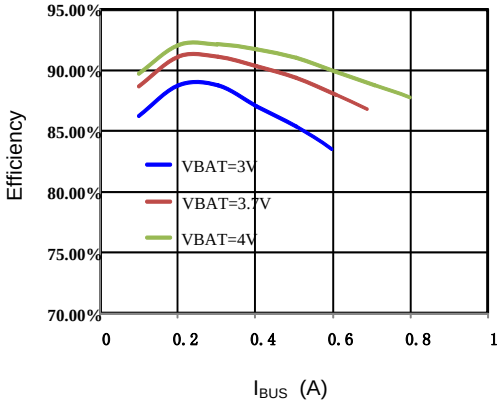
Boost Mode Load transient

(VBAT=3.6V IBUS=0.1A~0.5A)



Time (4ms/div)

Efficiency vs. Load current (Boost mode)



Application Information

The battery charger design outlined below corresponds to the Schematic Diagram shown in Figure 1. This section describes how to select the external components, such as the inductor, input and output capacitors, and the sense resistor.

Charging Current Sense Resistor R_{SEN}:

The termination and charge current depend on the sense resistor R_{SEN}. The reference voltage range for the termination current is 3.4mV to 27.2mV, and the reference voltage range for the charge current is 37.4mV to 85mV.

The termination current can be calculated using the following formula:

$$I_{TERM} = \frac{V_{TERM}}{R_{SEN}}$$

Where:

- V_{TERM} is set by register04, Bit [2:0].
- Units are in mΩ

The charge current can be calculated using the following formula:

$$I_{CHG} = \frac{V_{CHG}}{R_{SEN}}$$

Where:

- V_{CHG} is set by register04, Bit [6:4].
- Units are in mΩ

For example, when R_{SEN} = 55mΩ, the constant current is:

REG04[6:4]	V_{CHG}/mV	I_{CHG}/mA
000	37.4	680
001	44.2	804
010	51	927
011	57.8	1051
100	64.6	1175
101	71.4	1298
110	78.2	1422
111	85	1545

The termination current is:

REG04[6:4]	V_{CHG} (mV)	I_{CHG} (mA)
000	37.4	680
001	44.2	804
010	51	927
011	57.8	1051
100	64.6	1175
101	71.4	1298
110	78.2	1422
111	85	1545

Inductor Selection:

Higher switching frequency allows the use of smaller inductor and capacitor values. The inductor saturation current should be higher than the maximum charging current.

(I_{CHG}) plus half the ripple current (I_{Ripple}):

$$I_{SAT} \geq I_{CHG} + \frac{1}{2} \times I_{Ripple}$$

The inductor ripple current depends on the input voltage (V_{VBUS}), duty cycle (D = V_{BAT}/V_{VBUS}), switching frequency (f_{SW}), and inductance (L):

$$I_{Ripple} = \frac{V_{VBUS} \times D \times (1-D)}{f_{SW} \times L}$$

The maximum inductor ripple current happens with D = 0.5 or close to 0.5. Usually, inductor ripple is designed in the range of (20-40%) maximum charging current as a trade-off between inductor size and efficiency for a practical design.

Output Capacitor Selection:

In parallel with the battery, the output capacitor absorbs the high frequency switching ripple current and smooths the output voltage.

The RMS value of the output ripple current I_{RMS} is calculated as follows:

$$I_{RMS} = \frac{V_{VBUS}}{2\sqrt{3} \times L \times f_{SW}} \times D \times (1-D)$$

Where:

- the duty cycle D is the ratio of the output voltage (battery voltage) over the input voltage for CCM mode, which is a typical operation for the battery

charger.

It's recommended to use a typical 22μF low ESR ceramic capacitor capable of handling the ripple current. When necessary, multiple capacitors can be used in parallel to increase the ripple handling capability.

Input Capacitor Selection:

The input capacitor absorbs the input ripple current from the buck converter, which is given by the equation below:

$$I_{RMS} = I_{CHG} \times \frac{\sqrt{V_{BAT} \times (V_{VBUS} - V_{BAT})}}{V_{VBUS}}$$

This RMS ripple current must be smaller than the rated RMS current in the capacitor datasheet. Non-tantalum chemistries (ceramic, aluminum, or OSCON) are preferred due to their resistance to power-up surge currents when the AC-adapter is plugged into the battery charger.

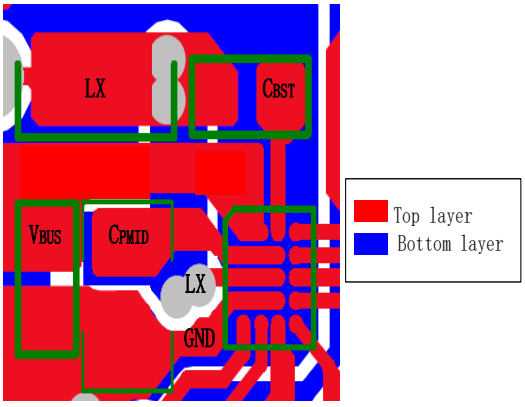
For notebook battery charger applications, it is recommended to use ceramic capacitors or polymer capacitors due to their small size and reasonable cost.

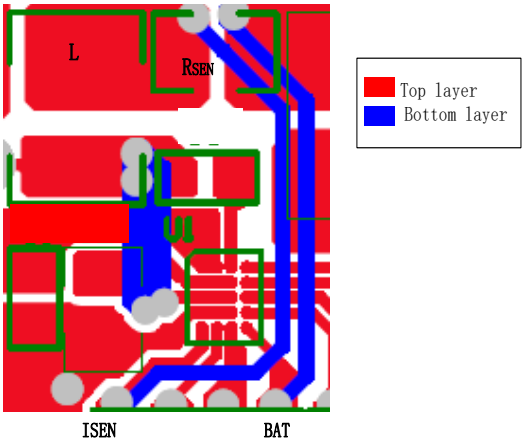
PCB Layout Guide:

For best performance of the SY20716D, the following guidelines must be followed:

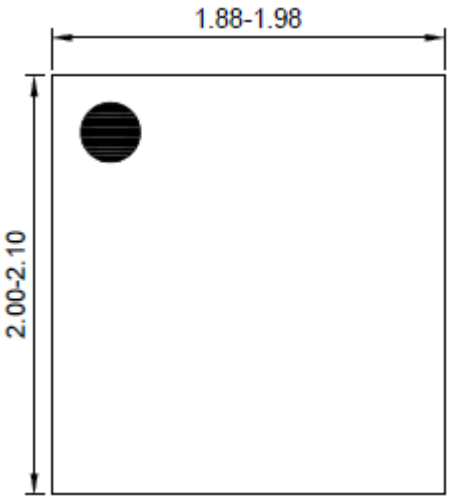
1. Enhance thermal and noise performance by maximizing the PCB copper area connected to the GND pin. Where board space permits, a ground plane is highly recommended.
2. For the best efficiency and minimum noise problems, the following components should be placed close to the device: C_{VBUS}, C_{PMID}, and C_{BST}.
3. Minimize the loop area formed by CPMID and GND. Also, keep the PCB copper area associated with the LX pin as small as possible to mitigate potential noise issues.
4. Position the sense resistor close to the junction of the inductor and the output capacitor. The route from the sense leads on the sense resistor back to the device should be kept close to minimize the loop area. Avoid routing the sense leads through high-current paths.

   Refer to the images below for the recommended layout design of the inductor (L), CVBUS, CPMID, and CBST:

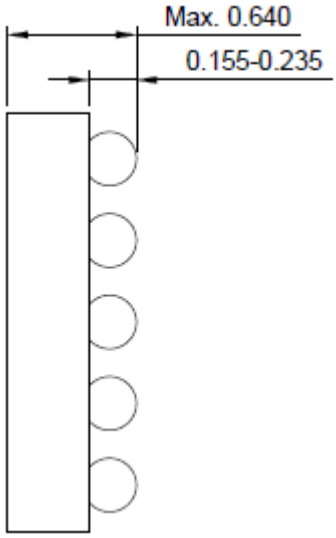




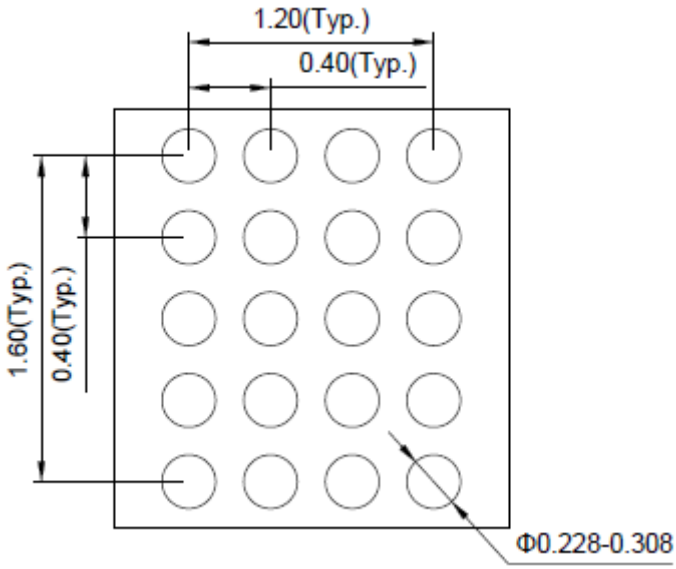
CSP1.93x2.05-20 Package Outline Drawing



Top View



Side View

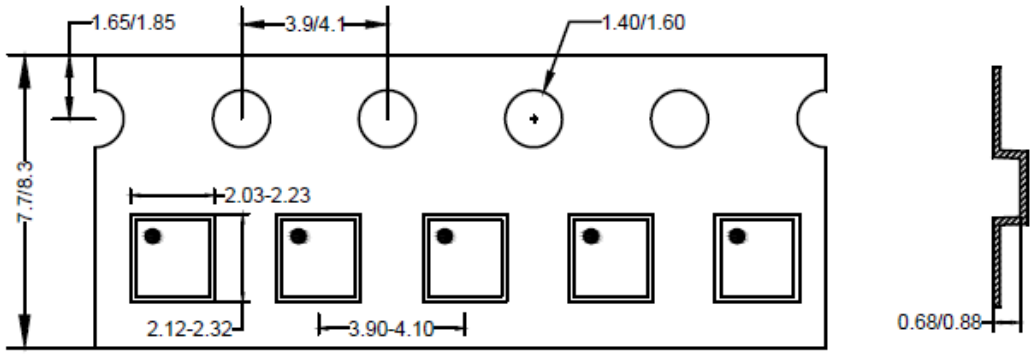


Bottom View

Note: All dimensions are in millimeters and exclude mold flash and metal burr.

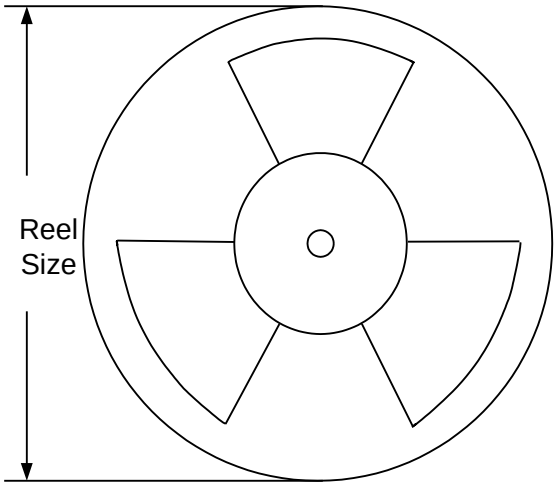
Taping & Reel Specification

CSP1.93x2.05 Taping Orientation



Feeding direction ⟶

Carrier Tape & Reel Specification for Packages



Package types	Tape width (mm)	Pocket pitch (mm)	Reel size (Inch)	Trailer length (mm)	Leader length (mm)	Qty per reel
CSP1.93x2.05	8	4	7"	400	160	3000

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