SY21061

High Efficiency, 800kHz, 1.2A, 40V Input Asynchronous Buck Converter

General Description

The SY21061 high-efficiency asynchronous Buck converter can deliver 1.2A output current over a wide input voltage range from 5V to 40V. The SY21061 employs a constant off-time and peak current mode control strategy to achieve fast transient responses. It integrates a main switch with low $R_{DS(ON)}$ to minimize conduction loss.

The 800kHz switching frequency permits low output voltage ripple and reduces external inductor and capacitor sizes. The SY21061 also provides cycle-by-cycle current limiting, over temperature protection, and output short circuit protection.

The SY21061 is available in a compact SOT23-6 package.

Features

- Low $R_{DS(ON)}$ for Internal N-channel Power FET: 180mΩ
- 5V to 40V Input Voltage Range
- Up to 1.2A Output Current
- 800kHz Switching Frequency
- Constant Off-Time and Peak Current Mode Control
- Internal Soft-Start Limits Inrush Current
- ±2% 0.6V Reference
- Output Short Circuit Protection
- Cycle-by-Cycle Peak Current Limit
- Over Temperature Protection
- RoHS-Compliant and Halogen-Free
- Compact SOT23-6 Package

Applications

- Smart Meter
- Set Top Box
- Portable TV
- Access Point Router
- DSL Modem
- LCD TV

Typical Application

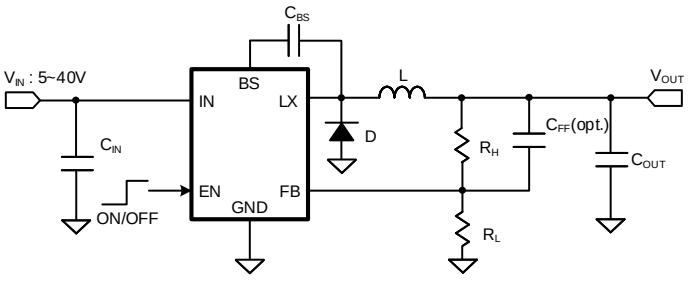


Figure 1. Typical Application Circuit

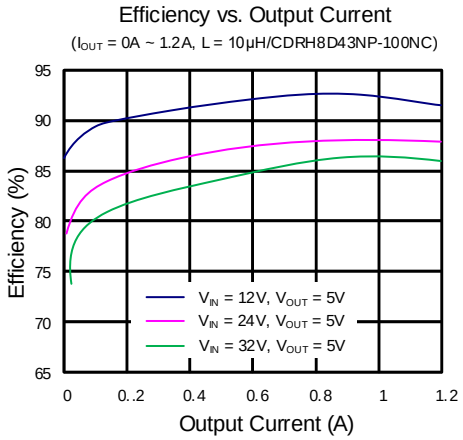


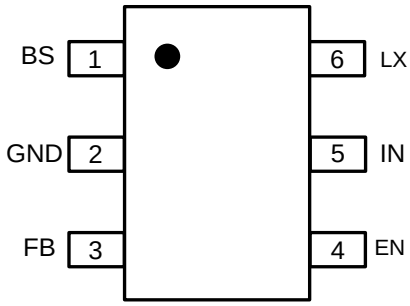
Figure 2. Efficiency vs. Output Current

Ordering Information

Ordering Part Number	Package type	Top Mark
SY21061ABC	SOT23-6 RoHS-Compliant and Halogen-Free	**YM*xyz***

x = year code, y = week code, z = lot number code

Pinout (top view)



Pin Description

Pin No	Pin Name	Pin Description
1	BS	Bootstrap pin. Supply for high-side gate driver. Connect a 0.1µF ceramic capacitor between the BS and LX pin.
2	GND	Ground pin.
3	FB	Output feedback pin. Connect this pin to the center point of the output resistor-divider as shown in Figure 1. $V_{OUT} = 0.6 \times (1 + R_H/R_L)$.
4	EN	Enable pin. Pull low to disable the device, pull high to enable. Do not leave this pin floating.
5	IN	Power input. Decouple this pin from the GND pin with at least a 2.2µF ceramic capacitor.
6	LX	Inductor pin. Connect this pin to the switching node of inductor and rectifier diode.

Block Diagram

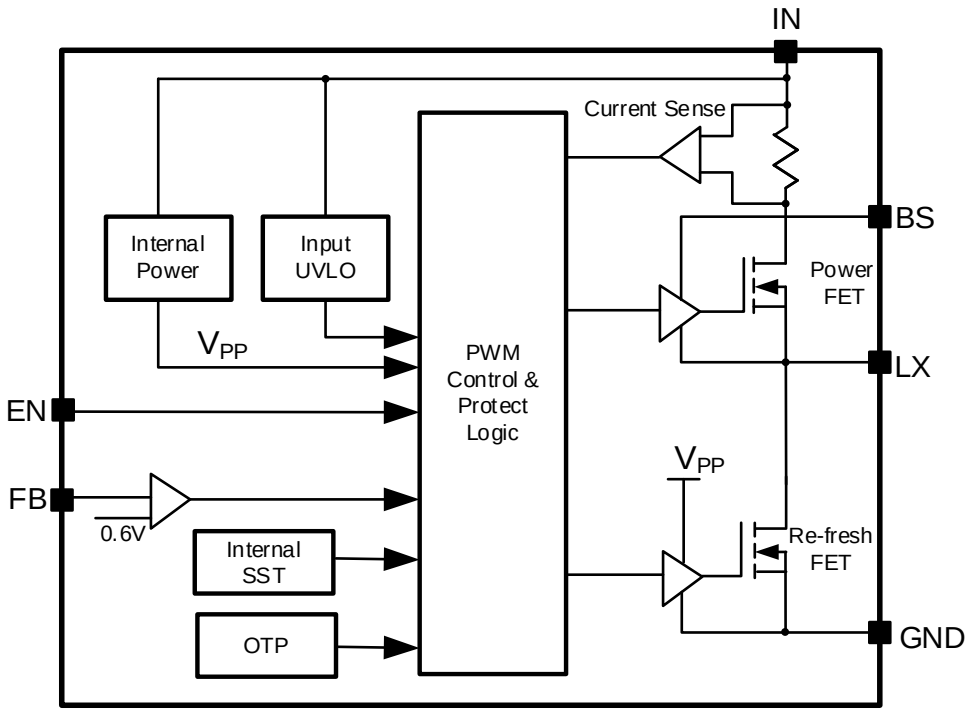


Figure 3. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
IN, LX	-0.3	42	V
EN	-0.3	V_{IN} + 0.6	
FB, BS-LX	-0.3	3.6	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering,10sec.)		260	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-ambient Thermal Resistance	170	°C/W
θ_{JC} Junction-to-case Thermal Resistance	130	
P_D Power Dissipation T_A=25°C	0.6	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
IN	5	40	V
BS-LX		3.3	
Output Current		1.2	A
Junction Temperature	-40	125	°C
Ambient Temperature	-40	85	

Electrical Characteristics

(V_{IN} = 12V, V_{OUT} = 5V, L = 10μH, C_{OUT} = 22μF, T_A = 25°C, I_{OUT} = 0.5A unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input	Voltage Range	V_{IN}		5		40	V
	UVLO Rising Threshold	$V_{IN,UVLO}$	Rising		4.5		
	UVLO Hysteresis	$V_{IN,HYS}$			200		mV
	Quiescent Current	I_Q	I_{OUT} = 0A, V_{FB} = V_{REF}×105%		160		μA
	Shutdown Current	I_{SHDN}	EN = Low			10	
Output	Reference Voltage	V_{REF}		0.588	0.6	0.612	V
	FB input Current	I_{FB}	V_{FB} = V_{IN}	-50		50	nA
	Soft-Start Time	t_{SS}	(Note 4)		400		μs
MOSFET	Power FET $R_{DS(ON)}$	$R_{DS(ON)}$			180		mΩ
	Power FET Current Limit	I_{LIM}	V_{FB} = V_{REF}×98%	1.6		2	A
Enable (EN)	Input Voltage High	$V_{EN,H}$		1.5			V
	Input Voltage Low	$V_{EN,L}$				0.4	
Frequency	Switching Frequency	f_{SW}			800		kHz
	Minimum On-time	$t_{ON,MIN}$	(Note 4)			100	ns
	Maximum On-time	$t_{ON,MAX}$			2		μs
	Minimum Off-time	$t_{OFF,MIN}$				100	ns
OTP	Temperature	T_{OTP}	(Note 4)		150		°C
	Temperature Hysteresis	T_{HYS}	(Note 4)		15		

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions.

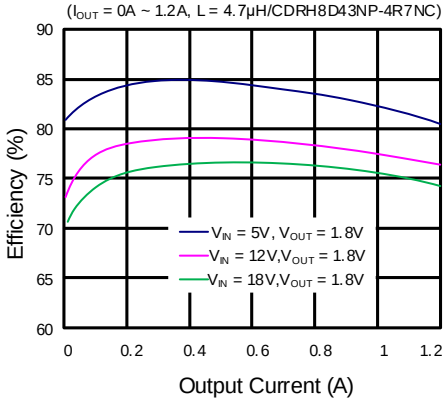
Note 4: Guaranteed by design.

Typical Performance Characteristics

(T_A = 25°C, V_{IN} = 12V, V_{OUT} = 5V, L = 10μH, C_{OUT} = 22μF, unless otherwise specified)

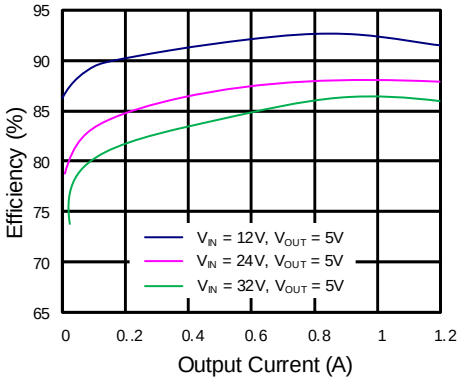
Efficiency vs. Output Current

(I_{OUT} = 0A ~ 1.2A, L = 4.7μH/CDRH8D43NP-4R7NC)



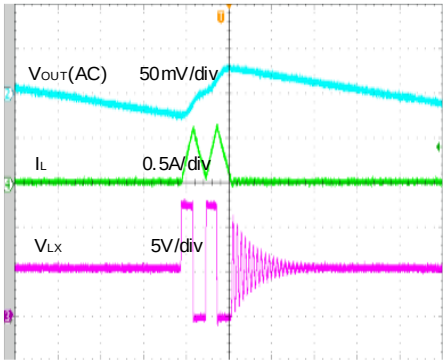
Efficiency vs. Output Current

(I_{OUT} = 0A ~ 1.2A, L = 10μH/CDRH8D43NP-100NC)



Output Ripple

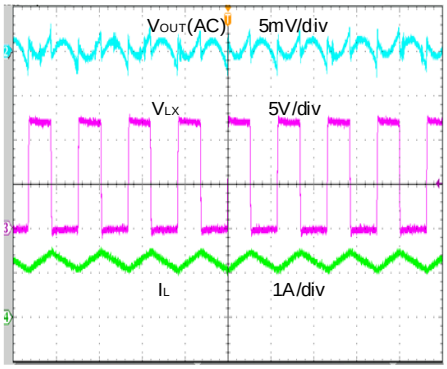
(V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 0.05A)



Time (2μs/div)

Output Ripple

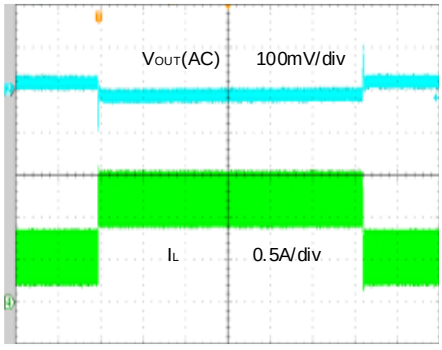
(V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 1.2A)



Time (1μs/div)

Load Transient

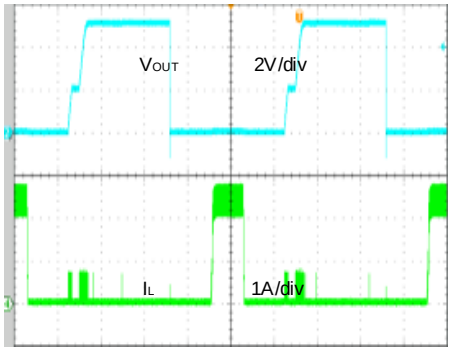
(V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 0.5A ~ 1.2A)



Time (800μs/div)

Short Circuit Protection

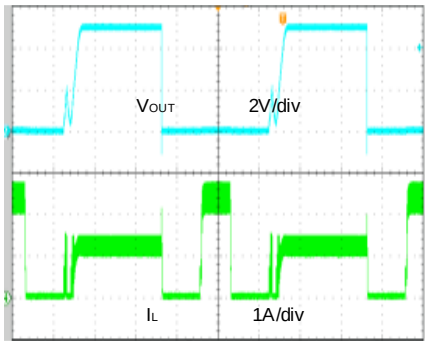
(V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 0A ~ Short)



Time (2ms/div)

Short Circuit Protection

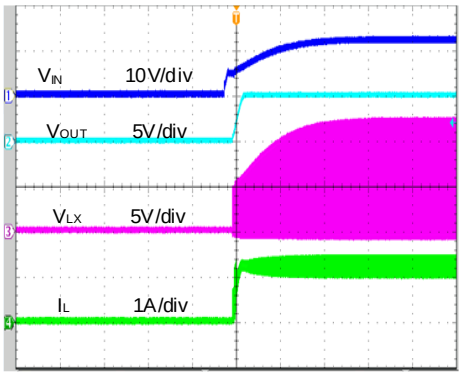
(V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 1.2A ~ Short)



Time (2ms/div)

Startup from V_{IN}

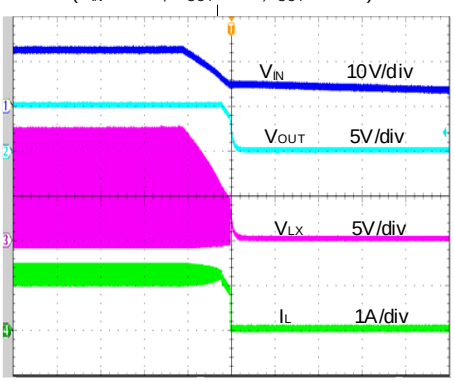
(V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 1.2A)



Time (2ms/div)

Shutdown from V_{IN}

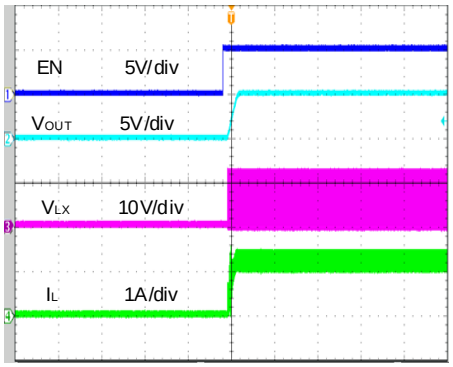
(V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 1.2A)



Time (2ms/div)

Startup from Enable

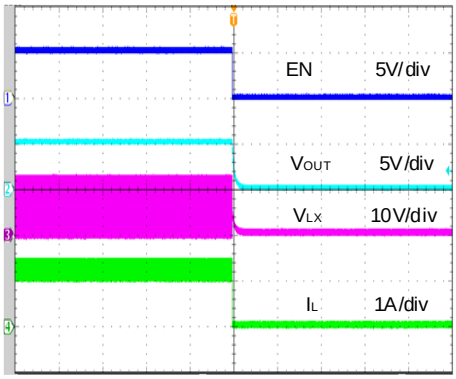
(V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 1.2A)



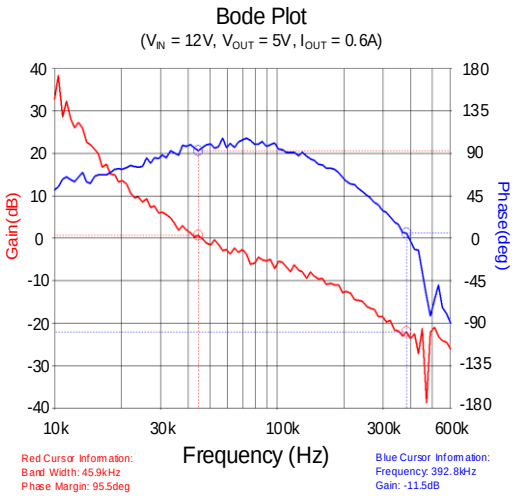
Time (2ms/div)

Shutdown from Enable

(V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 1.2A)



Time (2ms/div)



Detailed Description

The SY21061 high-efficiency asynchronous Buck converter can deliver 1.2A output current over a wide input voltage range from 5V to 40V. It integrates a power FET with low $R_{DS(ON)}$ to minimize conduction loss.

The 800kHz switching frequency permits low output voltage ripple and reduces external inductor and capacitor sizes. The SY21061 also provides cycle-by-cycle current limiting, over temperature protection and output short circuit protection.

The SY21061 employs a constant off-time and peak-current mode control strategy. When the power FET's current-sense signal reaches internal V_{COMP}, the power FET turns off for a fixed period of time (constant off-time). t_{OFF} is internally calculated according to the input voltage, output voltage, and desired switching frequency (f_{SW}):

$$t_{OFF} = \frac{1 - V_{OUT}/V_{IN}}{f_{SW}}$$

The power FET turns on after a period of t_{OFF}.

Enable Control

The EN input is a high-voltage capable input with logic-compatible threshold. When EN is driven higher than 1.5V, normal device operation is enabled. When driven to lower than 0.4V, the device will shut down, reducing input current to less than 10μA.

Fault-Protection Modes

Output Current Limit

With load current increasing, as soon as the power FET current exceeds the peak current-limit threshold, the power FET will turn off. If the load current continues to increase, the output voltage will drop.

Output Under Voltage Protection

With output current increasing, as soon as the power switch current exceeds the peak current limit threshold, the power switch will turn off. If the load current continues to increase, the output voltage will drop. When the output voltage falls below 33% of the regulated level, the output undervoltage protection will be activated and the device will operate in hiccup mode. The hiccup on-time is 1.5ms, and the hiccup off-time is 1.5ms. If the hard short condition is removed, the device will return to normal operation.

Overtemperature Protection (OTP)

The device includes overtemperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. This will shut down the device when the junction temperature exceeds 150°C. Once the junction temperature cools by approximately 15°C, the device will resume normal operation after a complete soft-start cycle. For continuous operation, provide adequate cooling so that the junction temperature does not exceed the OTP threshold.

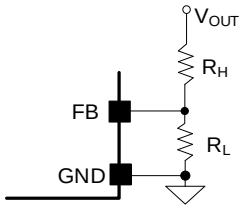
Application Information

The following paragraphs describe the selection process for the feedback resistors (R_H and R_L), input capacitor C_{IN}, output inductor L, output capacitor C_{OUT}, bootstrap capacitor and rectifier diode D.

Feedback Resistor-Divider R_H and R_L

Choose R_H and R_L to program the proper output voltage. Choose large resistance values between 10kΩ and 1MΩ for both R_H and R_L to minimize power consumption under light loads. If V_{OUT} is 5V, a value of 100kΩ is chosen for R_H, then using the following equation, R_L can be calculated as 13.7kΩ:

$$R_L = \frac{0.6V}{V_{OUT}\text{-}0.6V} R_H$$



Input Capacitor C_{IN}

For the best performance, select a typical X5R or better grade ceramic capacitor with a 50V rating and at least 2.2μF capacitance. The capacitor should be placed as close as possible to the device, while also minimizing the loop area formed by C_{IN} and the IN/GND pins.

When selecting an input capacitor, ensure that its voltage rating is at least 20% greater than the maximum voltage of the input supply. X5R or X7R dielectric types are the most often selected due to their small size, low cost, surge current capability, and high RMS current rating over a wide temperature and voltage range.

In situations where the input rail is supplied through long wires, it is recommended to add some bulk capacitance like electrolytic, tantalum or polymer type capacitors to reduce the overshoot and ringing caused by the added parasitic inductance.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1-D)}$$

The worst-case condition occurs at D = 0.5, then

$$I_{CIN\_RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplicity, use an input capacitor with an RMS current rating greater than 50% of the maximum load current.

The input capacitor value determines the input voltage ripple of the converter. If there is a voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification.

Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated using the formula:

$$V_{CIN\_RIPPLE,CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1-D)$$

The worst-case condition occurs at D = 0.5, then

$$V_{CIN\_RIPPLE,CAP,MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. A single 2.2μF X5R capacitor is sufficient in most applications.

Output Inductor L

Consider the following when choosing this inductor:

1) Choose the inductance to provide a ripple current that is approximately 40% of the maximum output current. The recommended inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT} / V_{IN,MAX})}{f_{sw} \times I_{OUT,MAX} \times 0.4}$$

Where f_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY21061 has high tolerance for ripple current amplitude variation. As a result, the final choice of inductance can vary slightly from the calculated value with no significant performance impact.

2) The inductor's saturation current rating must be greater than the peak inductor current under full load:

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{2 \times f_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. Choose an inductor with DCR less than 50mΩ to achieve good overall efficiency.

Output Capacitor C_{OUT}

Select the output capacitor C_{OUT} to handle the output ripple requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting the component. For the best performance, use an X5R or better grade ceramic capacitor with a 25V rating and capacitance greater than 22μF.

For applications where the design must meet stringent ripple requirements, the following considerations must be followed:

The output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔI_L) on the output capacitor's ESR (ESR ripple), as well as the stored charge (capacitive ripple).

When calculating total ripple, consider both.

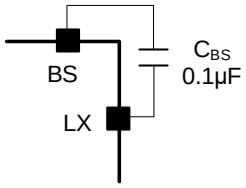
$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

The capacitive ripple might be higher because the effective capacitance for ceramic capacitors decreases with the voltage across the terminals. The voltage derating is usually included as a chart in the capacitor datasheet, and the ripple can be recalculated after taking the target output voltage into account.

External Bootstrap Capacitor

This external bootstrap capacitor provides the gate driver voltage for internal power MOSFET. A 0.1μF low-ESR ceramic capacitor connected between the BS pin and the LX pin is recommended.

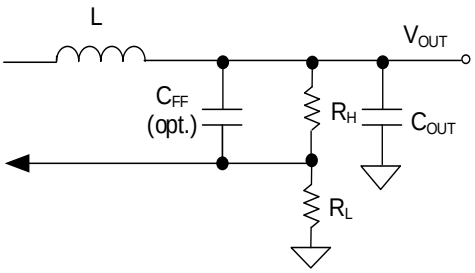


Rectifier Diode

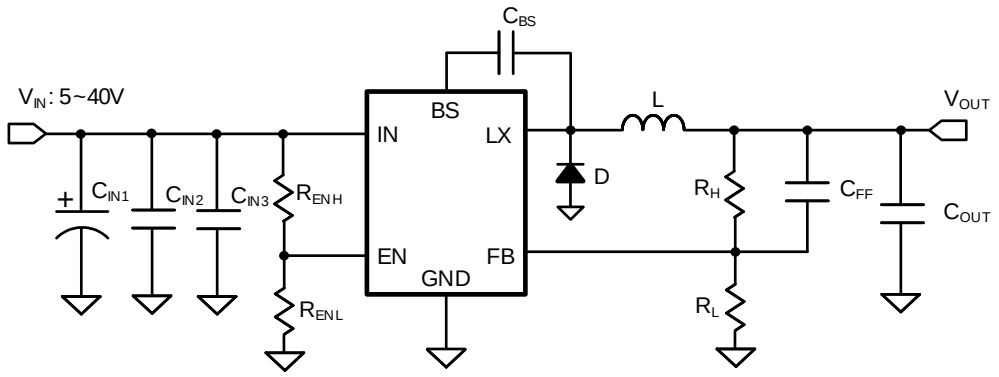
To accommodate the device high switching speed, choose a Schottky diode with low forward voltage and fast switching speed. The diode's voltage rating must be higher than the Buck converter maximum input voltage, and the diode's average and peak current rating should be greater than the Buck converter output average current and peak current.

Load Transient Consideration

The device integrates the compensation components to achieve good stability and fast transient responses. In some applications, adding a small ceramic capacitor in parallel with R_H may further speed up the load transient response. It is recommended for applications with large load transient step requirements.



Application Schematic (V_{OUT}=5V)



BOM List

Designator	Description	Part Number	Manufacturer
C_{IN1}	47μF/50V (electrolytic capacitor)		
C_{IN2}	2.2μF/50V/1206	C3216X7R1H225K	TDK
C_{IN3}, C_{BS}	0.1μF/50V/0603	C1608X7R1H104K	TDK
C_{OUT}	22μF/16V/1206	C3216X5R1C226K	TDK
C_{FF}	47pF/50V/0603	C1608C0G1H470J	TDK
D	3A/60V	SS36	
L	10μH/inductor, 3.2A	CDRH8D43NP-100NC	Sumida
R_H	100kΩ, 0603	RC0603FR-07100KL	
R_L	13.7kΩ, 0603	RC0603FR-0713K7L	
R_{ENH}	10kΩ, 1%, 0603		
R_{ENL}	1MΩ, 1%, 0603		

Recommend Table for Typical Applications

V_{OUT}(V)	R_H(kΩ)	R_L(kΩ)	C_{FF}(pF)	L/Part Number	C_{OUT}
1.2	100	100	22	4.7μH/CDRH8D43NP-4R7NC	22μF/16V,1206,X5R
3.3	100	22.1	47	6.8μH/CDRH8D43NP-6R8NC	22μF/16V,1206,X5R
5	100	13.7	47	10μH/CDRH8D43NP-100NC	22μF/16V,1206,X5R

Layout Design

Follow these PCB layout guidelines for optimal performance and thermal dissipation:

- **Input Capacitors:** Place the input capacitors close to the IN and GND pins, minimizing the loop formed by these connections. The input capacitor should be connected to the IN and GND using wide copper areas.
- **Output Capacitors:** Connect the C_{OUT} negative terminal to the GND pin using wide copper traces instead of vias, in order to achieve better accuracy and stability of output voltage.
- **Feedback Network:** Place the feedback components (R_H, R_L, and C_{FF}) as close to the FB pin as possible. Avoid routing the feedback line near LX, or other high-frequency signals as it is noise-sensitive. Use a Kelvin connection to connect with C_{OUT} rather than the inductor output terminal.
- **LX Connection:** Keep the LX area small to prevent excessive EMI, while providing a wide copper area to minimize parasitic resistance and inductance.
- **EN Signal:** It is not recommended to connect EN signal directly to V_{IN}. A resistor in a range of 1kΩ to 1MΩ should be used if the lines are pulled high to V_{IN}.
- **GND Vias:** Place an adequate number of vias on the GND layer around the device for better thermal performance. The exposed GND pad should be connected to a copper area larger than its size. Place multiple GND vias on it for heat dissipation.
- **PCB Board:** To achieve the best thermal and noise performance, maximize the PCB copper area connecting to the GND pin. A ground plane is highly recommended if board space allows. Connect the ground pad to a large copper area to enhance thermal performance.

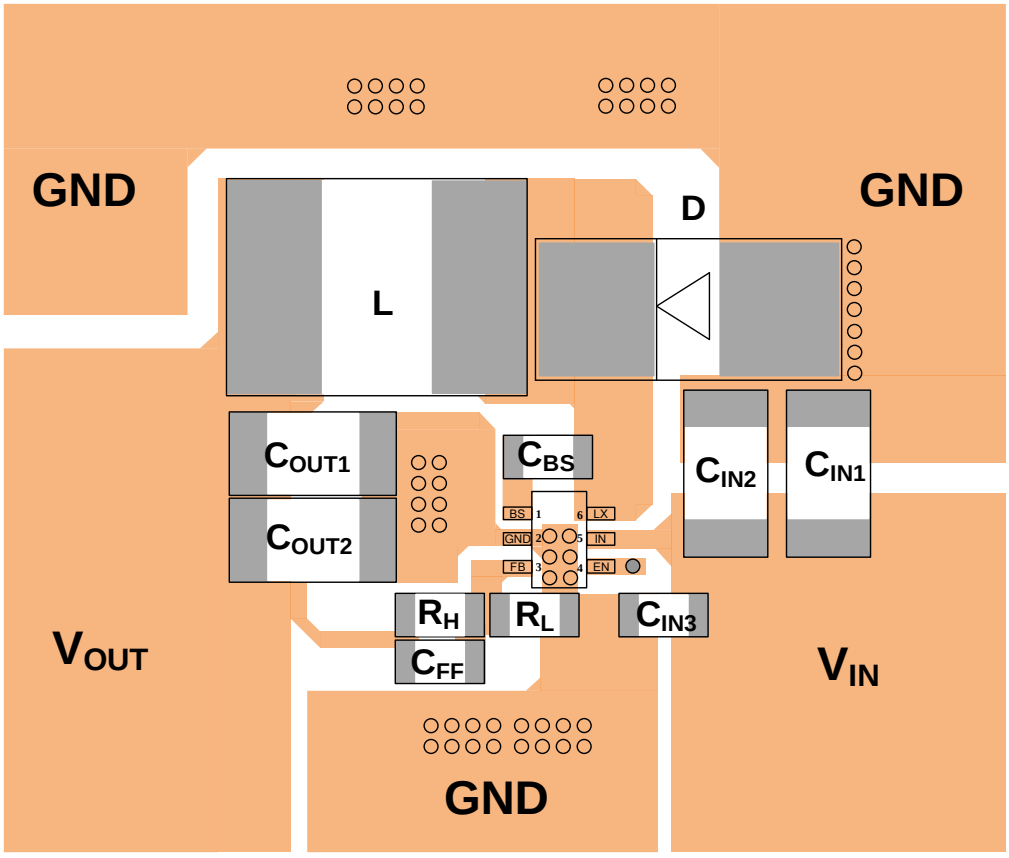
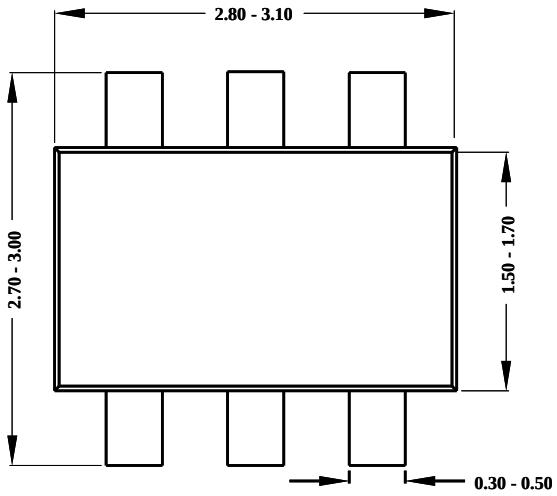
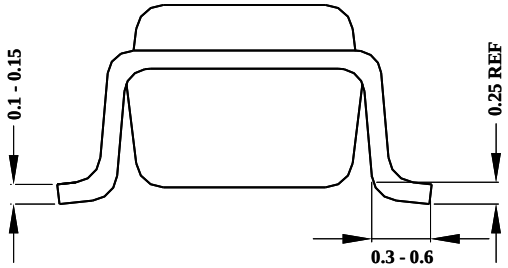


Figure 4. Suggested PCB Layout

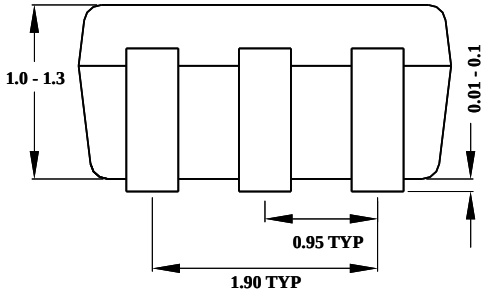
SOT23-6 Package Outline & PCB Layout



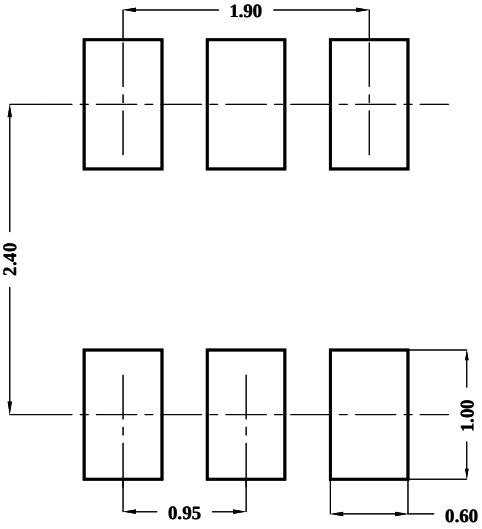
Top View



Side View



Side View

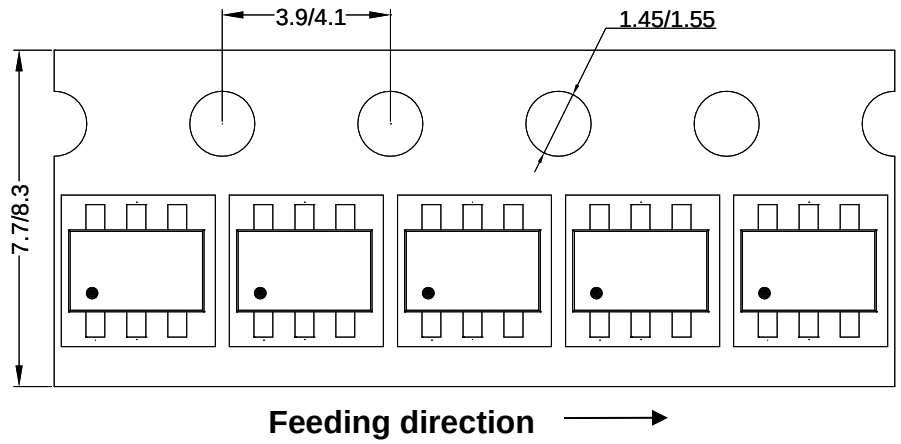


Recommended Pad Layout

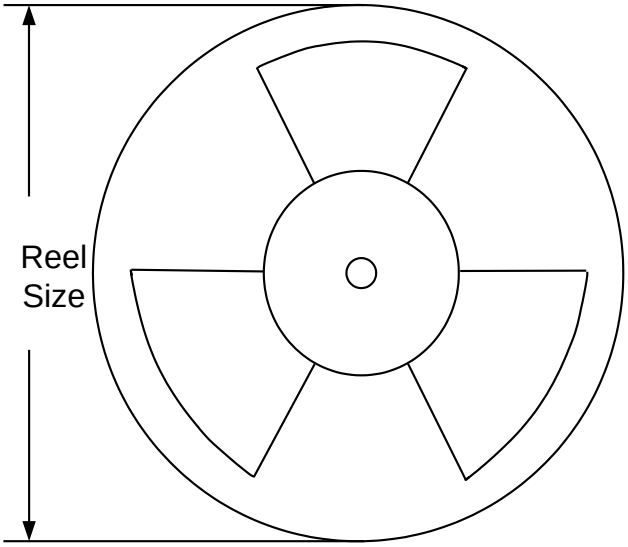
Notes: All dimension in millimeter and exclude mold flash & metal burr.

Taping & Reel Specification

SOT23-6 Taping Orientation



Carrier Tape & Reel Specification for Packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SOT23-6	8	4	7"	280	160	3000

Others: NA

Revision History

The revision history provided is for informational purposes only and is believed to be accurate; however, it is not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change
Nov. 16, 2014	Revision 0.9	Initial Release
Aug. 30, 2023	Revision 1.0	Production Release

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