SY21211

High Efficiency, Fast Response，5A, 30V Input Synchronous Buck Regulator with Accurate EN threshold

General Description

The SY21211, high efficiency synchronous step-down DC/DC converter is capable of delivering 5A output current while operating over a wide input voltage range from 4.5V to 30V. The device integrates very low $R_{DS(ON)}$ main and synchronous MOSFETs to minimize the conduction loss and deliver high efficiency.

The SY21211 uses the instant PWM architecture to achieve fast transient responses for high step-down ratio applications and high efficiency at light loads. In addition, it operates at pseudo-constant frequency of 500kHz under continuous conduction mode to minimize the size of inductor and capacitor.

The device is available in a 3mm x 4 mm DFN package.

Ordering Information

SY21211□(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY21211DNC	DFN4×3-12	--
SY21211FCC	SO8E	--

Features

- 4.5-30V Input Voltage Range
- 5A Continuous, 6A Peak Load Current Capability
- Low $R_{DS(ON)}$ for Internal Switches (Top/Bottom): 70 mΩ /40 mΩ
- Instant PWM Architecture to Achieve Fast Transient Responses
- External Soft-start Limits the Inrush Current
- Pseudo-constant Frequency: 500kHz at Heavy Loads
- 1.5% 0.6V Reference
- Output Over Current Limit
- Output Short Circuit Protection with Current Fold Back
- Thermal Shutdown and Auto Recovery
- RoHS Compliant and Halogen Free
- Compact Package: DFN4×3-12/SO8E

Applications

- LCD-TVs
- Set-Top Boxes
- Notebooks
- High Power AP Routers
- Storage
- Networking
-

Typical Applications

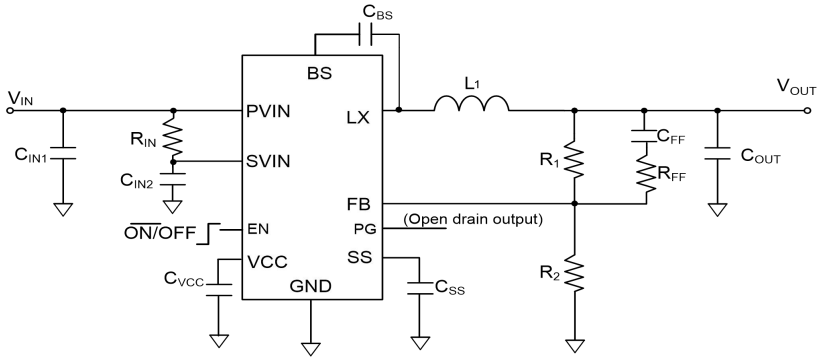


Figure1. Schematic Diagram (SY21211DNC)

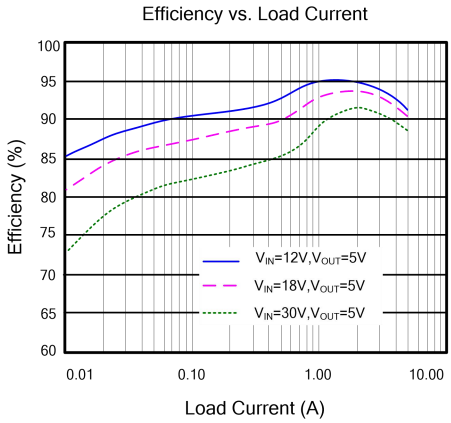


Figure2. Efficiency vs. Load Current (SY21211DNC)

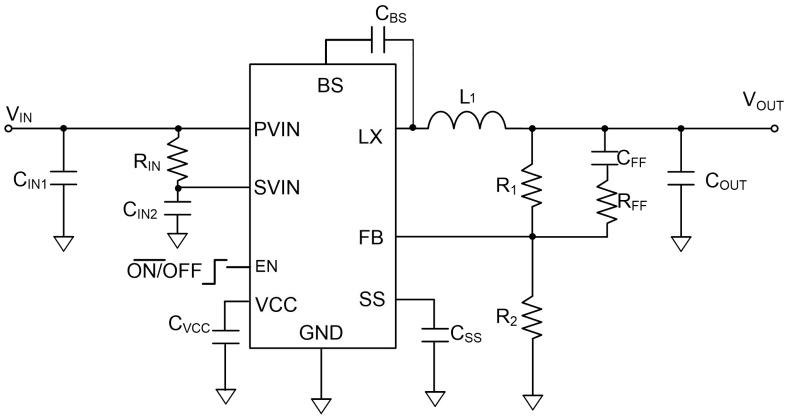


Figure3. Schematic Diagram (SY21211FCC)

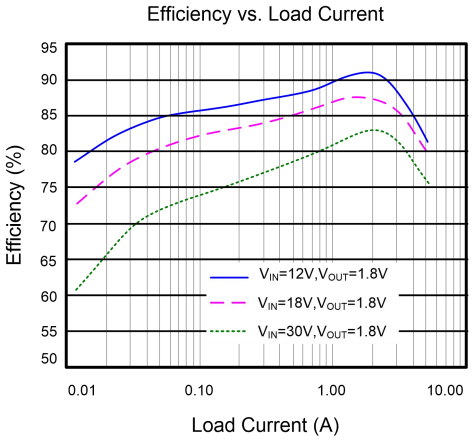
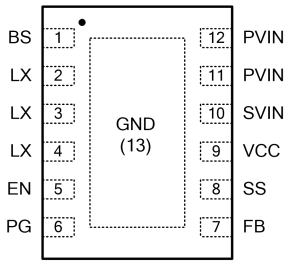
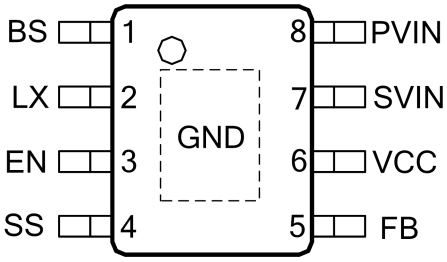


Figure4. Efficiency vs. Load Current (SY21211FCC)

Pinout (top view)



(DFN4×3-12)



(SO8E)

Top Mark: ADS***xyz*** for SY21211DNC (Device code: ADS, ***x=year code, y=week code, z= lot number code***)
AHH***xyz*** for SY21211FCC (Device code: AHH, ***x=year code, y=week code, z= lot number code***)

Pin Name	DFN4x3-12	SO8E	Pin Description
BS	1	1	Boot-strap pin. Supply high side gate driver. Connect a 0.1μF ceramic capacitor between this pin and the LX pin.
LX	2,3,4	2	Inductor pin. Connect this pin to the switching node of the inductor.
EN	5	3	Enable control input. The device has an accurate 1.2V rising threshold that allows the user to program an accurate turn-on threshold using a resistor divider, or adding a turn-on delay by using a low pass RC filter between the host and the pin.
PG	6	/	Power good Indicator. Open-drain output. Low output if the output voltage is less than 90% of target voltage, high-impedance otherwise.
FB	7	5	Output feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{OUT}=0.6\times(1+R_1/R_2)$
SS	8	4	Soft-start programming pin. Connect a capacitor from this pin to the ground to program the soft-start time. $t_{SS}=Css\times0.6V/10\mu A$
VCC	9	6	Internal 3.3V LDO output. Power supply for internal analog circuits and driving circuit. Add a 1μF bypass capacitor to the GND.
SVIN	10	7	Analog supply input. Bypass a 1μF capacitor to the ground.
PVIN	11,12	8	Power supply input. Decouple this pin to GND pin with at least a 10μF ceramic capacitor.
GND	Exposed Pad	Exposed Pad	Ground pin.

Function Block

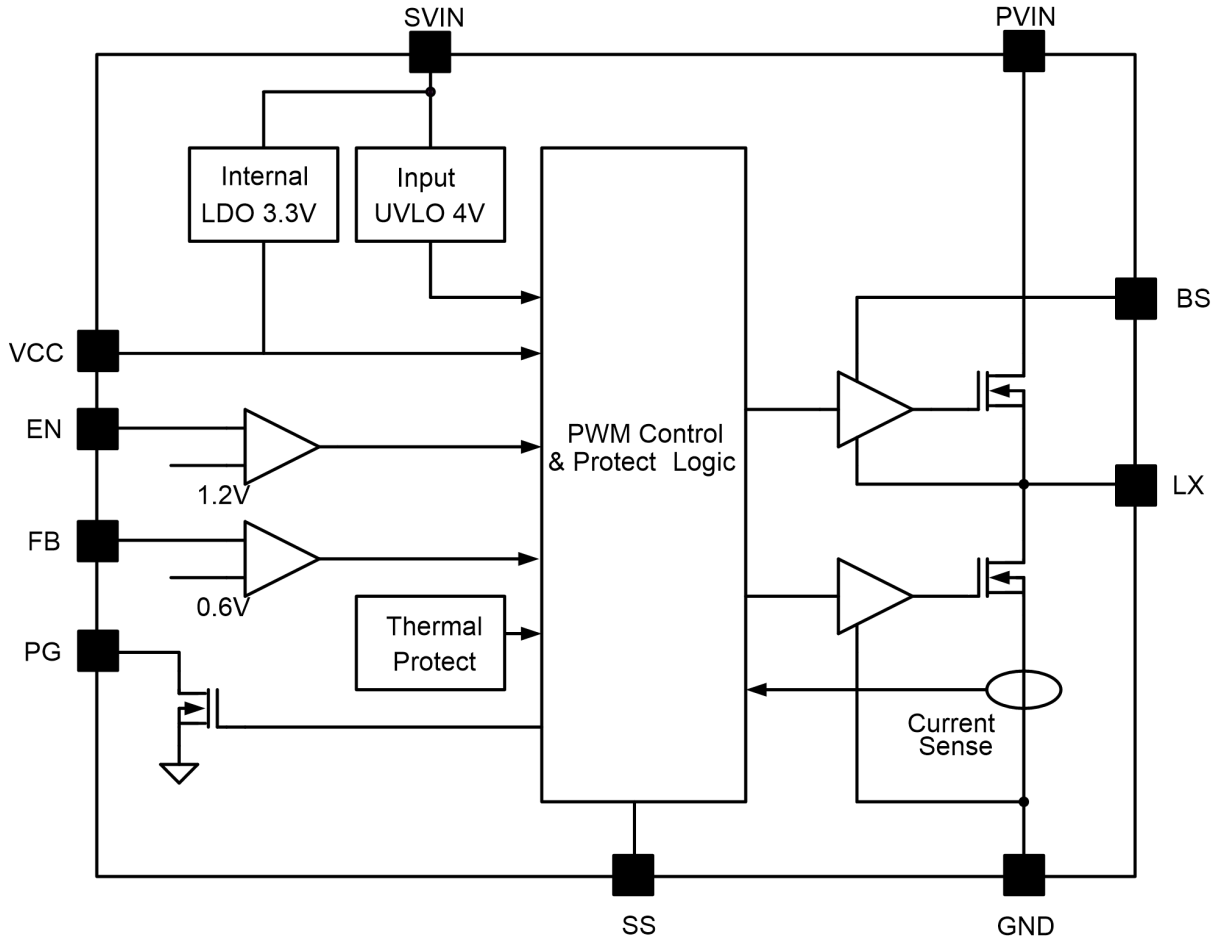


Figure5. Block Diagram

Absolute Maximum Ratings (Note 1)

PVIN, SVIN, LX, BS, EN, PG ---------- 33V
VCC, FB, SS, BS-LX ---------- 4V
Power Dissipation, P_D @ T_A = 25°C, DFN4×3-12/SO8E ---------- 2.8/3.3W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 36/30°C/W
θ_{JC} ---------- 18°/10°C/W
Junction Temperature Range ---------- 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C
Dynamic LX voltage in 10ns duration----------IN+3V to GND-4V

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 4.5V to 30V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{IN} = 12V, V_{OUT} = 5V, C_{OUT} = 47µF, T_A = 25°C, I_{OUT} = 1A unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		4.5		30	V
Quiescent Current	I_Q	I_{OUT}=0, V_{FB}=V_{REF}×105%		200		µA
Shutdown Current	I_{SHDN}	EN=0		5	10	µA
Feedback Reference Voltage	V_{REF}		0.591	0.6	0.609	V
FB Input Current	I_{FB}	V_{FB}=V_{CC}	-50		50	nA
Top FET RON	$R_{DS(ON)1}$			70		mΩ
Bottom FET RON	$R_{DS(ON)2}$			40		mΩ
Bottom FET Current Limit	I_{LIM}		5			A
EN Falling Threshold	V_{ENL}		1.1	1.2	1.3	V
EN Threshold Hysteresis	$V_{EN,HYS}$			0.1		V
Input UVLO Threshold	V_{UVLO}				4	V
UVLO Hysteresis	V_{HYS}			0.2		V
Oscillator Frequency	f_{OSC}	I_{OUT}=200mA		500		kHz
Min ON Time				80		ns
Min OFF Time				120		ns
Internal LDO Output	V_{VCC}	V_{IN}=4V	3.2	3.3	3.4	V
Thermal Shutdown Temperature	T_{SD}			160		°C
Thermal Shutdown Hysteresis	$T_{SD,HYS}$			20		°C

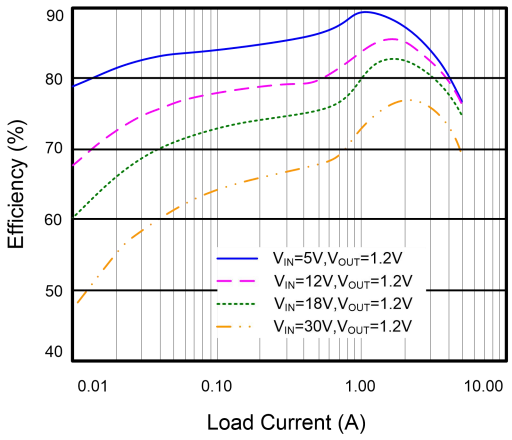
Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Paddle of DFN3x3-12/SO8E packages is the case position for θ_{JC} measurement.

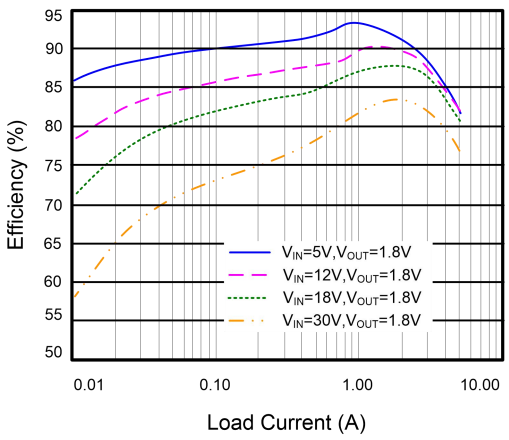
Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

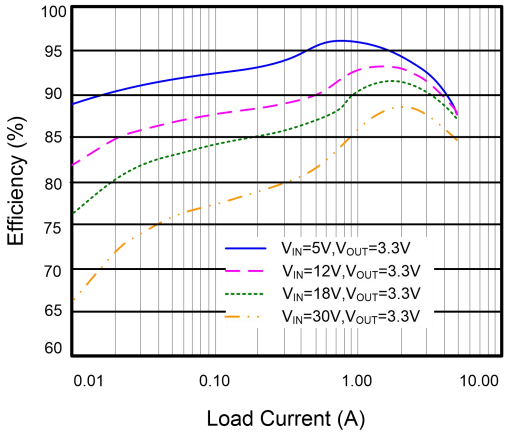
Efficiency vs. Load Current



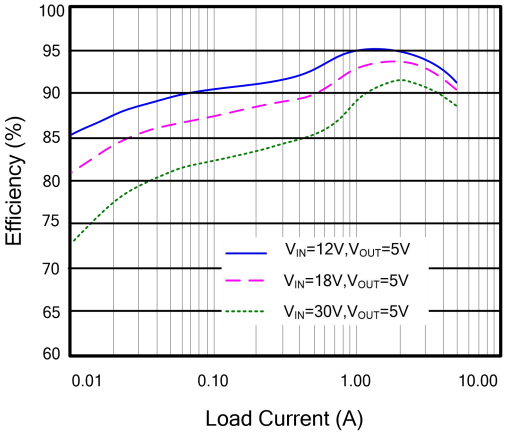
Efficiency vs. Load Current



Efficiency vs. Load Current

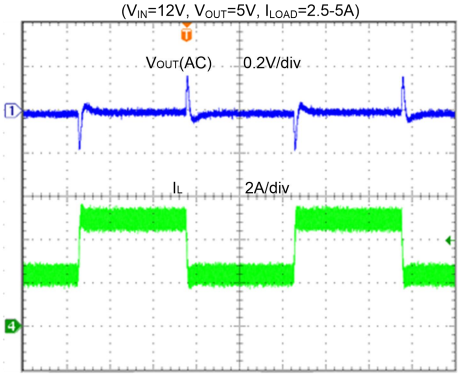


Efficiency vs. Load Current



Load Transient

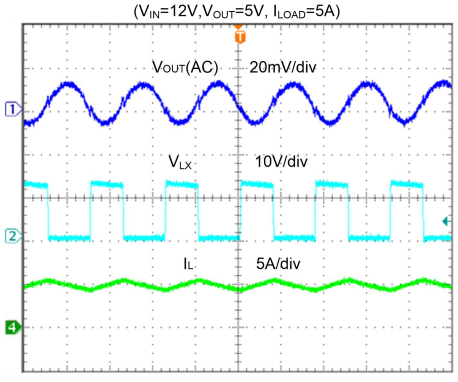
(VIN=12V, VOUT=5V, ILOAD=2.5-5A)



Time (200μs/div)

Output Ripple

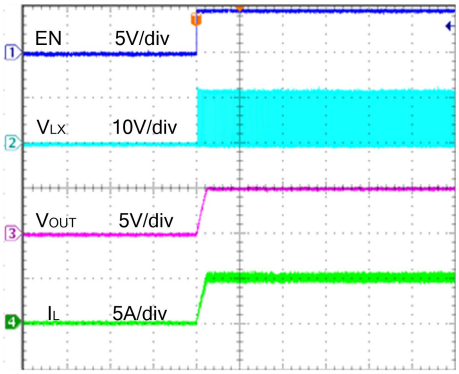
(VIN=12V,VOUT=5V, ILOAD=5A)



Time (1μs/div)

Startup

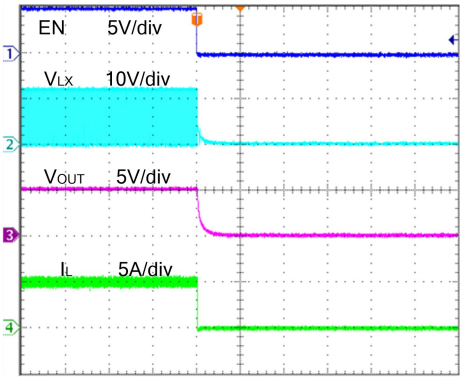
(EN=10Hz,V_{IN}=12V, V_{OUT}=5V, I_{LOAD}=5A)



Time (10ms/div)

Shutdown

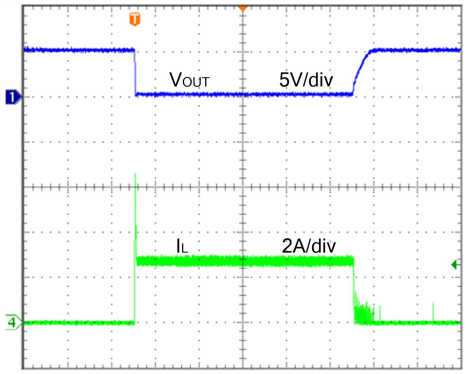
(EN=10Hz,V_{IN}=12V, V_{OUT}=5V, I_{LOAD}=5A)



Time (400μs/div)

Short Circuit Protection

(V_{IN}=12V, V_{OUT}=5V, Null load to Short)



Time (1ms/div)

Operation

The SY21211 is a synchronous buck regulator that integrates the PWM control and low $R_{DS(ON)}$ top and bottom MOSFETs on the same die to enable high-efficiency operation. This regulator can achieve high efficiency and high switching frequency simultaneously, to minimize the external inductor and capacitors sizes, resulting in a minimum solution footprint.

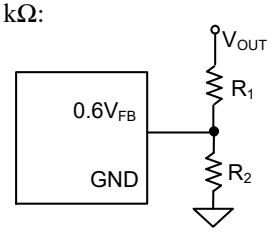
The SY21211 provides protection functions such as cycle by cycle current limit and thermal shutdown protection.
The EN pin accurate turn-on threshold enables increasing the UVLO threshold as required, based on the application requirements.

Applications Information

The following paragraphs provide information on the selection of the external components required, based on the application requirements.

Feedback Resistor Dividers R_1 and R_2:
Choose R_1 and R_2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_1 and R_2. A value of between 10kΩ and 1MΩ is highly recommended for both resistors. If V_{OUT} is 3.3V, R_1=100kΩ is chosen, then using the following equation, R_2 can be calculated to be 22.1kΩ:

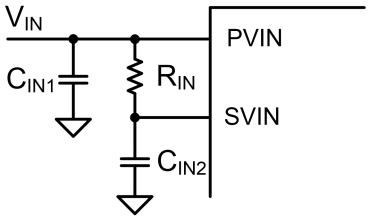
$$R_2 = \frac{0.6V}{V_{OUT} - 0.6V} R_1$$



Input Capacitor C_{IN}:
The ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D(1-D)}\ .$$

To minimize the potential noise problem, a typical X5R or better grade ceramic capacitor should be placed really close to the PVIN and the GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and the PVIN/GND pins. In this case, a 10µF low ESR ceramic capacitor is recommended.



The internal analog circuit is powered from the SVIN. To minimize noise, a 1µF ceramic capacitor connected between the SVIN and GND pins is recommended. A low-pass RC filter can also be added from the power input to the SVIN when large switching noise is present in the system.

Output Capacitor C_{OUT}:
The output capacitor is selected to handle the output ripple requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use an X5R or better grade ceramic capacitor greater than 47µF capacitance.

Output Inductor L:
There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{f_{SW} \times I_{OUT,MAX} \times 40\%}$$

Where fsw is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY21211 is tolerant of different ripple current amplitudes. Consequently, the final choice of inductance can be slightly different than the calculated value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1-V_{OUT}/V_{IN,MAX})}{2 \times f_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is

desirable to choose an inductor with DCR<10mΩ to achieve a good overall efficiency.

Soft-start

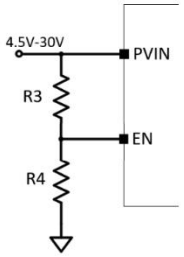
Connect a capacitor from the soft-start programming pin to ground to program the softstart time.

t_{SS}=Css×0.6V/10μA

Enable Operation

Pulling the EN pin low (<1.2V) disables the operation of the part, placing it in shutdown mode. During the shutdown mode, the SY21211 current drops to lower than 5μA. Driving the EN pin high (>1.3V) enables the soft-start circuit to ensure limiting of the inrush currents during startup.

For applications where the internally set UVLO threshold is too low, a resistor divider connected between VIN and GND with the center tap connected to the EN pin can be used to adjust the UVLO threshold as shown in the picture below:



Selecting a common resistor value for R4, for example 10KΩ, the second resistor R3 can be calculated using the following equation:

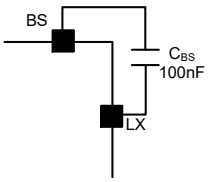
$$R3 = R4 \times \frac{V_{TH\_UVLO}-(V_{ENL}+V_{EN,HYS})}{V_{ENL}+V_{EN,HYS}}$$

where V_{TH_UVLO} is the new target UVLO threshold.

For the above example, for an UVLO target threshold of 8V, the calculated R4 value is: 103KΩ. Selecting the closest 1% tolerance value, R4 is chosen to be 102 KΩ.

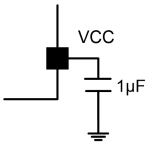
External Bootstrap Capacitor

This capacitor provides the gate driver voltage for internal high side MOSEFET. A 100nF low ESR ceramic capacitor connected between the BS pin and the LX pin is recommended.



VCC LDO

The internal 3.3V LDO provides the power supply for internal analog circuits and power MOSFETs. This pin should be bypassed to ground with a 1μF ceramic capacitor. The LDO can supply an external load for loads of 20mA, or less.



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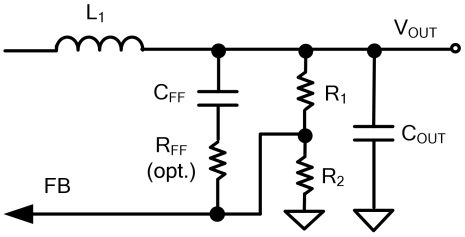
Power Good Indicator

PG is an open-drain output pin. The pin is pulled to ground if the output voltage is lower than 90% of the target voltage, and high-impedance otherwise.

Feed Forward Capacitor C_{FF}:

The SY21211 uses instant PWM architecture to achieve good stability and fast transient responses. In applications with high step load currents, adding an RC network, consisting of R_{FF} and C_{FF}, in parallel with R_1 may further speed up the load transient responses.



A 1kΩ R_{FF} is recommended .The selection of C_{FF} is related to the output capacitance present on the rail. Select the recommended C_{FF} value using the following table:

C_{OUT}(μF)	C_{FF}(nF)
47	0.1
100	0.68
220	1
330	3.3
470	6.8
680	10
1000	47

Schematic (SY21211DNC)

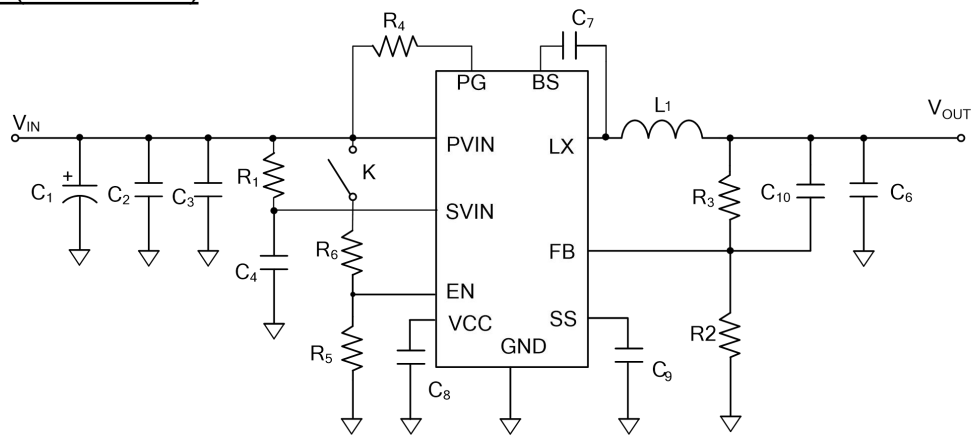


Figure1. Schematic Diagram

BOM List of (SY21211DNC)

Designator	Description	Part Number	Manufacturer
C1	47uF/50V Electrolytic Cap		
C2、C3	2.2uF/50V/X5R,1206	C3216X5R1H225K	TDK
C4	1uF/50V/X7R, 1206	C3216X7R1H105K	TDK
C6	47uF/6.3V/X5R,1206	C3216X5R0J476M	TDK
C7	0.1uF/50V/X7R, 0603	C1608X7R1H104K	TDK
C8	1uF/16V/X7R, 0603	C1608X7R1C105K	TDK
C9	47nF/50V/X7R,0603	C1608X7R1H473K	TDK
C10	47pF/50V/C0G,0603	C1608C0G1H470J	TDK
L1	2.2uH/12A	PCMB104T-2R2MS	CYNTEC
R1	2Ω , 1%, 0603		
R2	49.9k , 1%, 0603		
R3、R4	100k , 1%, 0603		
R5	1MΩ , 1%, 0603		
R6	10k, 1%, 0603		

Schematic (SY21211FCC)

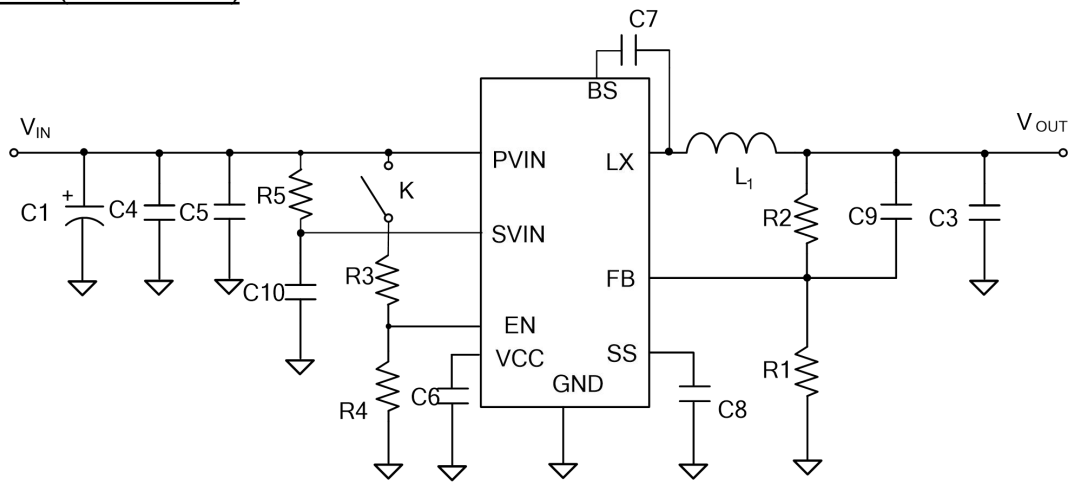


Figure1. Schematic Diagram

BOM List of SY21211FCC

Designator	Description	Part Number	Manufacturer
C1	47uF/50V Electrolytic Cap		
C3	47uF/6.3V/X5R,1206	C3216X5R0J476M	TDK
C4 、C5	2.2uF/50V/X5R,1206	C3216X5R1H225K	TDK
C6	1uF/16V/X7R, 0603	C1608X7R1H105K	TDK
C7、C10	0.1uF/50V/X7R, 0603	C1608X7R1H104K	TDK
C8	47nF/50V/X7R,0603	C1608X7R1H473K	TDK
C9	47pF/50V/COG,0603	C1608C0G1H470J	TDK
L1	2.2uH/12A	PCMB104T-2R2MS	CYNTEC
R1	49.9k , 1%, 0603		
R2	100k , 1%, 0603		
R3	10k , 1%, 0603		
R4	1MΩ, 1%, 0603		
R5	2Ω, 1%, 0603		

Layout Design:

Place the following components close to the device: C_{IN}, C_{VCC} L, R_1 and R_2.

1) It is desirable to maximize the PCB copper area connecting to the GND pin to achieve the best thermal and noise performance. If the board space allows, a large copper pour connected to ground is recommended.

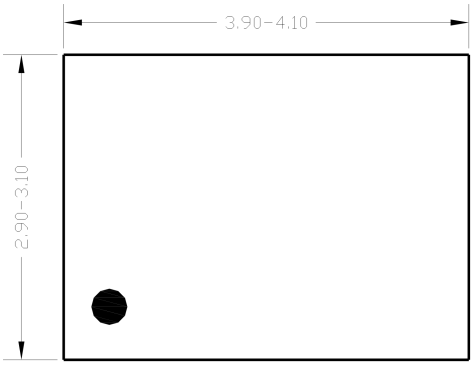
2) C_{IN} must be close to IN and the GND pins. The loop area formed by C_{IN} and GND must be minimized.

3) The PCB copper area associated with the LX pin must be minimized to minimize radiated emissions (EMI).

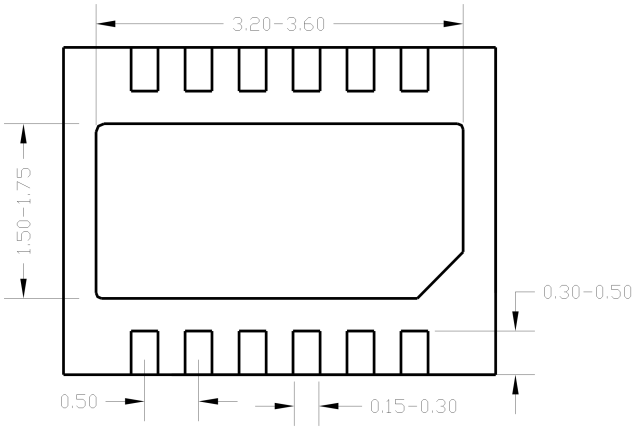
4) The components R_1 and R_2 and the trace connecting to the FB pin must NOT be adjacent to the LX net on the PCB layout to avoid crosstalk.

5) If the system chip interfacing with the EN pin has a high impedance state during shutdown, and the IN pin is connected directly to a power source such as a Li-Ion battery, add a pull-down 1MΩ resistor between the EN and the GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

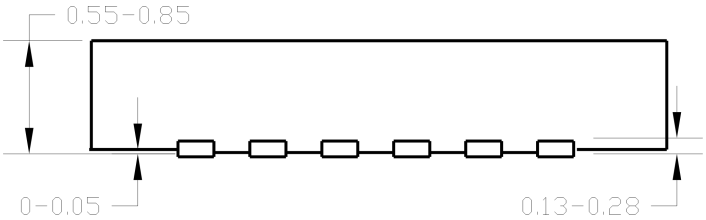
DFN4×3-12 Package Outline & PCB Layout



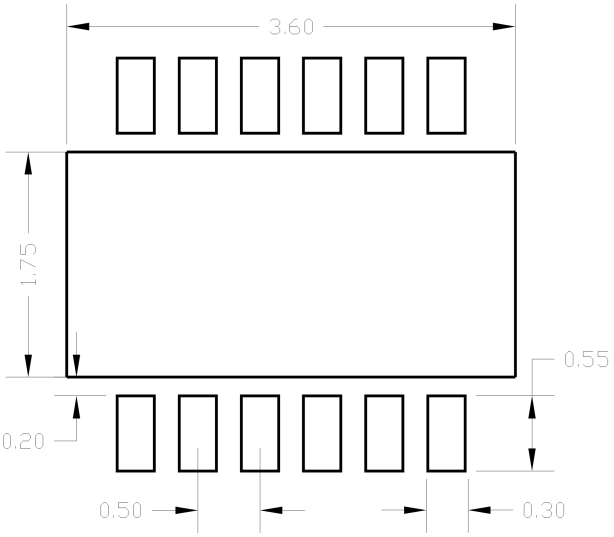
Top View



Bottom View



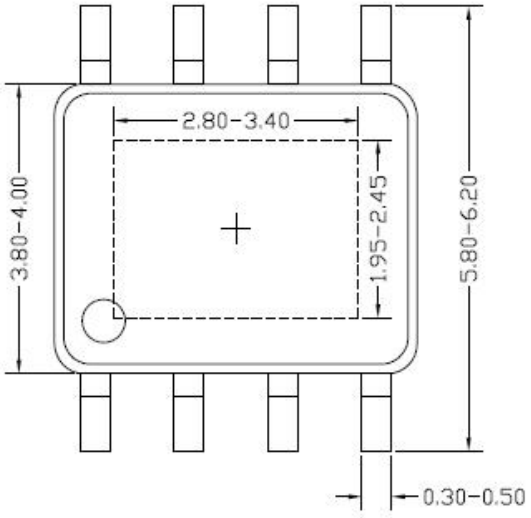
Side View



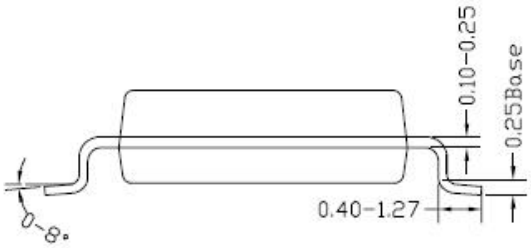
PCB layout (Recommended)

Notes: **All dimension in millimeter and exclude mold flash & metal burr**

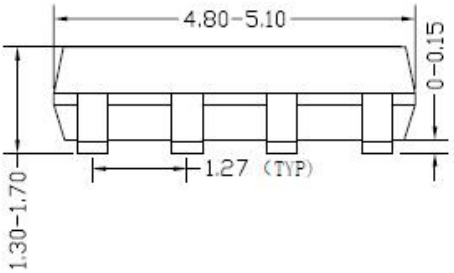
SO8E Package Outline & PCB Layout



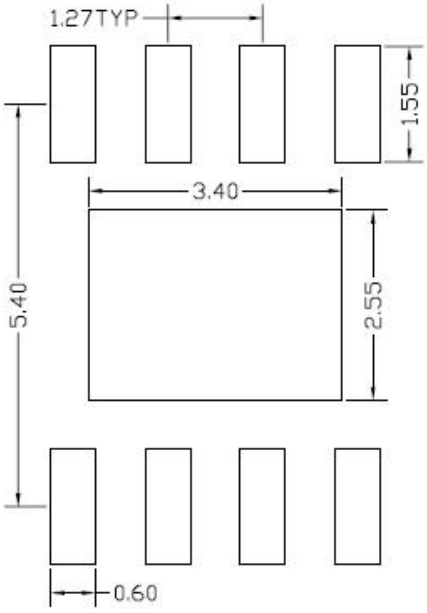
Top view



Side view



Front view



Recommended PCB layout
(Reference Only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

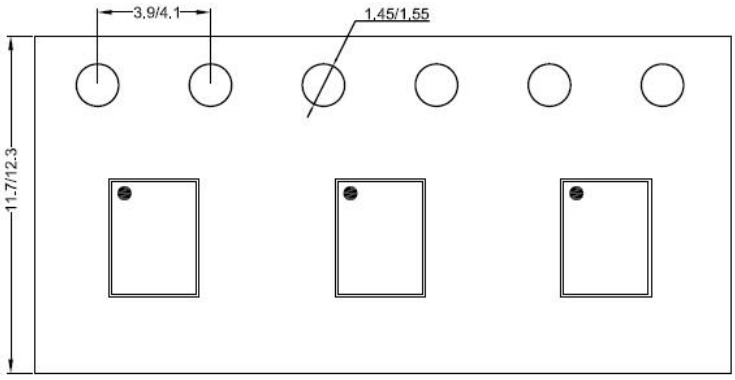
Taping & Reel Specification

1. Taping orientation

SOP8-E

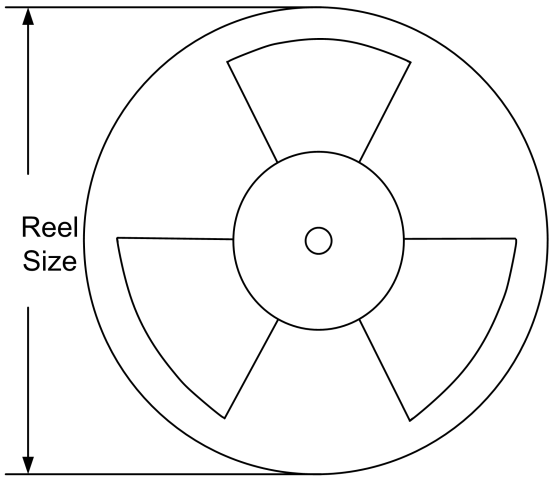
Feeding direction ⟶

DFN4x3 (DFN4030)



Feeding direction ⟶

2.Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SOP8E	12	8	13"	400	400	2500
DFN4x3	12	8	13"	400	400	5000

3. Others: NA

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