

General Description

The SY21264A high efficiency step-up regulator operates using current mode control, and can deliver 4A current over a wide input voltage range from 2V to 6V. It integrates an N-channel MOSFET with low 90mΩ $R_{DS(ON)}$ to minimize conduction loss.

The 1MHz switching frequency and internal compensation reduce external inductor and capacitor sizes, and the built-in internal soft-start circuitry minimizes inrush current at startup.

The SY21264A is available in a compact DFN3mmx3mm-10 package.

Features

- 2V to 6V Input Voltage Range
- Up to 6V Output Voltage
- Low $R_{DS(ON)}$ for Internal N-Channel MOSFET: 90mΩ Typical
- 1MHz Switching Frequency
- Minimum On-Time: 100ns Typical
- Minimum Off-Time: 100ns Typical
- Internal 4A Switch
- Internal Soft-Start Limits Inrush Current
- $\pm 2\%$ 0.6V Reference
- Overtemperature Protection
- Overcurrent Protection
- RoHS-Compliant and Halogen-Free
- Compact DFN3mmx3mm-10 Package

Applications

- Single-Cell Li-ion Battery-Powered Applications
- Portable Devices

Typical Application

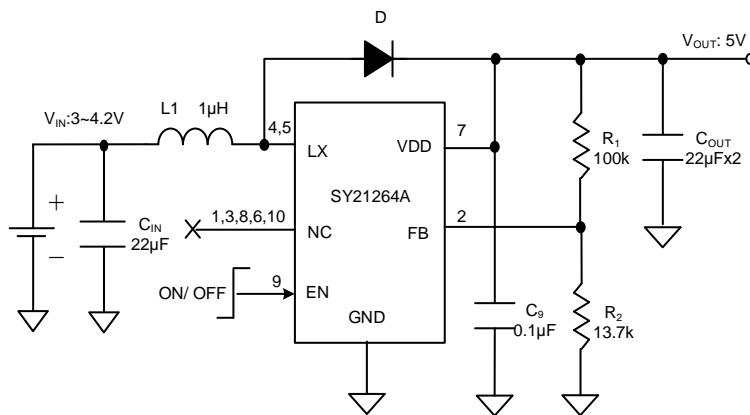


Figure 1. Typical Application Circuit

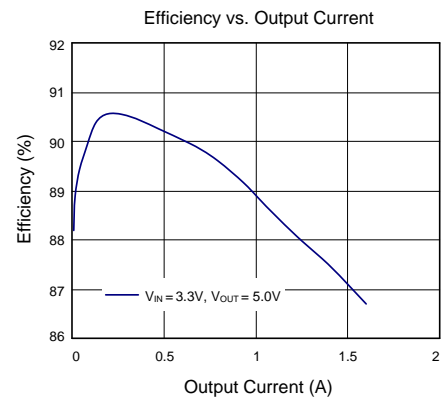


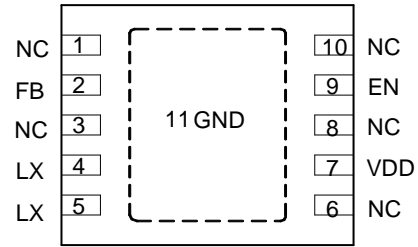
Figure 2. Efficiency vs. Output Current



Ordering Information

Ordering Part Number	Package Type	Top Mark
SY21264ADBC	DFN3x3-10 RoHS-Compliant and Halogen-Free	UCxyz

Pinout (top view)



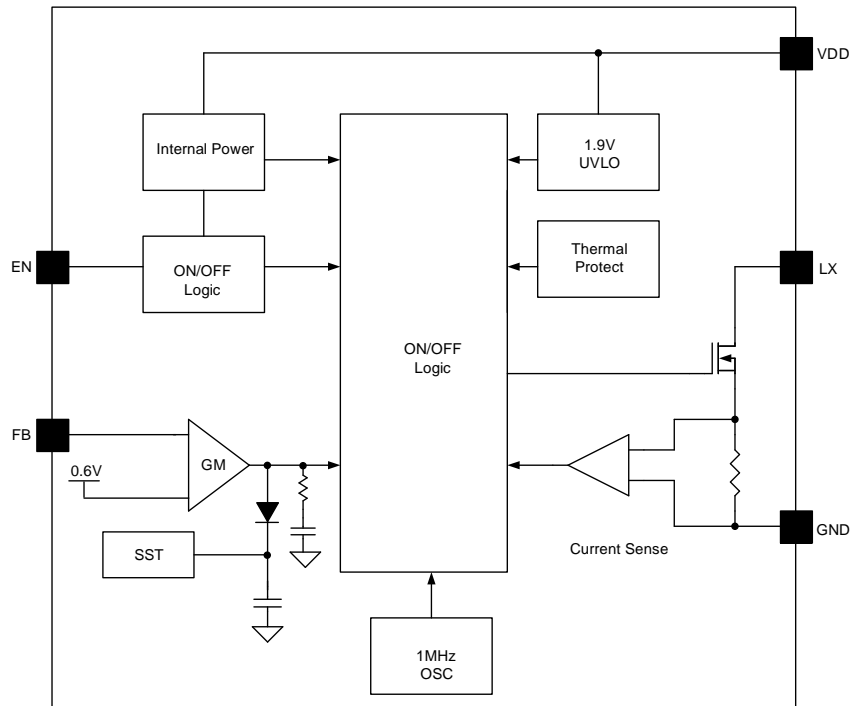
Device code: UC

x = year code, y = week code, z = lot number code

Pin Description

Pin Name	Pin Number	Pin Description
1,3,6,8,10	NC	No connection.
2	FB	Feedback pin. Connect a resistor R_1 between V_{OUT} and FB, and a resistor R_2 between FB and GND to program the output voltage: $V_{OUT} = 0.6V \times (R_1/R_2+1)$.
4,5	LX	Inductor node. Connect an inductor between the IN and LX pins.
7	VDD	Input pin. Decouple this pin to the GND pin with a $1\mu F$ ceramic capacitor.
9	EN	Enable pin. Pull low to disable the device, pull high to enable. Do not leave this pin floating.
11	GND	IC power supply input pin.

Block Diagram



Absolute Maximum Ratings

Parameter (Note1)	Min	Max	Unit
FB	-0.3	4	V
LX, EN, VDD	-0.3	7	
LX, 50ns Duration		VIN + 3	
Lead Temperature (Soldering, 10s)		260	°C
Junction Temperature, Operating	-40	150	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	38	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	8	
P_D Power Dissipation $T_A = 25^\circ\text{C}$	2.6	W

Recommended Operating Conditions

Parameter (Note3)	Min	Max	Unit
FB	-0.3	3.6	V
VDD	2	6	
LX, EN	0	6	
Junction Temperature, Operating	-40	125	°C
Ambient Temperature	-40	85	

Electrical Characteristics

($V_{IN} = 3V$, $V_{OUT} = 5V$, $I_{OUT} = 1A$, $T_A = 25^{\circ}C$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2		6	V
Quiescent Current	I_Q	$V_{FB} = 0.66V$		100		μA
Shutdown Current	I_{SHDN}	$EN = 0$			10	μA
Low Side Main FET R_{ON}	$R_{DS(ON)}$			90		m Ω
Main FET Current Limit	I_{LIM}		4			A
Switching Frequency	f_{SW}			1		MHz
Feedback Reference Voltage	V_{REF}		0.588	0.6	0.612	V
VDD UVLO Rising Threshold	V_{IN_UVLO}				1.9	V
UVLO Hysteresis	V_{UVLO_HYS}			0.1		V
Thermal Shutdown Temperature	T_{SD}			150		$^{\circ}C$
EN Rising Threshold	V_{ENH}		1.5			V
EN Falling Threshold	V_{ENL}				0.4	V
EN Pin Input Current	I_{EN}		0		100	nA

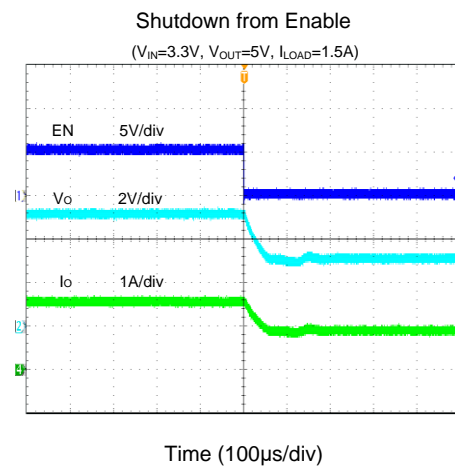
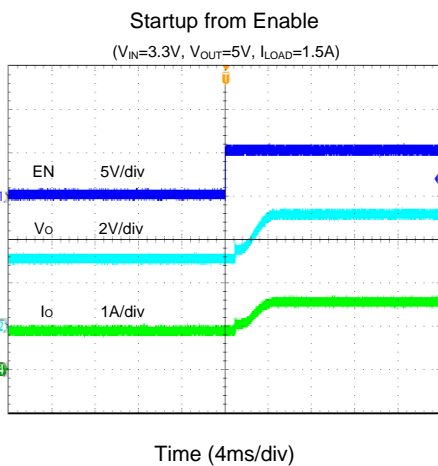
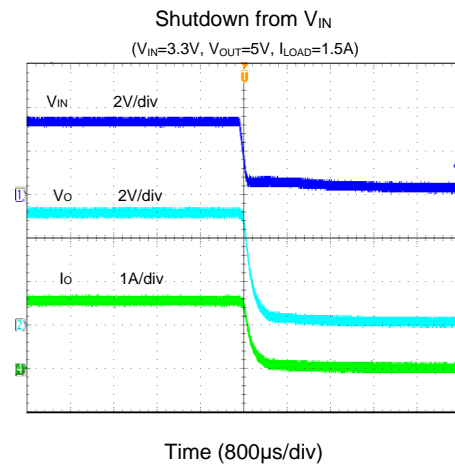
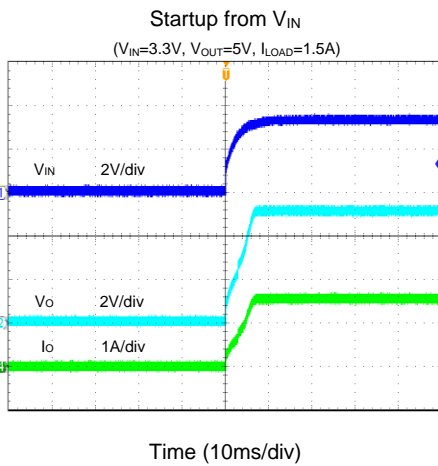
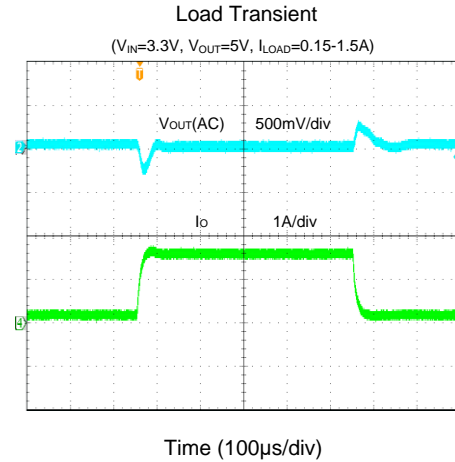
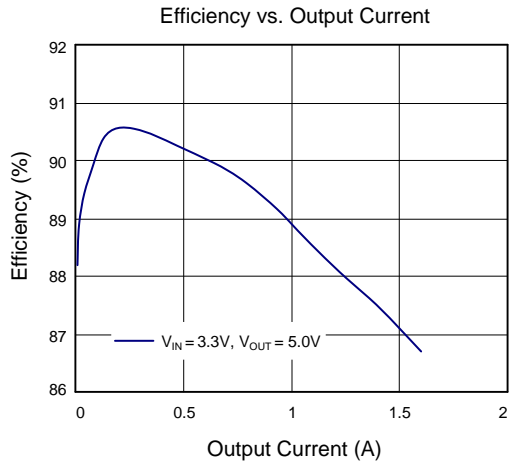
Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

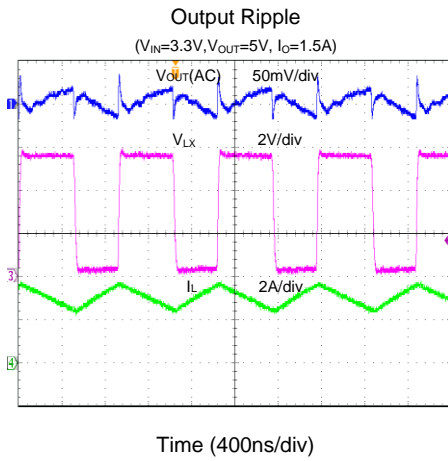
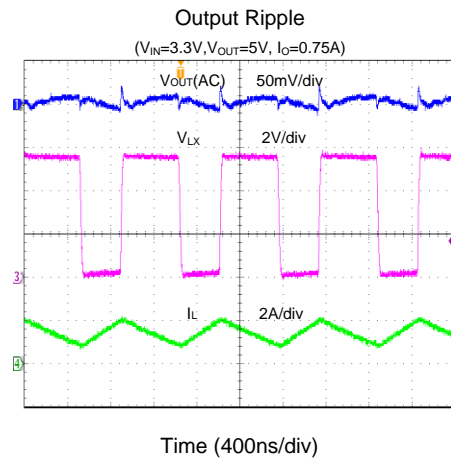
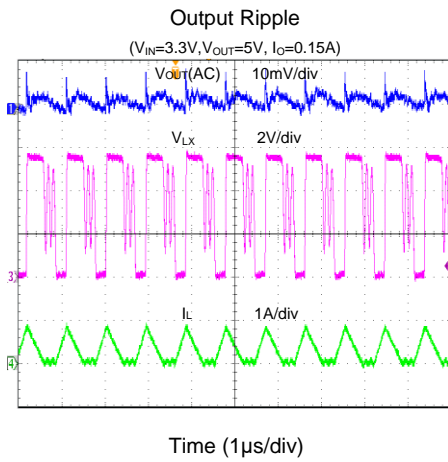
Note 2: θ_{JA} is measured in the natural convection at $T_A = 25^{\circ}C$ on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2” x 2” FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

Note 3: The device is not guaranteed to function outside its operating conditions,

Typical Performance Characteristics

($T_A = 25^\circ\text{C}$, $V_{IN} = 3.3\text{V}$, $V_{OUT} = 5\text{V}$, $L = 1\mu\text{H}$, $C_{OUT} = 44\mu\text{F}$, unless otherwise specified.)





Detailed Description

The SY21264A high efficiency step-up regulator operates using current mode control, and can deliver 4A current over a wide input voltage range from 2V to 6V. It integrates an N-channel MOSFET with low 90mΩ $R_{DS(ON)}$ to minimize conduction loss.

The 1MHz switching frequency and internal compensation reduce external inductor and capacitor sizes, and the built-in internal soft-start circuitry minimizes inrush current at startup.

The SY21264A is available in a compact DFN3mmx3mm-10 package.

Enable Operation

Driving the EN pin high (>1.5V) enables normal operation. Driving the EN pin low (<0.4V) will shut down the device. During shutdown mode, the SY21264A shutdown current drops to less than 10μA.

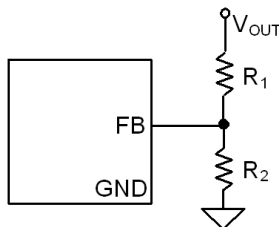
Application Information

The following paragraphs describe the selection process for the feedback resistors (R1 and R2), input capacitor C_{IN} , output capacitor C_{OUT} , boost inductor L, and diode D.

Feedback Resistor Divider R1 and R2

Choose R1 and R2 to program the proper output voltage. Choose large resistance values between 10kΩ and 1MΩ for both R1 and R2 to minimize power consumption under light loads. If a value is chosen for R1, then R2 can be calculated as:

$$R2 = \frac{0.6V}{V_{OUT}-0.6V} R1$$



Input Capacitor C_{IN}

Input filter capacitors reduce the ripple voltage on the input, filter the switched current drawn from the input supply, and helps with reducing EMI. When selecting an input capacitor, be sure to select a voltage rating at least 20% greater than the maximum voltage of the input supply and a temperature rating higher than the system requirements. X5R series

ceramic capacitors are most often selected due to their small size, low cost, surge-current capability, and high RMS current ratings over a wide temperature and voltage range. However, systems that are powered by a wall adapter or other long and therefore inductive cabling may be susceptible to significant inductive ringing at the input to the device. In these cases, consider adding some bulk capacitance like electrolytic, tantalum, or polymer type capacitors. Using a combination of bulk capacitors (to reduce overshoot or ringing) in parallel with ceramic capacitors (to meet the RMS current requirements) is helpful in these cases.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

$$I_{CIN_RMS} = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{\sqrt{3} \times L \times f_{SW} \times V_{OUT}}$$

For the best performance, select a typical X5R or better grade low ESR ceramic capacitor of at least 22μF, and place it as close as possible to the VDD and GND pins. Minimize the loop area formed by C_{IN} and the VDD/GND pins.

Output Capacitor C_{OUT}

Select the output capacitor C_{OUT} to handle the output ripple requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting the component. For the best performance, use two X5R or better grade ceramic capacitors with 10V rating and capacitance of at least 22μF each.

For applications where the design must meet stringent ripple requirements, the following considerations must be followed:

The output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔI_L) on the output capacitor's ESR (ESR ripple), as well as the stored charge (capacitive ripple). When calculating total ripple, both should be considered.

$$V_{RIPPLE, ESR1} = I_{LPEAK} \times ESR$$

$$V_{RIPPLE, ESR2} = I_{LVALLEY} \times ESR$$

$$V_{RIPPLE,CAP} = \frac{I_{OUT} \times (1-D)}{C_{OUT} \times f_{SW}}$$

The capacitive ripple might be higher because the effective capacitance for ceramic capacitors decreases with the voltage across the terminals. The voltage derating is usually included as a chart in the capacitor datasheet, and the ripple can be recalculated after taking the target output voltage into account.

Boost Inductor L

Consider the following when choosing this inductor:

- 1) Choose the inductance to provide a ripple current that is approximately 40% of the maximum output current. The recommended inductance is calculated as:

$$L = \left(\frac{V_{IN}}{V_{OUT}} \right)^2 \frac{V_{OUT} - V_{IN}}{f_{SW} I_{OUT,MAX} \times 0.4}$$

where f_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY21264A has high tolerance for ripple current amplitude variation. As a result, the final choice of inductance can vary slightly from the calculated value with no significant performance impact.

- 2) The inductor's saturation current rating must be greater than the peak inductor current under full load:

$$I_{SAT,MIN} = \left(\frac{V_{OUT}}{V_{IN}} \right) \times I_{OUT,MAX} + \frac{V_{IN}(V_{OUT} - V_{IN})}{2 \times f_{SW} \times L \times V_{OUT}}$$

- 3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. Choose an inductor with DCR less than 10mΩ to achieve good overall efficiency.

Rectifier Diode

For high efficiency, choose a Schottky diode with low forward voltage drop and fast reverse recovery. The maximum current rating of the diode must be higher than the maximum input current, and the average current rating of the diode must be higher than the output current.

Applications with Large Bulk Capacitance

In applications with large bulk capacitance present on the output, a very high inrush current could flow through the inductor during power-on. In order to limit the current flowing into the device and prevent damage, a Zener diode connected from the power input to the output or an RC delay circuit added on the EN pin are recommended, as shown in Figure 3.

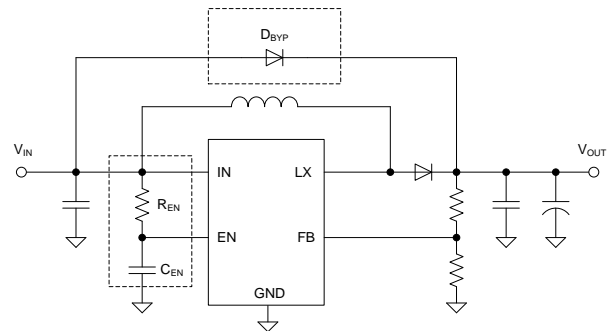
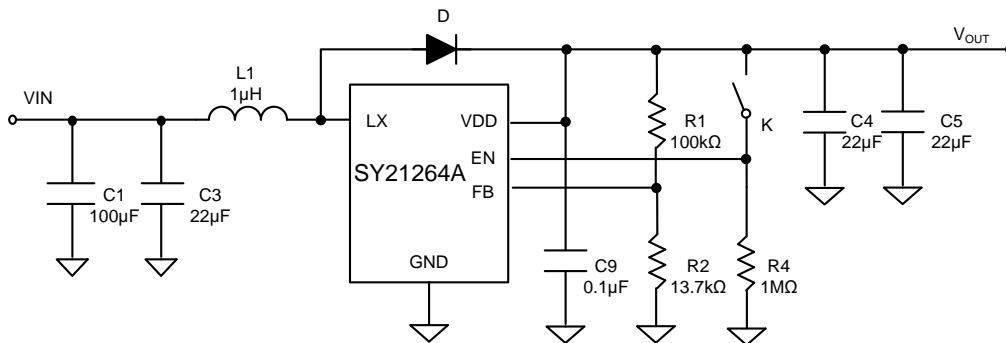


Figure 3. Application Circuit with Large Bulk Capacitance

Application Schematic



Design Specifications

Input Voltage (V)	Output Voltage(V)	Output Current Limit (A)
3-4.2	5	1.5

BOM List

Reference Designator	Description	Part Number	Manufacturer
U1	4A, 1MHz Sync Boost (DFN3x3-10)	SY21264ADBC	Silergy
L1	1µH/7A inductor	SPM6530T-1R0M120	TDK
C1	100µF/16V (electrolytic capacitor)		
C3, C4, C5	22µF/10V,1206,X5R	C3216X5R1A226M	TDK
C9	0.1µF/25V, 0603, X5R	GRM188R61E104K	muRata
D1	5A Schottky diode	SS54	
R1	100k,1%,0603		
R2	13.7k,1%,0603		
R4	1MΩ, 0603		

Recommend Components for Typical Applications

V _{OUT} (V)	R1(kΩ)	R2(kΩ)	L(µH)	C3
5	100	13.7	1	2×22µF/10V/X5R,1206

Layout Design

To achieve optimal design, follow these PCB layout considerations:

- Place C_{IN} , L, R1, and R2 close to the converter.
- To achieve the best thermal and noise performance, maximize the PCB copper area connecting to the GND pin. A ground plane is highly recommended if board space allows.
- C_{IN} must be close to pins VDD and GND. Minimize the loop area formed by C_{OUT} , LX, and GND.

- To reduce switching noise, minimize the PCB copper area connected to the LX pin.
- In order to reduce crosstalk, R1, R2, and the trace connected to the FB pin must not be adjacent to the LX net on the PCB layout.
- If the system chip interfacing with the EN pin has a high impedance state during shutdown mode, and the VDD pin is connected directly to a power source such as a Li-ion battery, add a 1M Ω pull-down resistor between the EN and GND pins to prevent noise from falsely triggering the regulator during shutdown mode.

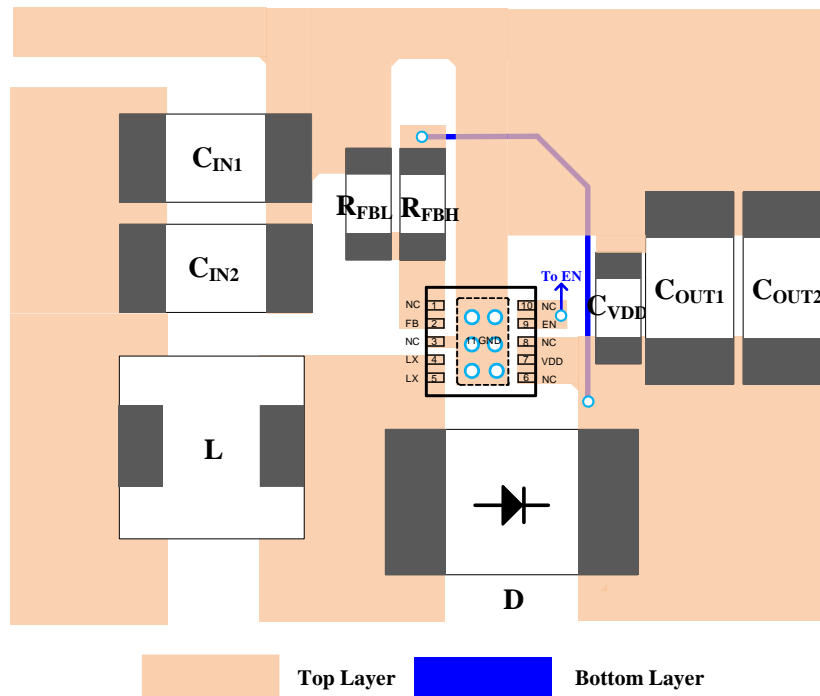
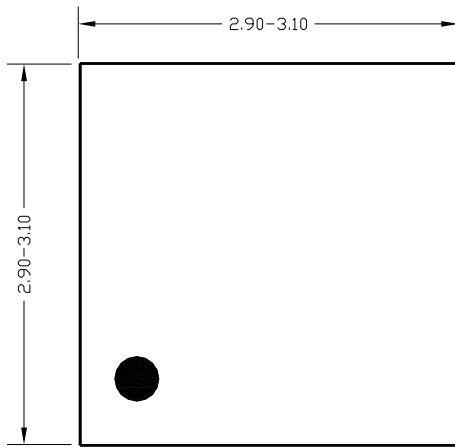
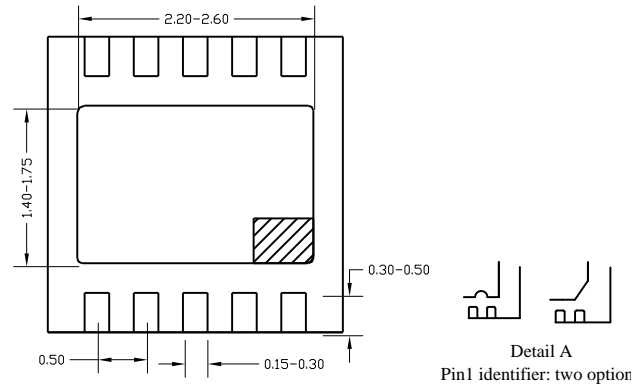


Figure 4. Suggested PCB Layout

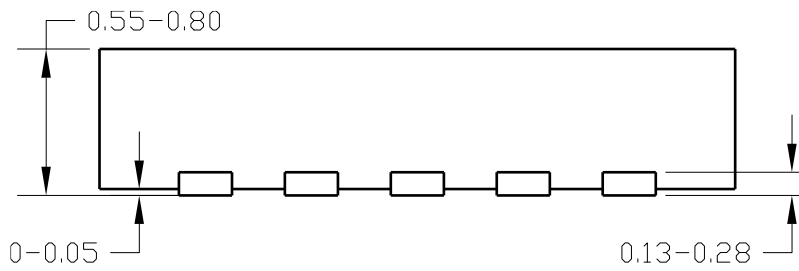
DFN3x3-10 Package Outline and PCB Layout



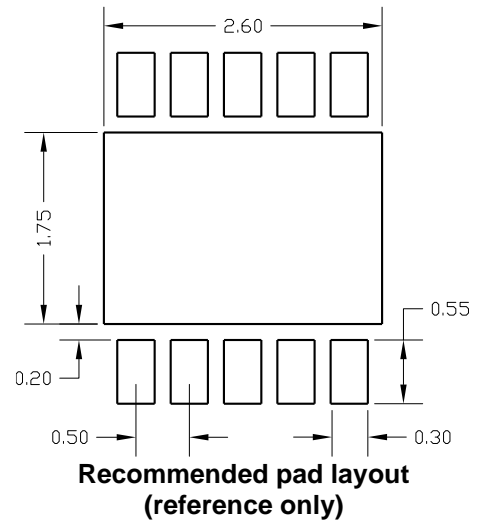
Top view



Bottom view



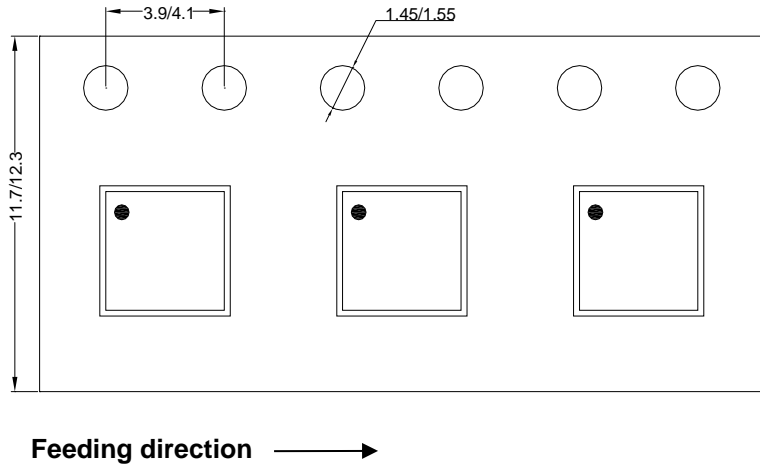
Side view



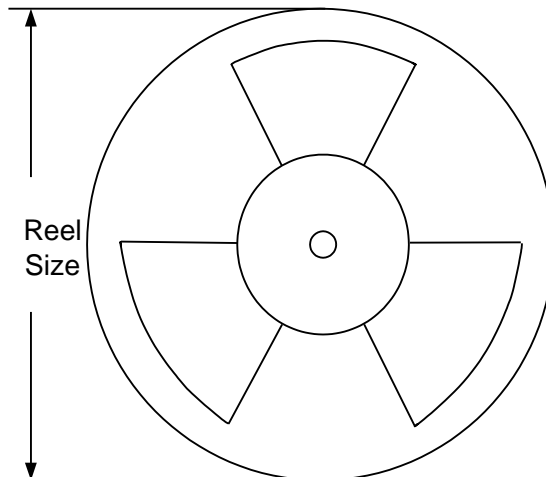
Note: All dimensions are in millimeters and exclude mold flash and metal burr.

Taping and Reel Specification

DFN3x3-10 taping orientation



Carrier tape and reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN3x3	10	8	13"	400	400	5000

Others: NA

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Apr.20, 2023	Revision 1.0	Language improvements for clarity.
Feb.22, 2019	Revision 0.9A	Modify the formula in "Output Inductor L" (page 6) From $I_{SAT, MIN} > \left(\frac{V_{OUT}}{V_{IN}} \right) \times I_{OUT, MAX} + \left(\frac{V_{IN}}{V_{OUT}} \right)^2 \frac{(V_{OUT} - V_{IN})}{2 \times F_{SW} \times L}$ To $I_{SAT, MIN} > \left(\frac{V_{OUT}}{V_{IN}} \right) \times I_{OUT, MAX} + \frac{V_{IN} \cdot (V_{OUT} - V_{IN})}{V_{OUT} \cdot 2 \times F_{SW} \times L}$
May 03, 2013	Revision 0.9	Initial Release

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