SY21282

High Efficiency 1MHz, 16V, 6A Synchronous Step-Up Regulator with Accurate Output Current Limit

General Description

The SY21282 high efficiency synchronous step-up regulator operates using adaptive constant off-time and current mode control, and supports a wide input voltage range from 3V to 9V. It integrates switches with low $R_{DS(ON)}$ to minimize conduction loss.

The SY21282 features cycle-by-cycle peak current limit, output short-circuit protection, and true shutdown. It also provides enable control and power-good indicator for system power sequencing. The 1MHz pseudo-constant frequency reduces the output voltage ripple and permits smaller external capacitors and inductor.

The SY21282 is available in a compact QFN3×3-16 package.

Features

- 3V to 9V Input Voltage Range
- 6A (Min.) Main MOSFET Current Limit
- 7 µA Shutdown Current (Max.)
- 600 µA Quiescent Current (Typ.)
- Programmable Output Current Limit
- Low $R_{DS(ON)}$ for Internal N-Channel MOSFET: 80mΩ Main, 40mΩ Rectifier, 40mΩ Disconnection
- Synchronous Rectification for High Efficiency
- Pseudoconstant 1MHz Frequency
- Enable Control
- Input Voltage UVLO
- Output Overvoltage Protection
- Overtemperature Protection
- Output Short-Circuit Protection
- Power-Good Indicator
- True Shutdown Function
- RoHS-Compliant and Halogen-Free
- Compact QFN3mm×3mm-16 Package

Applications

- Power Bank
- High Power Application
- SSD

Typical Application

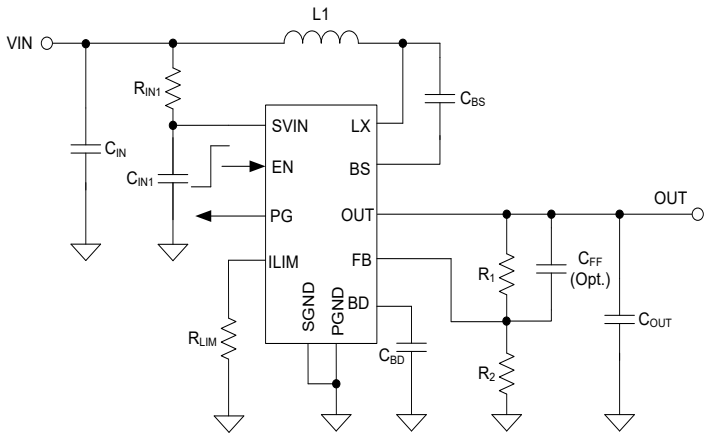


Figure 1. Typical Application Circuit

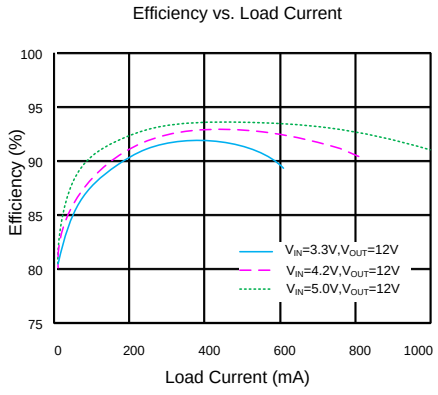


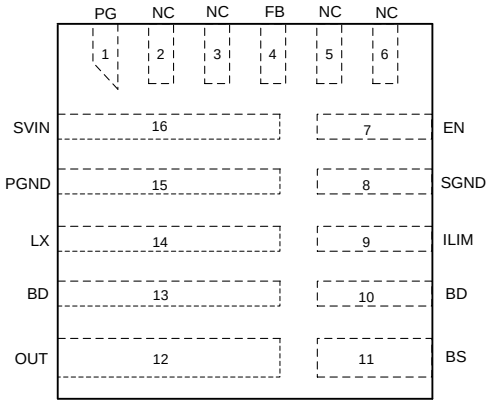
Figure 2. Efficiency vs. Output Current

Ordering Information

Ordering Part Number	Package type	Top Mark
SY21282QDC	QFN3×3-16 RoHS-Compliant and Halogen-Free	**XJ*xyz***

x = year code, y = week code, z = lot number code

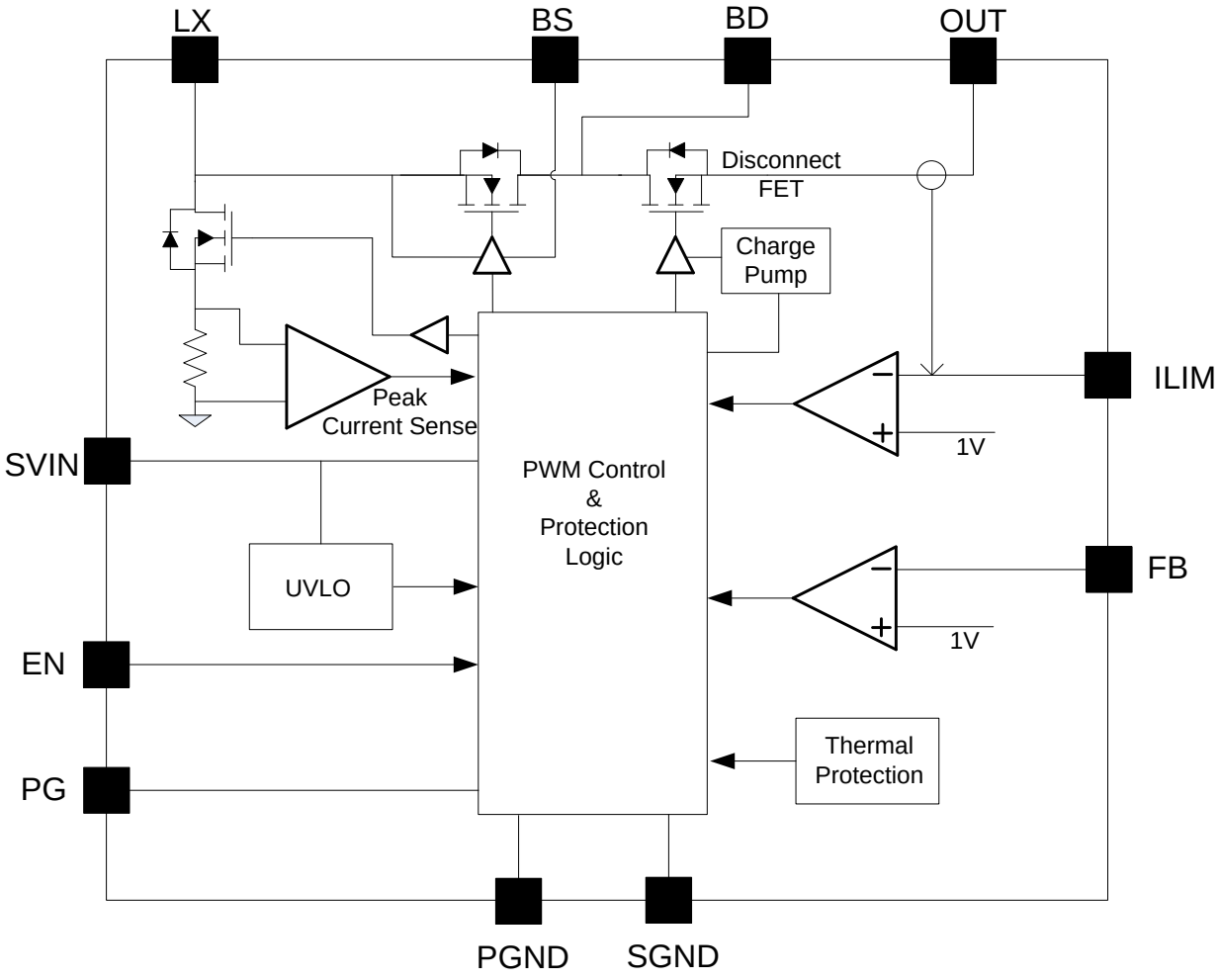
Pinout (top view)



Pin Description

Pin Number	Pin Name	Pin Description
1	PG	Power-good indicator. Open-drain output, pulled low when the output is less than 90% of regulation voltage or OVP is triggered; high impendence otherwise.
2, 3, 5,6	NC	Not connected.
4	FB	Feedback pin. Connect to the center of the resistor voltage divider to program the output voltage: V_{OUT} = 1V ×(R1/R2 + 1)
7	EN	Enable pin. Pull low to disable the device, pull high to enable. Do not leave this pin floating.
8	SGND	Signal ground pin. Connect to system GND.
9	I_{LIM}	Output current limit program pin. Connect a resistor R_{LIM} from this pin to the SGND pin to program the output current limit threshold: I_{LIM}(A) =10(V)/ R_{LIM}(kΩ)
10,13	BD	Output of the boost regulator, and the input of the disconnection FET. Connect an MLCC from this pin to the PGND pin with at least a 10μF capacitor.
11	BS	Bootstrap pin. Power supply for the rectifier gate driver. Connect a 0.1μF ceramic capacitor between BS and the LX pins.
12	OUT	Output of the load disconnect FET.
14	LX	Inductor node. Connect an inductor from the power input to the LX pin.
15	PGND	Power ground pin. Connect to system GND.
16	SVIN	IC power supply input pin. Decouple this pin to the SGND pin with a 1μF ceramic capacitor.

Block Diagram



Absolute Maximum Ratings

Parameter (Note1)	Min	Max	Unit
SVIN, EN, OUT, BD, LX	-0.3	16	V
BS-LX		3.6	
PG, FB, ILIM, BS	-0.3	3.6	
Lead Temperature (Soldering, 10 sec.)		260	°C
Junction Temperature, Operating	-40	150	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	50	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	4	
P_D Power Dissipation T_A= 25°C	2.6	W

Recommended Operating Conditions

Parameter (Note3)	Min	Max	Unit
SVIN	3	9	V
FB	0	3.3	
Junction Temperature, Operating	-40	150	°C
Ambient Temperature	-40	85	

Electrical Characteristics

(V_{IN} =5V, V_{OUT}=12V, I_{OUT}=100mA, T_A= 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{SVIN}		3		9	V
Maximum Output Voltage	V_{OUT}				13	V
Quiescent Current	I_Q	FB = 2V		600		μA
Shutdown Current	I_S	V_{IN} = 9V, EN = 0			7	μA
Main FET R_{ON}	$R_{DS(ON)\_M}$			80		mΩ
Rectifier FET R_{ON}	$R_{DS(ON)\_R}$			40		mΩ
Disconnection FET R_{ON}	$R_{DS(ON)\_D}$			40		mΩ
Main FET Current Limit	I_{LIM}		6			A
Switching Frequency	f_{SW}			1		MHz
Feedback Reference Voltage	V_{REF}		0.98	1	1.02	V
Output OVP Threshold	$V_{OVP,\ FB}$	V_{FB} rising		120%		V_{REF}
	$V_{OVP,\ OUT}$	V_{OUT} rising			16	V
Output Short-Circuit Protection Threshold	$V_{OUT,SCP}$	V_{OUT} falling		2		V
Output Current Limit	I_{LIM}	R_{LIM} = 10kΩ	0.85	1	1.15	A
SVIN UVLO Rising Threshold	$V_{SVIN,UVLO}$				2.9	V
SVIN UVLO Hysteresis	$V_{SVIN,HYS}$			0.1		V
Minimum On-Time	t_{ON_MIN}			100		ns
Minimum Off-Time	t_{OFF_MIN}			100		ns
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Recovery Hysteresis	T_{HYS}			15		°C

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

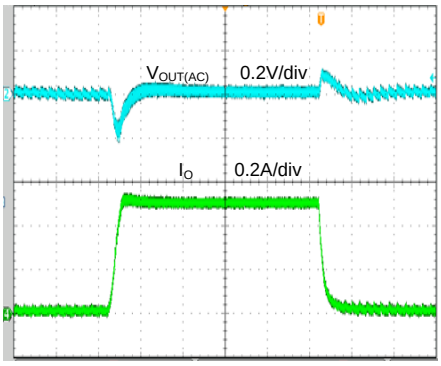
Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

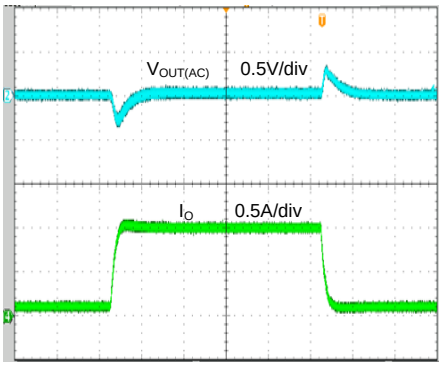
(T_A= 25℃, V_{IN}=5V, V_{OUT} = 12V, L = 2.2uH, C_{OUT}= 44uF, unless otherwise specified.)

Load Transient
V_{IN}=5V,V_{OUT}=12V,I_{OUT}=0A-500mA



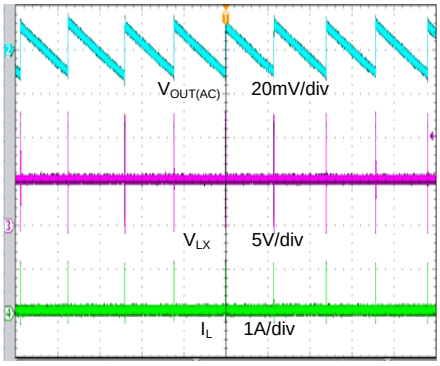
Time (100μs/div)

Load Transient
V_{IN}=5V,V_{OUT}=12V,I_{OUT}=100mA~1A



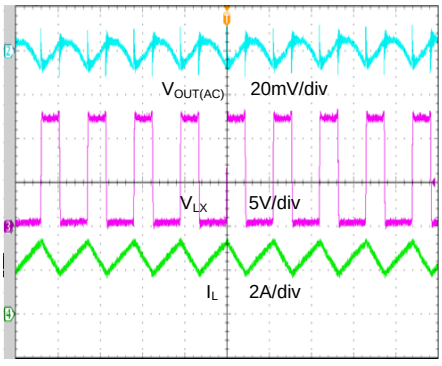
Time (100μs/div)

Output Ripple
V_{IN}=5V,V_{OUT}=12V,I_{OUT}=0A



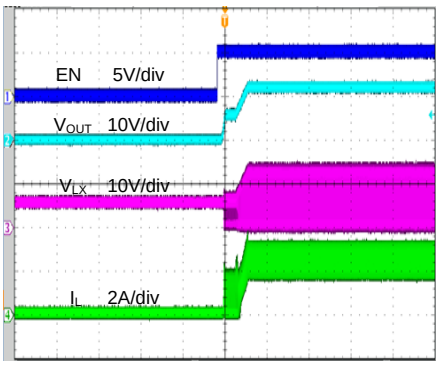
Time (400μs/div)

Output Ripple
V_{IN}=5V,V_{OUT}=12V,I_{OUT}=1A



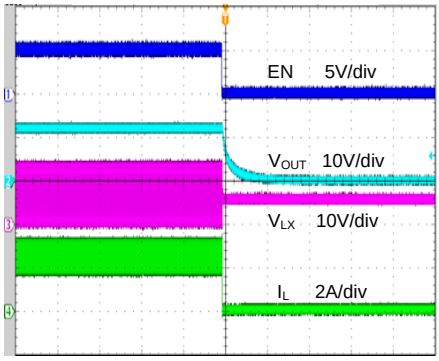
Time (1μs/div)

Startup from Enable
V_{IN}=5.0V, V_{OUT}=12V, Io=1.0A



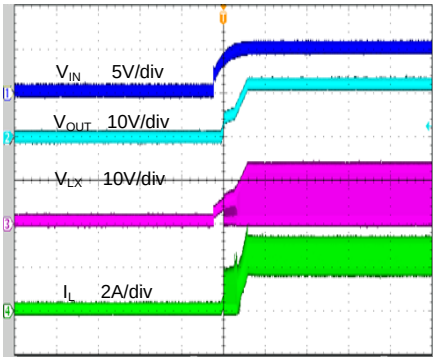
Time (10ms/div)

Shutdown from Enable
V_{IN}=5.0V, V_{OUT}=12V, Io=1.0A



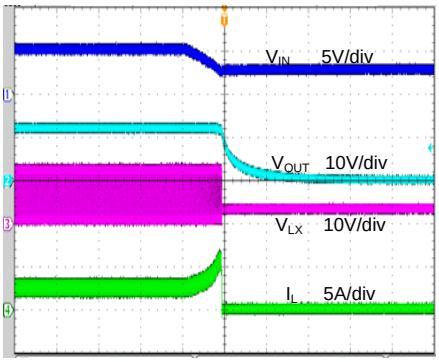
Time (800μs/div)

Startup from VIN
V_{IN}=5.0V, V_{OUT}=12V, Io=1.0A



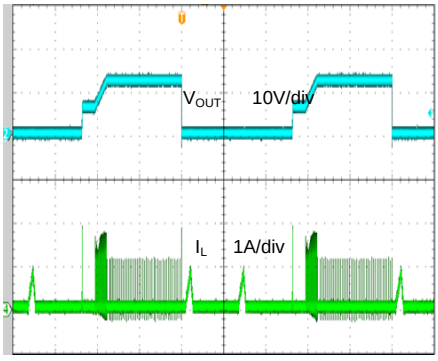
Time (10ms/div)

Shutdown from VIN
V_{IN}=5.0V, V_{OUT}=12V, Io=1.0A



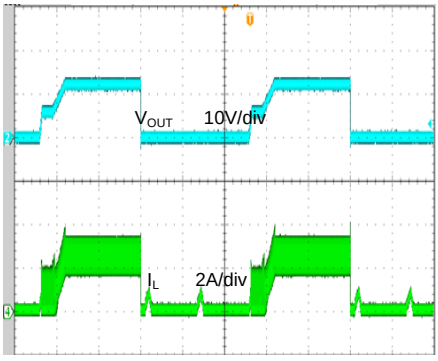
Time (400µs/div)

Short circuit Protection
V_{IN}=5.0V, V_{OUT}=12V, Io=0A to Short



Time (10ms/div)

Short circuit Protection
V_{IN}=5.0V, V_{OUT}=12V, Io=1A to Short



Time (10ms/div)

Detailed Description

The SY21282 high efficiency synchronous step-up regulator operates using adaptive constant off-time and current mode control, over a wide input voltage range from 3V to 9V. It integrates switches with low $R_{DS(ON)}$ to minimize conduction loss.

The SY21282 features cycle-by-cycle peak current limit, output short-circuit protection, and true shutdown. It also provides enable control and power-good indicator for system sequence control. The 1MHz pseudoconstant frequency reduces output voltage ripple and permits smaller external capacitors and inductor.

Enable Operation

Driving the EN pin high (>1.5V) enables normal operation. Driving the EN pin low (<0.4V) will place the device in shutdown. During shutdown mode, the SY21282 shutdown current drops to less than 7μA.

Switch Frequency

The SY21282 operates under 1MHz pseudo-constant frequency in Continuous Conduction Mode (CCM). Under light load conditions, the SY21282 linearly folds back the frequency, thus minimizing the output ripple.

Power-Good Indication

PG is an open-drain output pin. This pin is driven low if the output voltage is lower than 90% of the target regulation voltage, or if OVP is triggered. Otherwise, this pin is in a high impedance state.

Overcurrent Limit and Short-Circuit Protections

The SY21282 features overcurrent limit and short-circuit protections. The output current is sensed on the disconnection FET and mirrored to the I_{LIM} by sourcing a current with a ratio of 1/10000.

The output overcurrent limit can be configured using the following equation:

$$I_{LIM}(A) = 10(V)/ R_{LIM}(k\Omega)$$

Under overcurrent conditions, if V_{OUT} is lower than V_{IN}, the current through the disconnection FET is limited by controlling its gate drive voltage. If V_{OUT} is equal to or higher than V_{IN}, the disconnection FET is fully ON, and the current limit is achieved by limiting the peak inductor current, which is controlled by the current control loop.

Under severe overcurrent conditions, if the OUT pin voltage drops below 2V, the device will immediately shut down and try to restart after a 5ms delay.

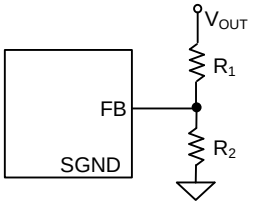
Application Information

The following paragraphs describe the selection process for the feedback resistor divider (R1 and R2), output current limit resistor R_{LIM}, input capacitor C_{IN}, output capacitors C_{BD} and C_{OUT}, boost inductor L, and external bootstrap capacitor.

Feedback Resistor Divider R1 and R2

Choose R1 and R2 to program the proper output voltage. Choose large resistance values between 10kΩ and 1MΩ for both R1 and R2 to minimize power consumption under light loads. If a value of 200kΩ is chosen for R1, then R2 can be calculated as:

$$R_2 = \frac{R_1}{V_{OUT} - 1}(\Omega)$$



Input Capacitors C_{IN}, C_{IN1}

Input filter capacitors reduce the ripple voltage on the input, filter the switched current drawn from the input supply, and reduce potential EMI. When selecting an input capacitor, be sure to select a voltage rating at least 20% greater than the maximum voltage of the input supply and a temperature rating higher than the system requirements. X5R series ceramic capacitors are most often selected due to their small size, low cost, surge-current capability, and high RMS current ratings over a wide temperature and voltage range. However, systems that are powered by a wall adapter or other long and therefore inductive cabling may be susceptible to significant inductive ringing at the input to the device. In these cases, consider adding some bulk capacitance like electrolytic, tantalum, or polymer type capacitors. Using a combination of bulk capacitors (to reduce overshoot or ringing) in parallel with ceramic capacitors (to meet the RMS current requirements) is helpful in these cases.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

$$I_{CIN\_RMS} = \frac{V_{IN} \cdot (V_{OUT} - V_{IN})}{2\sqrt{3} \cdot L \cdot F_{SW} \cdot V_{OUT}}$$

For the best performance, select a typical X5R or better grade low ESR 10μF ceramic capacitor and place it as close as possible to the V_{IN} and PGND pins. Minimize the loop area formed by C_{IN}, V_{IN}, and the PGND pin.

The SVIN capacitor must be placed as close as possible to the SVIN and SGND pins. Minimize the loop area formed by C_{IN} and the SVIN/SGND pins. A 2μF low ESR ceramic capacitor is recommended for most applications.

A resistor, R_{IN1}, with a value of 10Ω is recommended to be used between the VIN input and the SVIN pin. Together with the C_{IN1} capacitor, this helps filter the switching noise coming into the SVIN pin.

Boost Output Capacitor C_{BD} and Disconnection FET Output Capacitor C_{OUT}

The boost output capacitor C_{BD} and disconnection FET output capacitor C_{OUT} are selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be considered when selecting these capacitors. For the best performance, it is recommended to use X5R or better grade ceramic capacitors with 25V rating and more than 22μF capacitance.

Boost Inductor L

Consider the following when choosing this inductor:

1) Choose the inductance to provide a ripple current that is approximately 40% of the maximum output current. The recommended inductance is calculated as:

$$L = \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \frac{V_{OUT} - V_{IN}}{f_{SW}\, I_{OUT,MAX} \times 0.4}$$

where f_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY21282 has high tolerance for ripple current amplitude variation. As a result, the final choice of inductance can vary slightly from the calculated value with no significant performance impact.

2) The inductor's saturation current rating must be greater than the peak inductor current under full load:

$$I_{SAT,MIN} = \left(\frac{V_{OUT}}{V_{IN}}\right) \times I_{OUT,MAX} + \frac{V_{IN}(V_{OUT} - V_{IN})}{2 \times f_{SW} \times L \times V_{OUT}}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. Choose an inductor with DCR less than 10mΩ to achieve good overall efficiency.

Maximum Output Current Estimation

The maximum current that the converter can provide to the load depends on the output voltage / input voltage ratio and the current limit for the main MOSFET device.

Use the following formulas to evaluate an approximate max current that the converter can deliver when driving the load.

$$D=1-V_{IN(MIN)}\times\frac{\eta}{V_{OUT}}$$

Estimate the maximum output current:

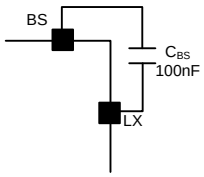
$$I_{MAXOUT} = (IL_{MIN} - \frac{\Delta IL}{2}) \times \frac{\eta \times V_{IN(MIN)}}{V_{OUT}}$$

$$I_{MAXOUT}=\left(I_{LIM(MIN)}-\frac{\Delta IL}{2}\right)\times(1-D)$$

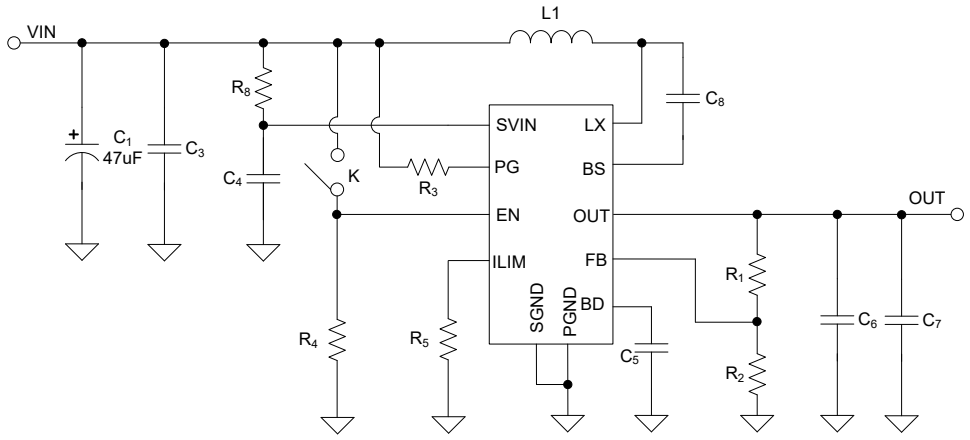
Where: $V_{IN(MIN)}$ is the minimum voltage at the boost input in the application, IL_{MIN} is the minimum device current datasheet limit (6A for SY21282), ΔIL is the current ripple and η is the efficiency, which can be substituted with a value of 0.8 for simplicity.

External Bootstrap Capacitor

This capacitor provides the gate driver voltage for the internal rectifier. A 100nF low ESR ceramic capacitor connected between the BS pin and the LX pin is recommended.



Application Schematic



Design Specifications

Input Voltage (V)	Output Voltage (V)	Output Current Limit (A)
3-9	12	1.8

BOM List

Reference Designator	Description	Part Number	Manufacturer
L1	2.2μH/8.4A	SPM6530T-2R2M	TDK
C1	47μF/50V/Electrolytic capacitor		
C3	10μF, 16V, 1206	C3216X7R1C106K	TDK
C4	1μF, 25V, 0603	C1608X7R1E105K	TDK
C5, C6, C7	22μF,16V,1206	C3216X5R1C226K	TDK
C8	100nF,50V,0603	C1608X7R1H104K	TDK
R1, R3	100k,0603	RC0603FR-07100KL	YAGEO
R2	9.09k,0603	RC0603FR-079K09L	YAGEO
R4	1Mk,0603	RC1206FR-071ML	YAGEO
R5	5.1k,0603	RC1206FR-075K11L	YAGEO
R7	0,0603	RC0603FR-070RL	YAGEO
R8	2R,0603	RC0603FR-072RL	YAGEO

Recommend Components for Typical Applications

V_{OUT}(V)	R_H(kΩ)	R_L(kΩ)	L(μH)	C_{OUT}
6	100	20	2.2	2×22μF/16V/X7R,1206
9	100	12.4	2.2	2×22μF/16V/X7R,1206
12	100	9.09	2.2	2×22μF/16V/X7R,1206

Layout Design

To achieve optimal design, follow these PCB layout considerations:

- Place C_{IN}, C_{IN1}, C_{BD}, C_{OUT}, L, R1, and R2 close to the device.
- To achieve the best thermal and noise performance, maximize the PCB copper area connecting to the GND pin. A ground plane is highly recommended if cost allows.
- C_{IN} must be close to pins SVIN and SGND. Minimize the loop area formed by C_{BD} and the LX and PGND pins.
- To reduce switching noise, minimize the PCB copper area connected to the LX pin.
- In order to reduce crosstalk, R1, R2, and the trace connected to the FB pin must not be adjacent to the LX net on the PCB layout.
- If the system chip interfacing with the EN pin has a high impedance state during shutdown mode, and the SVIN pin is connected directly to a power source such as a Li-ion battery, add a 1MΩ pulldown resistor between the EN and GND pins to prevent noise from falsely triggering the regulator during shutdown mode.

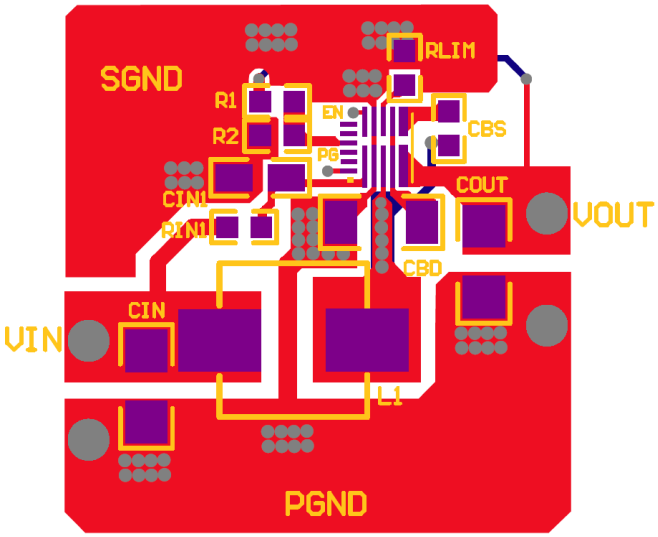
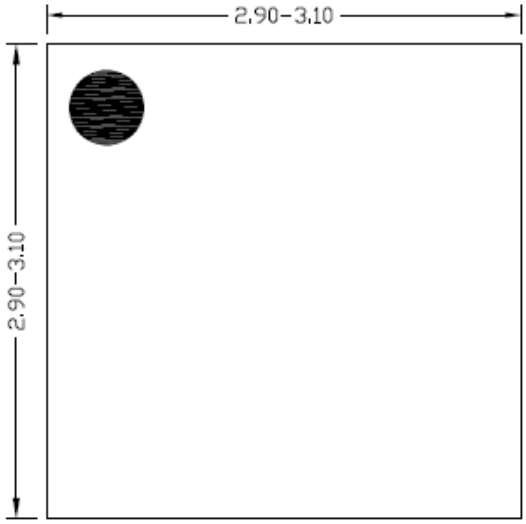
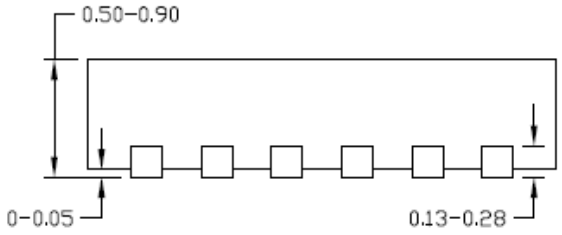


Figure 4. Suggested PCB Layout

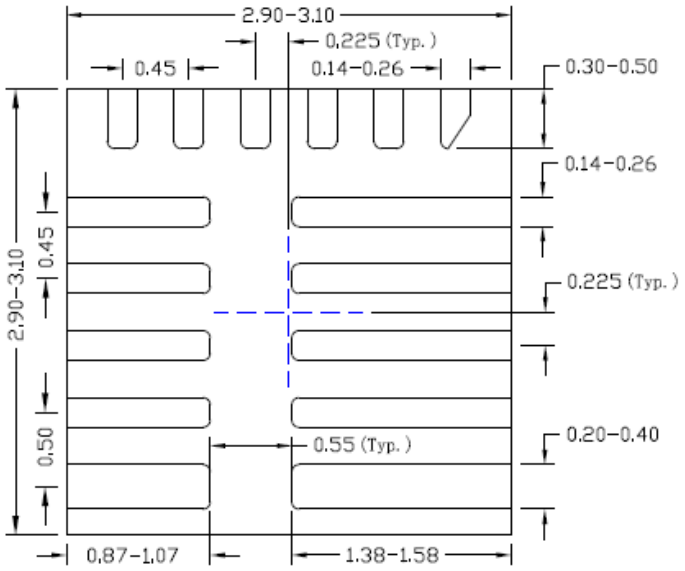
QFN3×3-16 Package Outline



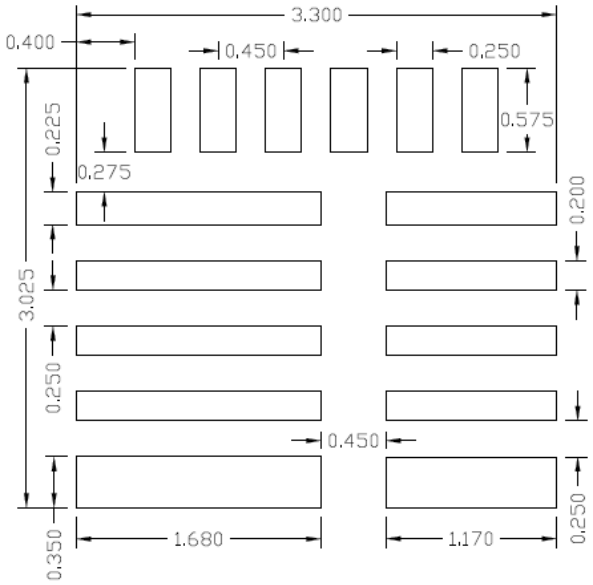
Top view



Side view



Bottom view

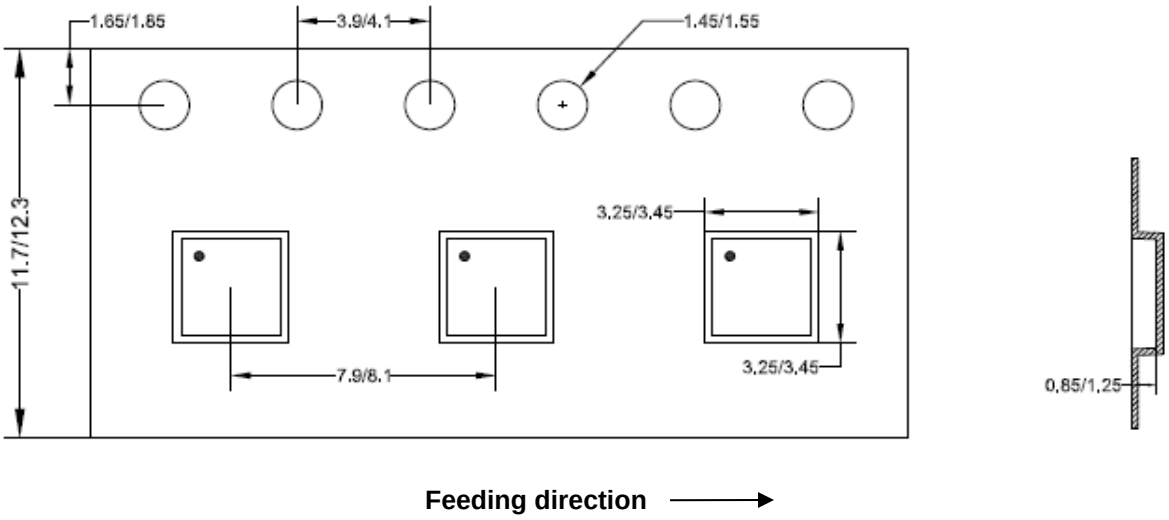


Recommended PCB layout
(Reference only)

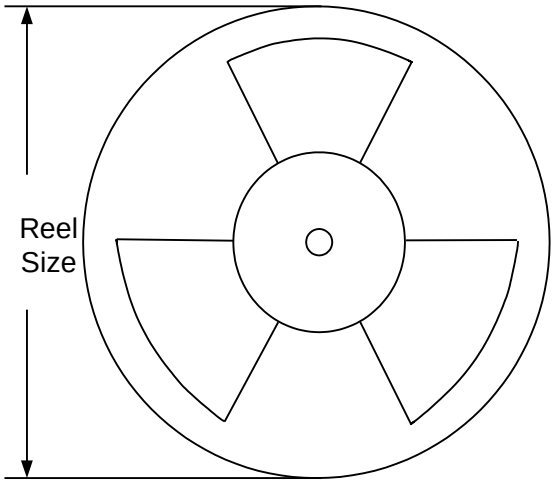
Note: *All dimensions are in millimeters and exclude mold flash and metal burr.*

Taping and Reel Specification

QFN3×3 taping orientation



Carrier tape and reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN3×3	12	8	13"	400	400	5000

Others: NA

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
June 17, 2023	Revision 1.0	Language improvements for clarity.
Feb.22, 2019	Revision 0.9D	Modify the formula in "Output Inductor L" (page 9) From $I_{SAT,\,MIN} > \left(\frac{V_{OUT}}{V_{IN}}\right) \times I_{OUT,\,MAX} + \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \frac{(V_{OUT} - V_{IN})}{2 \times F_{SW} \times L}$ To $I_{SAT\_MIN} > \left(\frac{V_{OUT}}{V_{IN}}\right) \times I_{OUT\_MAX} + \frac{V_{IN}}{V_{OUT}} \frac{(V_{OUT} - V_{IN})}{2 \times f_{SW} \times L}$
Nov.26, 2018	Revision 0.9C	1. Revise the test condition for Shutdown Current in EC table; 2. Add Recommended PCB layout (Reference only) in Package Outline.
July 13. 2015	Revision 0.9B	Update the Absolute Maximum Ratings for LX pin (page 4)
June 24, 2015	Revision 0.9A	Update the application info. Of " over current limit and short circuit protection" (Page 8)
Nov.25, 2014	Revision 0.9	Initial Release

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