SY20466/SY20466A

1.8V Minimum Input, 5.5V Maximum Output, 6A Peak-Current Synchronous Boost Converter with Output Disconnect

General Description

The SY20466/SY20466A high-efficiency synchronous Boost regulator has an input voltage range of 1.8V to 5.25V and can output an output voltage up to 5.5V. The device uses a NMOS MOSFET for the main switch and a PMOS for the synchronous switch. The output is disconnected from the input during shutdown mode and features programmable output-current limit using the I_{LIM} pin.

The SY20466/SY20466A is available in a compact QFN2mmx2mm-10 package.

Applications

Single-cell Lithium or Dual-Cell Nickel Battery-Powered Devices (MP3 players, PDAs, etc.)

Features

- 1.8V Minimum Input Voltage
- Adjustable Output Voltage from 2.5V to 5.5V
- 6A Peak Current Limit
- Input Undervoltage Lockout
- Quiescent Current: 27 µA (typ.)
- Shutdown Current: 0.1 µA (typ.)
- Load Disconnect During Shutdown
- Output Overvoltage Protection
- Input Battery Voltage Monitor
- Low $R_{DS(ON)}$ for Internal Switches at 5.0V Output: 20mΩ Main, 40mΩ Synchronous
- Automatic Output Discharge at Shutdown:
  - SY20466: Automatic Output Discharge Function
  - SY20466A: No Output Discharge Function
- Compact Package: QFN2mmx2mm-10

Typical Application

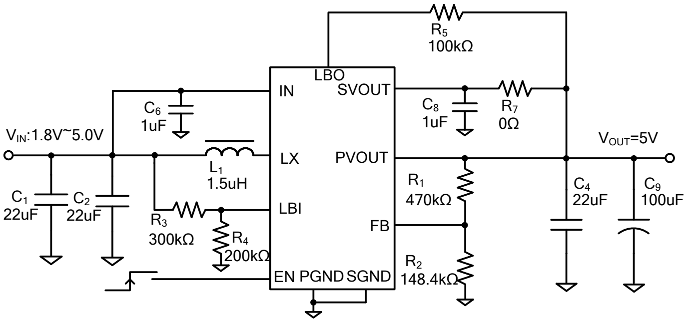


Figure 1. Schematic Diagram

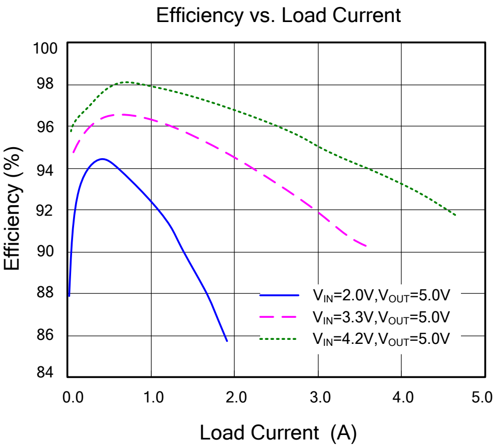


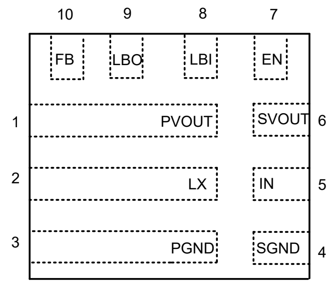
Figure 2. Efficiency vs. Load Current

Ordering Information

Ordering Part Number	Package Type	Top Mark
SY20466QMC	QFN2×2-10 RoHS-Compliant and Halogen-Free	**MG*xyz***
SY20466AQMC	QFN2×2-10 RoHS-Compliant and Halogen-Free	**A*axyz***

***x* = year code, *y* = week code, *z* = lot number code**

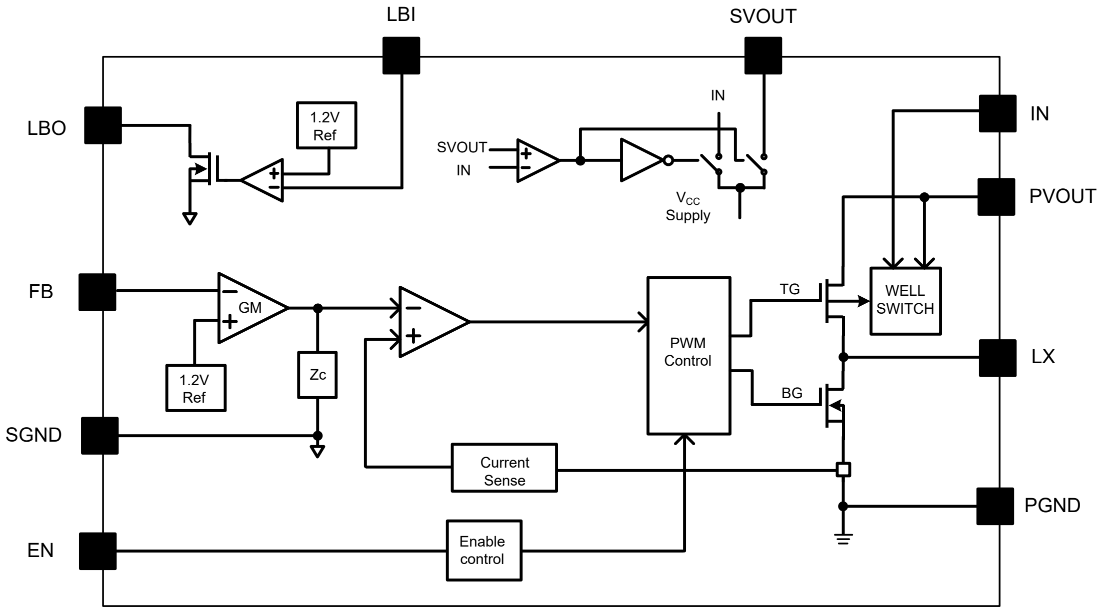
Pinout (top view)



Pin Description

Pin Name	Pin Number	Pin Description
PVOUT	1	Power output pin. Decouple this pin to the GND pin with at least a 22µF ceramic capacitor.
LX	2	Inductor pin. Connect an inductor between the IN pin and the LX pin.
PGND	3	Power ground pin.
SGND	4	Signal ground pin.
IN	5	Signal input pin. Decouple this pin to GND with at least a 4.7µF ceramic capacitor.
SVOUT	6	Signal output pin. Decouple this pin to GND with at least a 1µF ceramic capacitor for noise immunity consideration.
EN	7	Enable pin. Internally integrated 1MΩ pulldown resistor.
LBI	8	Low-battery comparator input.
LBO	9	Low-battery comparator output (open-drain).
FB	10	Feedback pin. Connect a resistor R1 between OUT and FB, and a resistor R2 between FB and GND to program the output voltage. $V_{OUT} = 1.2V \times (R1/R2 + 1)$.

Functional Block Diagram



Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
EN		V_{OUT}+0.3	V
PVOUT, LX, IN, SVOUT, LBI, LBO, FB		6	
Lead Temperature (Soldering, 10s)		260	°C
Junction Temperature, Operating	-40	150	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	50	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	10	
P_D Power Dissipation T_A = 25°C	2.5	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
IN	1.8	5.25	V
PVOUT, SVOUT	2.5	5.5	
EN	0	V_{OUT} + 0.3	
LX, LBI, LBO, FB	0	5.5	
Junction Temperature, Operating	-40	125	°C
Ambient Temperature	-40	85	

Electrical Characteristics

(V_{IN} = 2.4V, V_{OUT} = 5V, I_{OUT} = 500mA, T_A = 25°C unless otherwise specified.)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage		V_{IN}		1.8		5.25	V
Output Voltage Range		V_{OUT}		2.5		5.5	V
Quiescent Current	V_{IN}	I_Q	I_O = 0A, V_{EN} = V_{IN} = 1.8V, V_{OUT} = 5.0V		10		µA
	V_{OUT}				27		µA
Shutdown Current		I_{SHDN}	V_{EN} = 0V, V_{IN} = 2.4V		0.1	1	µA
Linear Charge Current		I_{CHARGE}	$V_{OUT} \leq$ 1V		1.2		A
			1V < V_{OUT} < 90%V_{IN}		1.0		
Soft-Start Time		t_{SS}			1		ms
Input UVLO Threshold		V_{UVLO}				1.78	V
Input UVLO Hysteresis		V_{HYS}			0.1		V
EN Rising Threshold		V_{ENH}		1.2			V
EN Falling Threshold		V_{ENL}				0.4	V
LBI Voltage Threshold		V_{LBI}		1.176	1.2	1.224	V
LBI Input Hysteresis		V_{LBI_HYS}			20		mV
Low-Side Main FET R_{ON}		$R_{DS(ON)1}$	V_{OUT} = 5.0V		20		mΩ
Synchronous FET R_{ON}		$R_{DS(ON)2}$	V_{OUT} = 5.0V		40		mΩ
Main FET Current Limit		I_{LIM1}		6.0			A
Switching Frequency		f_{SW}			500		kHz
Feedback Reference Voltage		V_{REF}		1.182	1.2	1.218	V
Output Overvoltage Protection		V_{OVP}			6		V
Minimum On-Time		t_{ON_MIN}			100		ns
Minimum Off-Time		t_{OFF_MIN}			100		ns
Max On-Time		t_{ON_MAX}			2		µs
Thermal Shutdown Temperature		T_{SD}			150		℃
Thermal Shutdown hysteresis		T_{HYS}			20		℃
Output Discharge Resistor		R_{DSC}			80		Ω

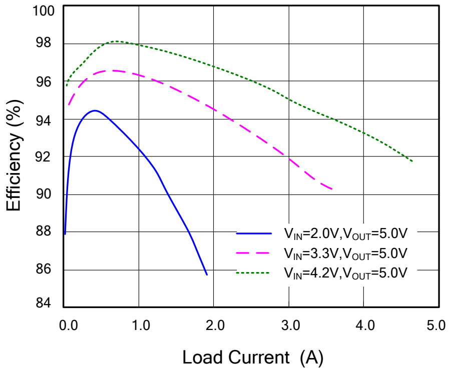
Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a four-layer Silergy evaluation board.

Note 3: The device is not guaranteed to function outside its operating conditions.

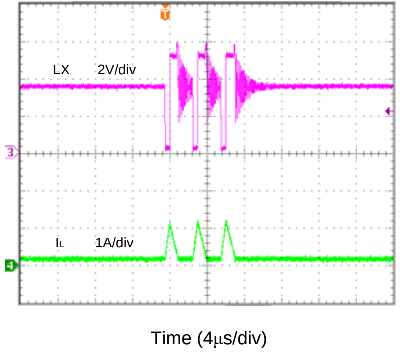
Typical Performance Characteristics

Efficiency vs. Load Current



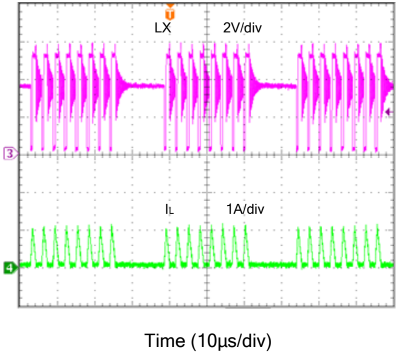
Steady State

(V_{IN}=3.3V, V_{OUT}=5.0V, I_{LOAD}=0A)



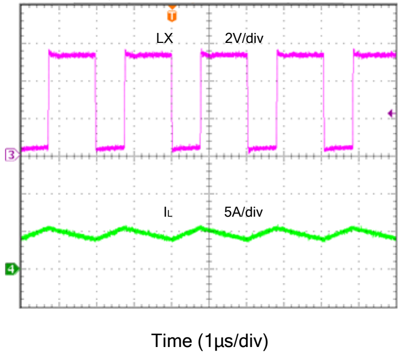
Steady State

(V_{IN}=3.3V,V_{OUT}=5.0V, I_{LOAD}=0.1A)



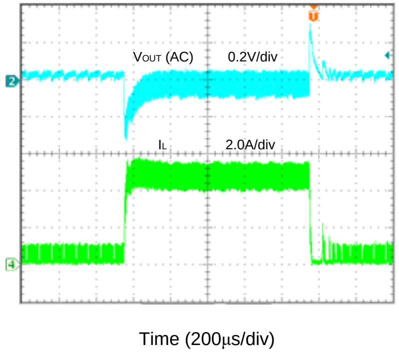
Steady State

(V_{IN}=3.3V,V_{OUT}=5.0V, I_{LOAD}=3.0A)



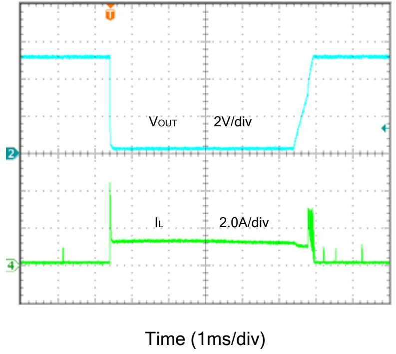
Load Transient

(V_{IN}=3.3V, V_{OUT}=5.0V, I_{LOAD}=0.3-2.8A)



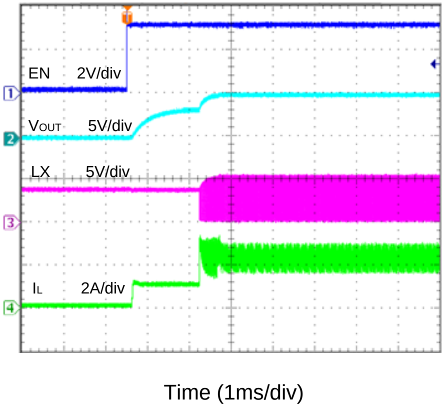
Short Circuit

(V_{IN}=3.3V, V_{OUT}=5.0V, I_{LOAD}=0.3A to Short Circuit)



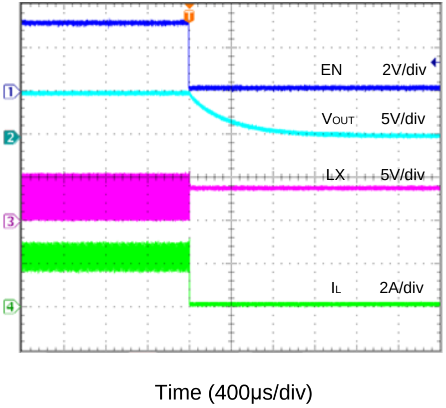
Startup from Enable

(V_{IN}=3.3V, V_{OUT}=5.0V, I_{LOAD}=1.4A)



Shutdown from Enable

(V_{IN}=3.3V, V_{OUT}=5.0V, I_{LOAD}=1.4A)



Application Information

Operation

The SY20466/SY20466A uses constant-frequency peak-current control to regulate the output voltage. A PWM cycle initiated by the internal clock turns the bottom FET on, which remains on until its current reaches the value set by V_{COMP}. When the PWM signal goes low, the bottom FET turns off and remains off until the next cycle starts. When V_{FB} drops below the internal reference voltage (V_{REF}), V_{COMP} will be driven higher, so the switch peak current becomes higher and the IC delivers more energy to the output. Conversely, when V_{FB} rises above V_{REF}, the V_{COMP} will be driven lower and the switch peak current output drops. See Figure 3 for details.

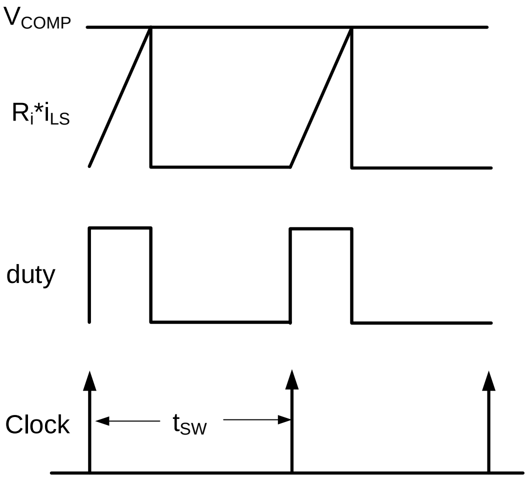


Figure 3. Constant-On-Time Peak-Current Control

The following paragraphs describe the selection process for the input capacitor C_{IN}, the output capacitor C_{OUT}, the inductor L, and the feedback resistor-divider (R1 and R2).

Feedback Resistor-Divider R1 and R2:

Choose R1 and R2 in the feedback resistor-divider to configure the output voltage. A value between 10kΩ and 1MΩ is recommended for both resistors to minimize power consumption under light loads. If V_{OUT} = 5.0V and R1 is chosen to be 470kΩ, then R2 can be calculated as 148.4kΩ using the following formula:

$$R_2 = \frac{1.2V}{V_{OUT} - 1.2V} R_1$$

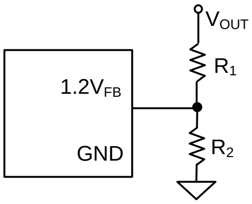


Figure 4. Feedback Resistor-Divider

Input Capacitor C_{IN}

Input filter capacitors reduce the ripple voltage on the input, filter the switched current drawn from the input supply, and reduce potential EMI. When selecting an input capacitor, be sure to select a voltage rating at least 20% greater than the maximum voltage of the input supply and a temperature rating higher than the system requirements. X5R or X7R series ceramic capacitors are most often selected due to their small size, low cost, surge-current capability, and high RMS current ratings over a wide temperature and voltage range. Systems that are powered by a wall adapter or other long and therefore inductive cabling may be susceptible to significant inductive ringing at the input to the device. In these cases, consider adding some bulk capacitance like electrolytic, tantalum, or polymer type capacitors. Using a combination of bulk capacitors (to reduce overshoot or ringing) in parallel with ceramic capacitors (to meet the RMS current requirements) is helpful in these cases.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

The ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2\sqrt{3} \times L\, f_{SW} \times V_{OUT}}$$

For the best performance, select a typical X5R or better grade ceramic capacitor with a 6.3V rating and at least 22µF capacitance.

Li-Ion Battery Hot Plug Consideration

In the mass production stage, the Li-Ion battery will always hot plug between the IN and GND pins. The hot plug may lead to large voltage spikes, or even to device electrical overstress (EOS) failure. To avoid this potential risk, place one 22µF ceramic capacitor in series with a 0.1Ω resistor to absorb the input voltage spike. With this solution, the voltage spike can be reduced from 6.12V to 5.2V in order to meet the device absolute maximum operating conditions. See Figures 5, 6, and 7 for more details.

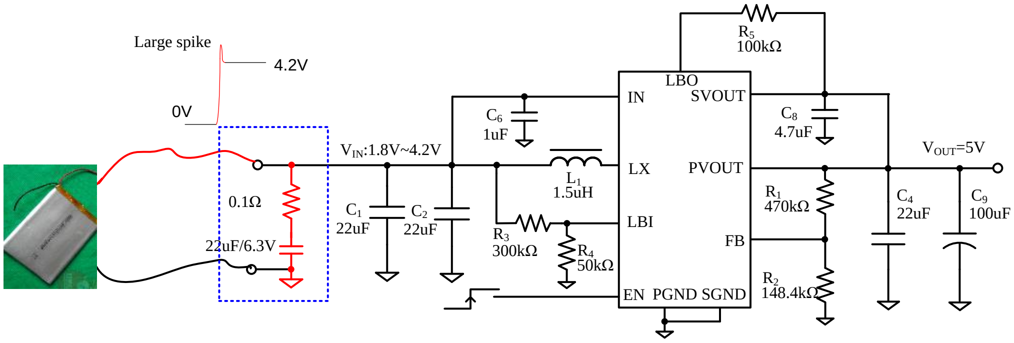


Figure 5. Voltage Spike Suppression

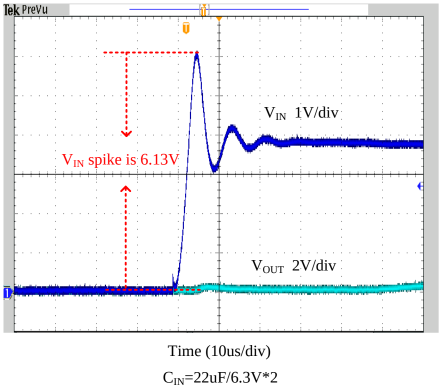


Figure 6. Voltage Spike without Suppression

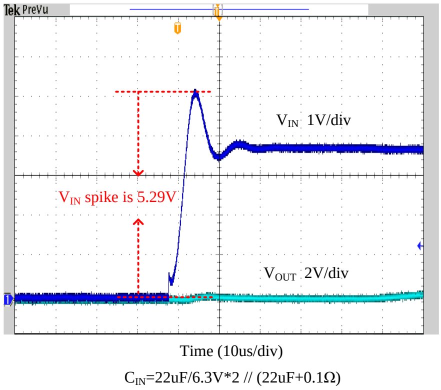


Figure 7. Voltage Spike with Suppression

Inductor L

Consider the following when choosing this inductor:

- Choose the inductance to provide a ripple current that is approximately 40% of the maximum output current. The recommended inductance is calculated as:

$$L=\left(\frac{V_{IN}}{V_{OUT}}\right)^2\frac{(V_{OUT}-V_{IN})}{f_{SW}\times I_{OUT,\,MAX}\times 40\%}$$

  where f_{SW} is the switching frequency and I_{OUT_MAX} is the maximum load current.

  The SY20466/SY20466A has high tolerance for ripple-current amplitude variation. As a result, the final choice of inductance can vary slightly from the calculated value with no significant performance impact.

- The saturation-current rating of the inductor must be selected to be greater than the peak inductor current under full-load conditions.

$$I_{SAT,MIN}>\left(\frac{V_{OUT}}{V_{IN}}\right)\times I_{OUT,MAX}+\frac{V_{IN}(V_{OUT}-V_{IN})}{2\times f_{SW}\times L\times V_{OUT}}$$

- The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. Choose an inductor with DCR lower than 50mΩ to achieve a good overall efficiency.

Output Capacitor C_{OUT}

For applications where the design must meet stringent ripple requirements, the following considerations must be followed:

The output-voltage ripple at the switching frequency is caused by the inductor-current ripple (ΔI_L) on the output capacitor's ESR (ESR ripple), as well as the stored charge (capacitive ripple). When calculating total ripple, both should be considered.

$$V_{RIPPLE,\ ESR1} = I_{LPEAK} \times ESR$$
$$V_{RIPPLE,\ ESR2} = I_{LVALLEY} \times ESR$$
$$V_{RIPPLE,CAP} = \frac{I_{OUT} \times (1\text{-}D)}{C_{OUT} \times f_{SW}}$$

The capacitive ripple might be higher because the effective capacitance for ceramic capacitors decreases with the voltage across the terminals. The voltage derating is usually included as a chart in the capacitor datasheet, and the ripple can be recalculated after taking the target output voltage into account.

Inductor vs. Output Capacitor

Select the output capacitor C_{OUT} to handle the output ripple requirements. Both steady-state ripple and transient requirements must be taken into consideration when selecting C_{OUT}. For the best performance, use an X5R or better grade ceramic capacitor with a 10V rating and a capacitance that is more than specified in Table1. Care should be taken to minimize the loop area formed by C_{OUT} and the OUT/GND pins. In some cases, reducing the number of ceramic capacitors and adding in parallel a tantalum capacitor with a 16V rating and at least 100μF capacitance can provide a lower cost solution.

All continuous-mode boost converters have a right-half-plane zero (RHP zero) due to the inductor being removed from the output during charging. In a converter with current-mode control, the current feedback loop allows the switch, inductor, and modulator to be lumped together into a small signal variable current source, as shown in Figure 8.

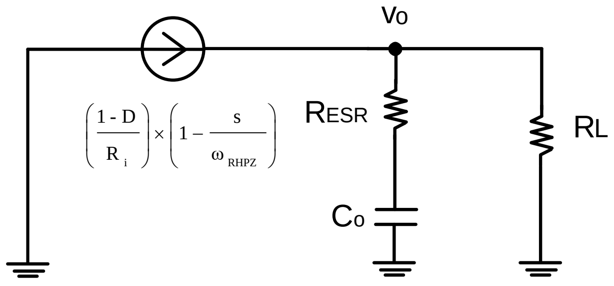


Figure8. Current Feedback Loop

The power stage approximate transfer function is:

$$G_c(s) = \frac{(1-D) \times R_L}{R_i} \times \frac{\left(1+\frac{s}{\omega_{ESR}}\right)\left(1-\frac{s}{\omega_{RHPZ}}\right)}{1+\frac{s}{\omega_p}}$$

where:

$$\omega_{ESR} = \frac{1}{R_{ESR} C_O}$$

$$\omega_p = \frac{1}{(R_{ESR} + R_L) \times C_O}$$

$$\omega_{RHPZ} = \frac{R_L}{L} \times \left(\frac{V_{IN}}{V_{OUT}}\right)^2$$

As Equation 6 shows, the transfer function for boost conversion with current-mode control consists of one ESR zero, one RHP zero, and one pole. The RHP zero provides a 20dB/decade gain increase and 90 degrees of phase drop. Therefore, the bandwidth of the boost converter must be lower than f_{RHPZ}.

As shown in Equation 9, the RHP zero depends on R2, L, and the duty cycle. Larger inductors lead to lower f_{RHPZ}, so bandwidth should be designed lower than f_{RHPZ}.

Some low-profile applications may benefit from using the ceramic capacitor solution, and some low-cost applications may benefit from using an electrolytic capacitor to reduce BOM cost.

Table 1. Inductance vs. Output Capacitor Selection

Inductance		Low-Profile Capacitor Application		Low-Cost Capacitor Application
Part Number	**L(μH)**	**Part Number**	**C_{OUT} (μF)**	**C_{OUT} (μF)**
SPM6530T-1R0M	1.0	C3216X5R1A226M	22μF/10V×3pcs	22μF/10V+100uF(E-cap)
SPM6530T-1R5M	1.5	C3216X5R1A226M	22μF/10V×4pcs	22μF/10V+100uF(E-cap)
SPM6530T-2R2M	2.2	C3216X5R1A226M	22μF/10V×5pcs	22μF/10V+200uF(E-cap)

Enable Operation

Pulling the EN pin high (>1.2V) enables normal operation. Pulling the EN pin low (<0.4V) will shut down the device. During shutdown mode, the SY20466/SY20466A shutdown current drops to less than 1μA.

Low-Battery Detector Function LBI/LBO

The low-battery detector function is used for monitoring the battery voltage and generating an error flag when the battery voltage drops below a user-defined threshold voltage.

This function is only active when the device is enabled. When the device is disabled, the LBO remains high impedance. The detection threshold is 1.2V at the LBI pin. During normal operation, the LBO remains high impedance when the voltage applied at LBI is above the threshold. It is active-low when the voltage at LBI goes below 1.2V.

The battery voltage at which the detection circuit switches can be programmed with a resistive divider connected to the LBI pin. The resistive divider scales down the battery voltage to a voltage level which is compared to the LBI threshold voltage. The LBI pin has a built-in hysteresis of 20mV. If the low-battery detection circuit is not used, the LBI pin should be connected to GND (or to the V_{BAT}) and the LBO pin can be left unconnected. Do not leave the LBI pin floating.

R3 and R4 are designed to program the proper low-battery threshold voltage. The voltage across R_4 is equal to the LBI voltage threshold that is generated on-chip, which has a value of 1.2V. The value of resistor R3, depending on the desired minimum battery voltage V_{BAT}, can be calculated as:

$$R_3 = \frac{V_{BAT} - 1.2V}{1.2V} R_4$$

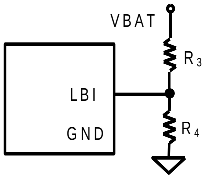


Figure 9. Low-Battery Threshold Setting

The output of the low-battery monitor is an open-drain output that goes active-low if the dedicated battery voltage drops below the programmed threshold voltage on the LBI. The output requires a pullup resistor with a recommended value of 100kΩ. The maximum voltage that is used for pulling up the LBO outputs should not exceed the output voltage of the DC/DC converter. If not used, the LBO pin can be left floating or tied to GND.

Overvoltage Protection

The SY20466/SY20466A provides output overvoltage protection. If the output voltage exceeds V_{OVP} (typ. 6V), the device stops switching, and the main switch is turned off. When the output voltage returns to the normal operating range, the device resumes operation.

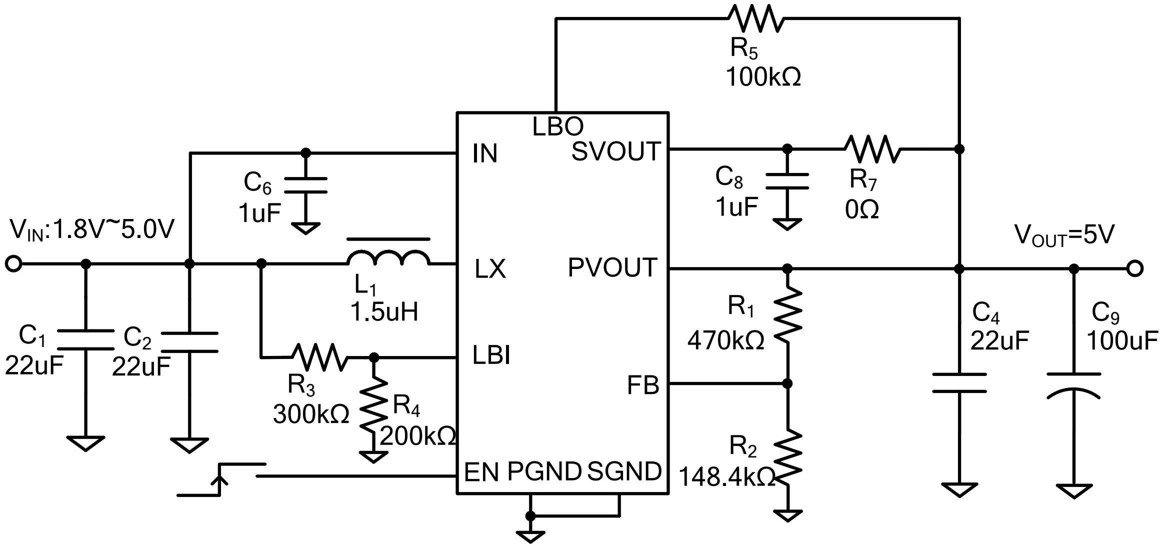
Overcurrent Protection

The SY20466/SY20466A provides cycle-by-cycle overcurrent protection. If the current through the Low-Side MOSFET current reaches the 6A current-limit threshold, it turns off to prevent the input current from increasing further. In this case, the output voltage will decrease until power is balanced between input and output. As soon as the overload condition is removed, the converter resumes operation.

Thermal Protection

The SY20466/SY20466A includes overtemperature protection circuitry to prevent overheating due to excessive power dissipation. This will shut down the device when the junction temperature exceeds 150°C. When the junction temperature cools down by approximately 20°C, the device will resume normal operation after a complete soft-start cycle. For continuous operation, provide adequate cooling so that the junction temperature does not exceed the thermal protection threshold.

Typical Application Schematic



Design Specifications

Input Voltage (V)	Output Voltage (V)	Output Current Limit (A)
1.8-5	5	3

BOM List

Reference Designator	Description	Part Number	Manufacturer
L1	1.5µH/10A	ETQP3W-1R5AFN	SAMPLES
		SPM6530T-1R5M	TDK
C1, C2	22µF/6.3V, 0805, X5R	C2012X5R1A226M	TDK
C4	22µF/10V, 1206, X5R	C3216X5R1A226M	TDK
C6	1µF/25V, 0603, X5R	C1608X5R1E105K	TDK
C8	1µF/25V, 0603, X5R	C1608X5R1E105K	TDK
C9	100µF/25V Electrolytic Capacitor		
R1	470kΩ, 0603, 1%		
R2	150kΩ, 0603, 1%		
R3	300kΩ, 0603, 1%		
R4	200kΩ, 0603, 1%		
R5	100kΩ, 0603, 1%		
R6	1MΩ, 0603, 1%		
R7	0Ω, 0603		

Recommended Components for Typical Applications

V_{OUT}(V)	R2(kΩ)	R1(kΩ)	L(µH)	C_{OUT}
5	470	150	1.5	22µF/10V/X5R,1206+100uF(E-cap)
3.3	510	300	1.5	22µF/6.3V/X5R,1206+100uF(E-cap)

Recommended PCB Layout

Follow these PCB layout guidelines for optimal performance and thermal dissipation:

- Place the following components as close as possible to the IC: C_{IN}, C_{OUT}, L, R1, and R2.
- To achieve the best thermal and noise performance, maximize the PCB copper area connecting to the PGND pin. If board space allows, using a large copper pour connected to GND ground plane is recommended.
- C_{OUT} must be close to the PVOUT and PGND pins. Minimize the loop area formed by C_{OUT} and GND.
- To minimize the output loop area, route the LX trace on the bottom or middle layer through a via.
- SVOUT is the power supply pin for the internal control circuit. Do not connect to the POUT pin directly. A 4.7µF ceramic capacitor is recommended to decouple the SVOUT pin to the SGND pin. Use a trace to connect the SVOUT pin to the output capacitor.
- Minimize the PCB copper area associated with the LX pin to reduce EMI emissions.
- To avoid crosstalk, R1, R2, and the trace connecting to the FB pin must not be adjacent to the LX net on the PCB layout.

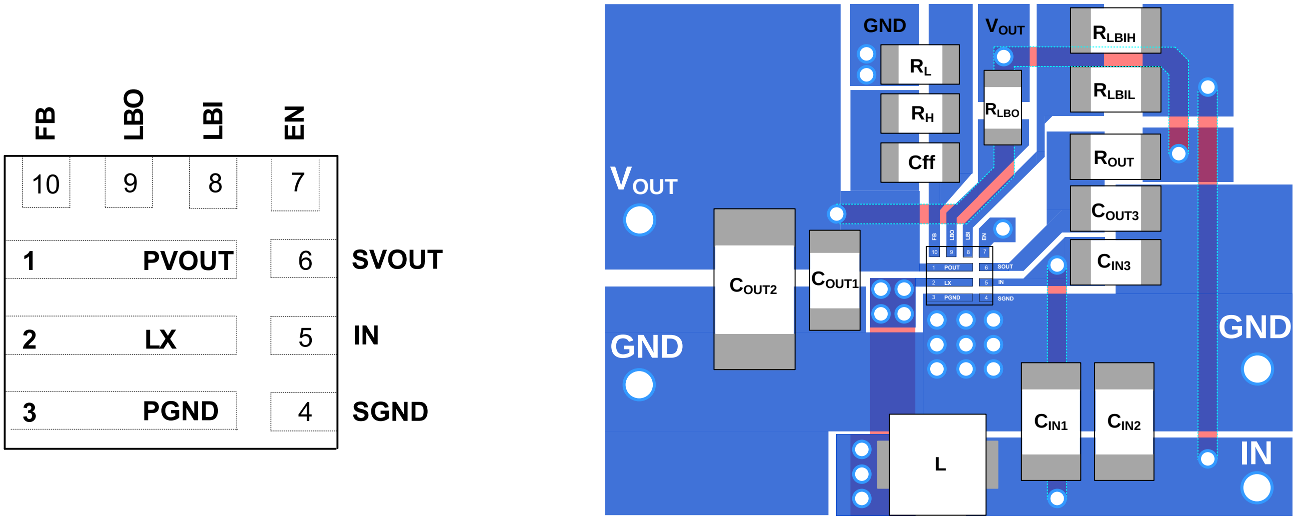
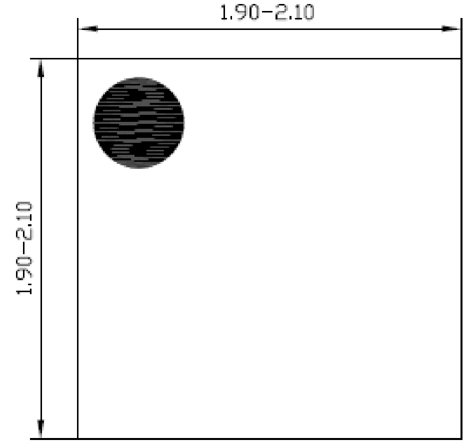
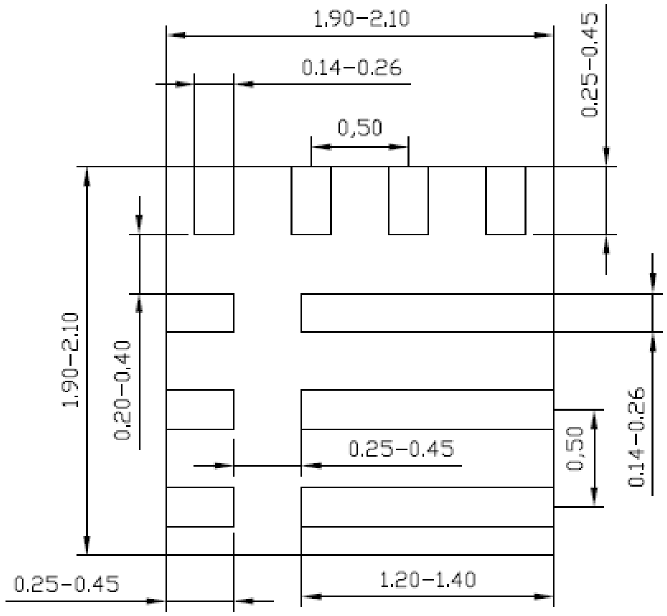


Figure 10. Suggested PCB Layout

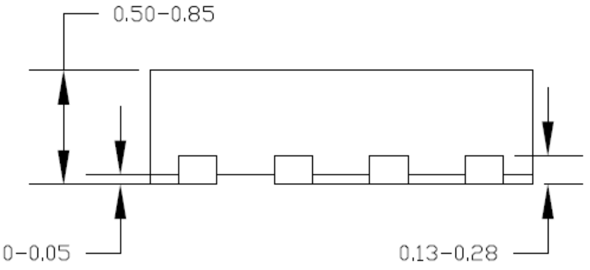
QFN2×2-10 Package Outline



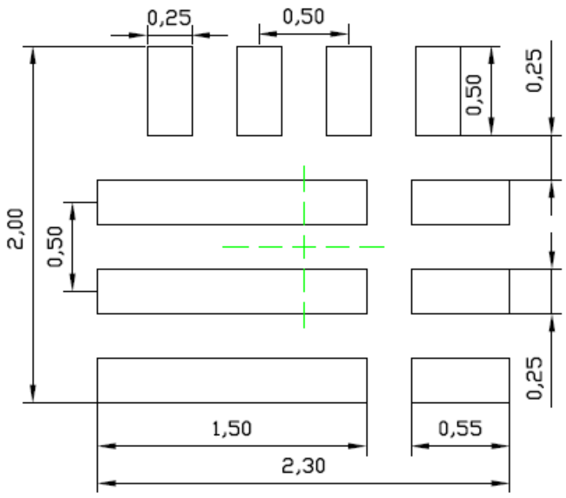
Top view



Bottom view



Side view

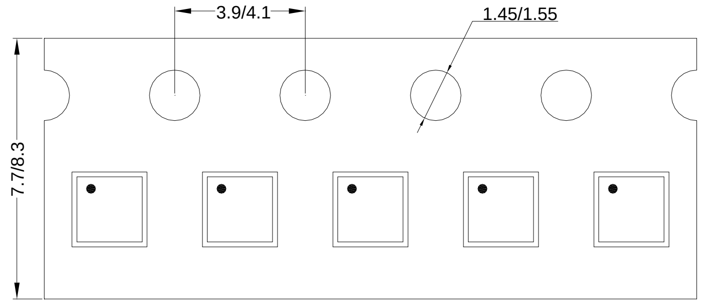


Recommended PCB layout (reference only)

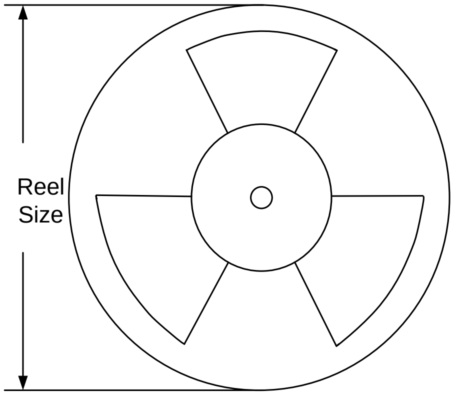
Note: *All dimensions are in millimeters and exclude mold flash and metal burr.*

Taping and Reel Specification

QFN2×2 taping orientation



Carrier tape and reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel (pcs)
QFN2x2	8	4	7"	400	160	3000

Others: NA

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