SY20496

2V Minimum Input, 5.5V Maximum Output, 6A Peak Current Synchronous Boost Converter with Output Current Limit

General Description

The SY20496 high-efficiency synchronous Boost regulator converts down to 2V input and up to 5.5V output voltage. It uses a NMOS for the main switch and a PMOS for the synchronous switch. The device disconnects the output from the input during shutdown mode, and features programmable output-current limit using the I_{LIM} pin.

The SY20496 is available in a compact QFN2mmx2mm-10 package.

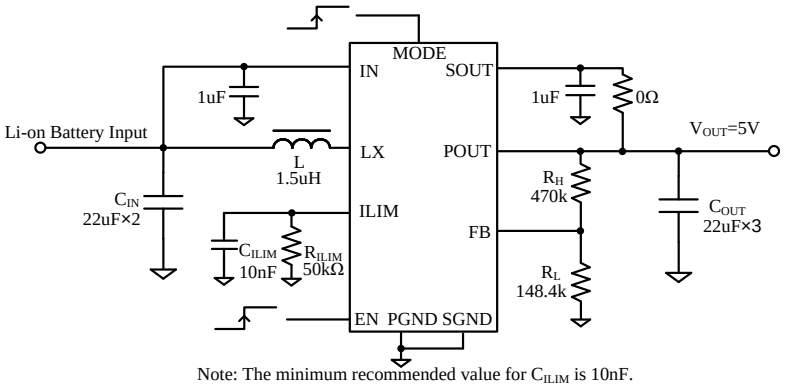
Applications

Single-cell Lithium or Dual-Cell Nickel Battery-Powered Devices (MP3 players, PDAs, etc.)

Features

- 2V Minimum Input Voltage
- Adjustable Output Voltage from 2.5V to 5.5V
- 6A Peak Current Limit
- Input Undervoltage Lockout
- Load Disconnect During Shutdown
- Programmable Output Current Limit Protection
- ±10% Output Current Limit Accuracy
- Selectable Forced-PWM Mode
- Hiccup Mode for Short-Circuit Protection
- Low $R_{DS(ON)}$ for Internal Switches at 5.0V Output: 20mΩ Main, 40mΩ Synchronous
- Output Overvoltage Protection (OVP)
- Compact Package: QFN2mmx2mm-10

Typical Application



Note: The minimum recommended value for C_{ILIM} is 10nF.

Figure 1. Schematic Diagram

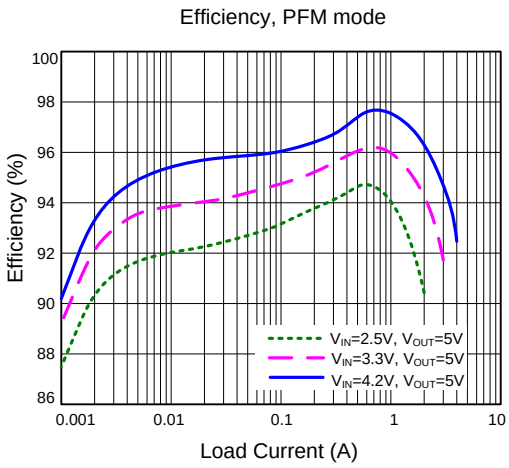


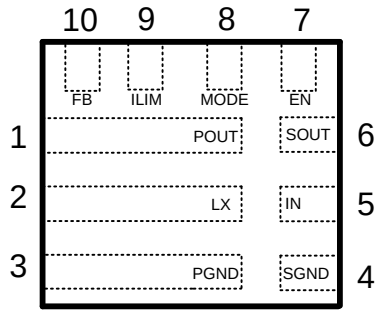
Figure 2. Efficiency vs. Load Current

Ordering Information

Ordering Part Number	Package Type	Top Mark
SY20496QMC	QFN2x2-10 RoHS-Compliant and Halogen-Free	**Fn*xyz***

x = year code, y = week code, z = lot number code

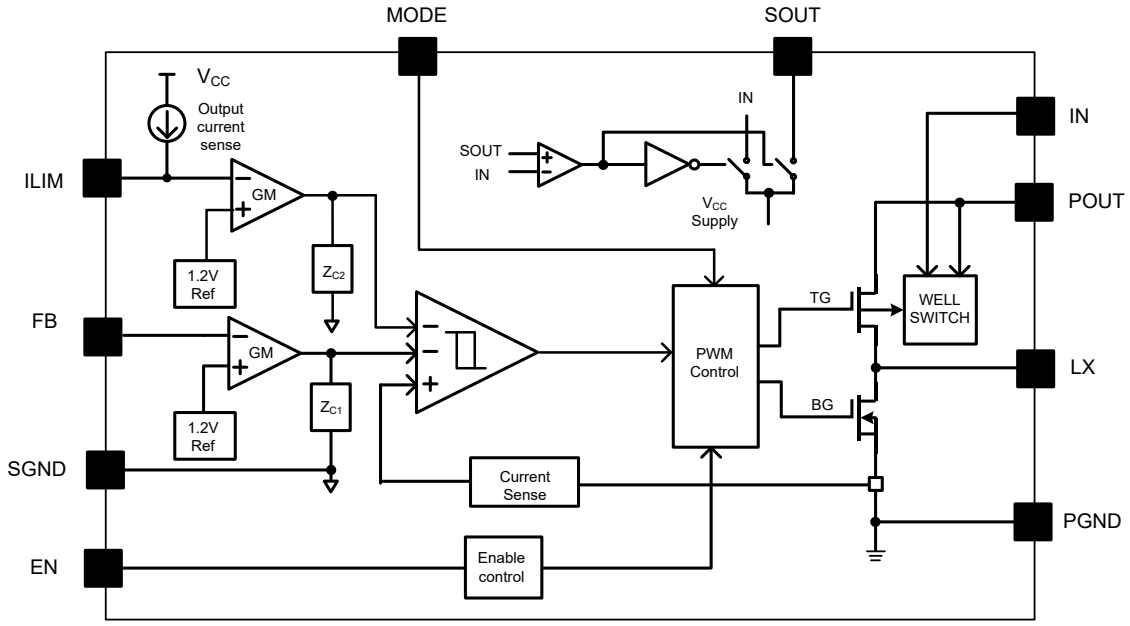
Pinout (top view)



Pin Description

Pin Name	Pin Number	Pin Description
POUT	1	Power output pin. Decouple this pin to the GND pin with at least two 22µF ceramic capacitors.
LX	2	Inductor pin. Connect an inductor between the IN pin and the LX pin.
PGND	3	Power ground pin.
SGND	4	Signal ground pin.
IN	5	Signal input pin. Decouple this pin to GND with at least a 4.7µF ceramic capacitor.
SOUT	6	Signal output pin. Decouple this pin to GND with at least a 1µF ceramic capacitor for noise immunity consideration.
EN	7	Enable pin. Internal integrated with a 1MΩ pulldown resistor.
MODE	8	PFM/PWM select pin. Pull low for auto-PFM/PWM mode, or high for forced-PWM mode. Internally integrated with a 1MΩ pulldown resistor.
ILIM	9	Current-limit program pin. Program the output current limit by connecting a resistor and capacitor parallel network to ground. $I_{LIM}(A) = 100k/R_{ILIM}(\Omega)$. C_{ILIM} must be larger than 10nF.
FB	10	Feedback pin. Connect a resistor R_H between POUT and FB, and a resistor R_L between FB and GND to program the output voltage. $V_{OUT} = 1.2V \times (R_H/R_L + 1)$.

Functional Block Diagram



Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
LX	-0.3	8	V
POUT, IN, SOUT, EN, MODE, ILIM, FB	-0.3	6	
Lead Temperature (Soldering, 10s)		260	°C
Junction Temperature, Operating	-40	150	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	50	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	10	
P_D Power Dissipation $T_{A=}$ 25°C	2.5	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
IN	2	5.5	V
OUT	2.5	5.5	
LX, EN, MODE, ILIM, FB	0	5.5	
Junction Temperature, Operating	-40	125	°C
Ambient Temperature	-40	85	

Electrical Characteristics

(V_{IN} = 3.0V, V_{OUT} = 4.2V, I_{OUT} = 500mA, T_A = 25°C unless otherwise specified.)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage		V_{IN}		2		5.5	V
Output Voltage Range		V_{OUT}		2.5		5.5	V
Quiescent Current	V_{IN}	I_Q	I_O = 0A, V_{EN} = V_{IN} = 3.0V, V_{OUT} = 5.0V		10		μA
	V_{OUT}				27		μA
Shutdown Current		I_{SHDN}	V_{EN} = 0V, V_{IN} = 3.0V		0.1	1	μA
Linear Charge Current		I_{CHARGE}	V_{OUT} < 0.5V_{IN}		2		A
Maximum Linear Charge Time		t_{CHG}			9		ms
Input V_{IN} UVLO Threshold		V_{UVLO}				2.0	V
V_{IN} UVLO Hysteresis		V_{HYS}			0.25		V
MODE and EN Rising Threshold		V_{ENH}		1.2			V
MODE and EN Falling Threshold		V_{ENL}				0.4	V
Low-Side Main FET R_{ON}		$R_{DS(ON)N}$	V_{OUT} = 5.0V		20		mΩ
Synchronous FET R_{ON}		$R_{DS(ON)P}$	V_{OUT} = 5.0V		40		mΩ
Main FET Current Limit		I_{LIM1}		6.0			A
Output Current limit		I_{LIM2}	R_{ILIM} = 100kΩ	0.9	1	1.1	A
Minimum Output Current Limit		$I_{LIM,MIN}$			0.8		A
Switching Frequency		fsw			500		kHz
Feedback Reference Voltage		V_{REF}		1.182	1.2	1.218	V
Minimum On-Time		t_{ON_MIN}			100		ns
Minimum Off-Time		t_{OFF_MIN}			100		ns
Maximum On-Time		t_{ON_MAX}			1.5		us
OUT Pin OVP Protection		V_{OVP}			6.0		V
OUT Pin OVP Hysteresis		$V_{OVP,HYS}$			0.2		V
Thermal Shutdown Temperature		T_{SD}			150		°C
Thermal Shutdown Hysteresis		T_{HYS}			20		°C

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

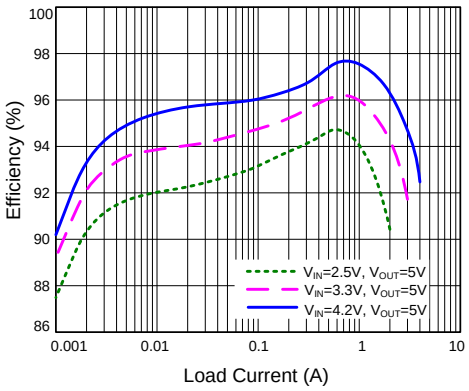
Note 2: θJA is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

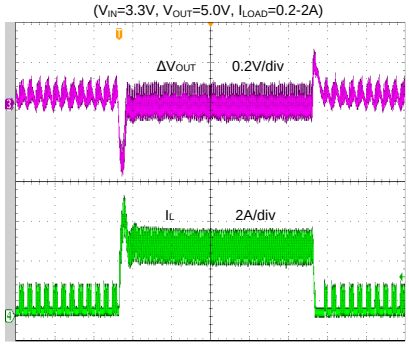
(T_A = 25°C, V_{IN} = 3.0V, V_{OUT} = 4.2V, unless otherwise specified.)

Efficiency, PFM mode



Load Transient

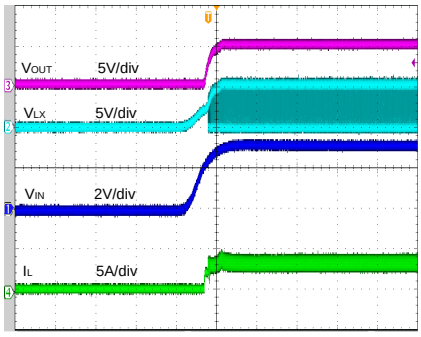
(V_{IN}=3.3V, V_{OUT}=5.0V, I_{LOAD}=0.2-2A)



Time (100μs/div)

Startup from V_{IN}

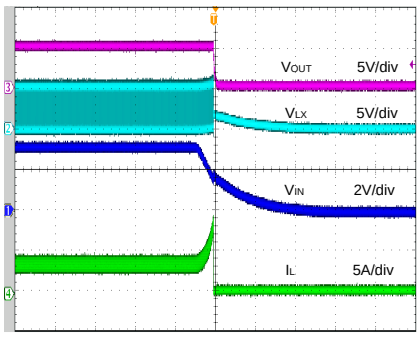
(V_{IN}=3.3V, V_{OUT}=5.0V, I_{Load}=2.0A)



Time (800μs/div)

Shutdown from V_{IN}

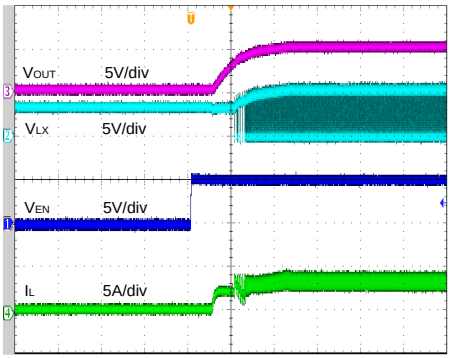
(V_{IN}=3.3V, V_{OUT}=5.0V, I_{Load}=2.0A)



Time (4ms/div)

Startup from Enable

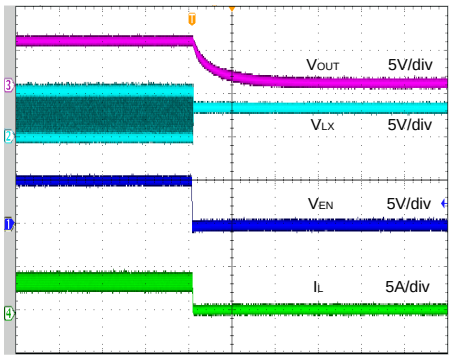
(V_{IN}=3.3V, V_{OUT}=5.0V, I_{Load}=2.0A)



Time (200μs/div)

Shutdown from Enable

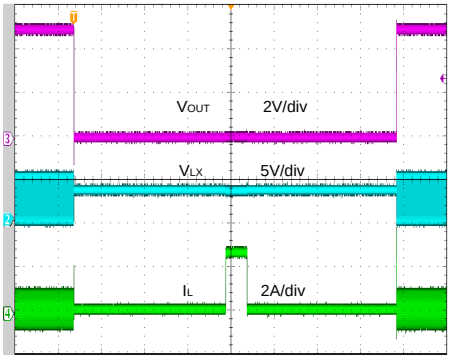
(V_{IN}=3.3V, V_{OUT}=5.0V, I_{Load}=2.0A)



Time (200μs/div)

Hard Short Protection

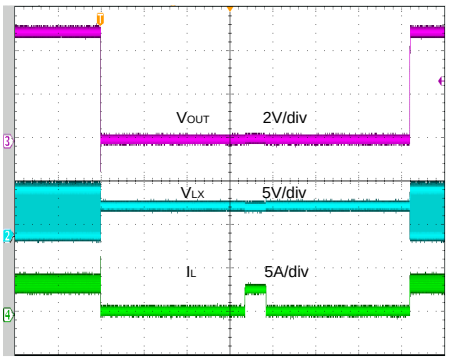
(V_{IN}=3.3V, V_{OUT}=5.0V, Null Load to Short)



Time (20ms/div)

Hard Short Protection

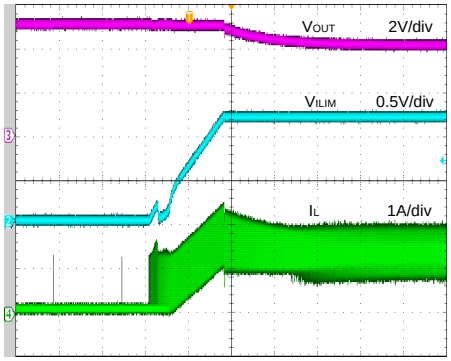
(V_{IN}=3.3V, V_{OUT}=5.0V, 2A to Short)



Time (20ms/div)

Adjustable Current Limit

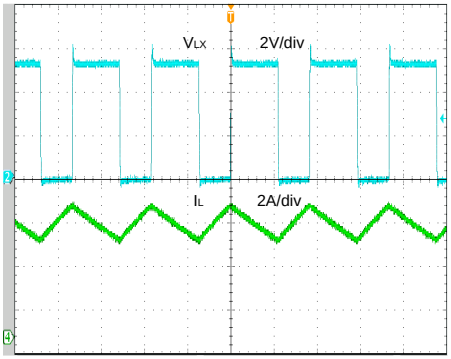
(V_{IN}=3.3V, V_{OUT}=5.0V, I_{LIMIT}=1A)



Time (10ms/div)

Steady State

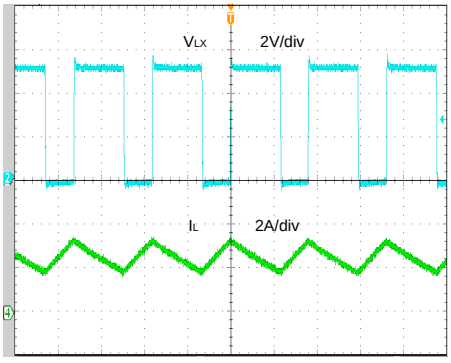
(V_{IN}=3.3V, V_{OUT}=5.0V, I_{LOAD}=2.0A)



Time (1μs/div)

Steady State

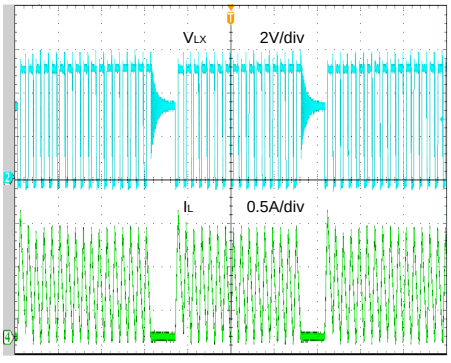
(V_{IN}=3.3V, V_{OUT}=5.0V, I_{LOAD}=1.0A)



Time (1μs/div)

Steady State

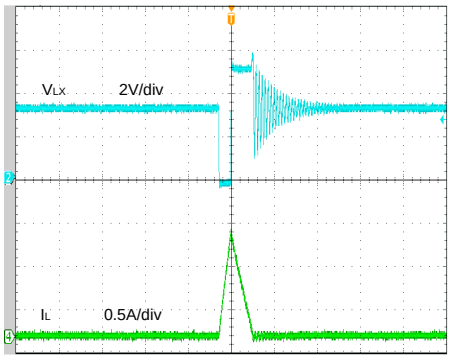
(V_{IN}=3.3V, V_{OUT}=5.0V, I_{LOAD}=0.3A)



Time (10μs/div)

Steady State

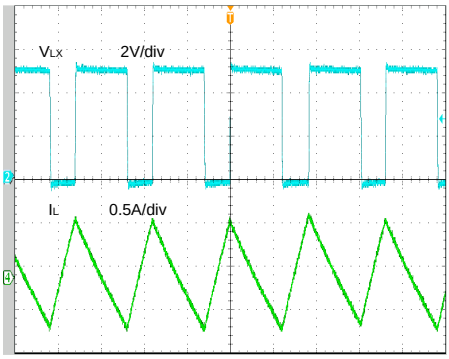
(V_{IN}=3.3V, V_{OUT}=5.0V, Null Load, PFM mode)



Time (2μs/div)

Steady State

(V_{IN}=3.3V, V_{OUT}=5.0V, Null Load, FCCM mode)



Time (1μs/div)

Application Information

Operation

The SY20496 uses constant frequency peak current control to regulate the output voltage. A PWM cycle initiated by the internal clock turns the bottom FET on, and the bottom FET remains on until its current reaches the value set by V_{COMP}. When the PWM signal goes low, the bottom FET turns off and remains off until the next cycle starts. When V_{FB} drops below the internal reference voltage (V_{REF}), V_{COMP} will be driven higher, so the switch peak current becomes higher and the IC delivers more energy to the output. Conversely, when V_{FB} rises above V_{REF}, the V_{COMP} will be driven lower and the switch peak current output drops. See Figure 3 for details.

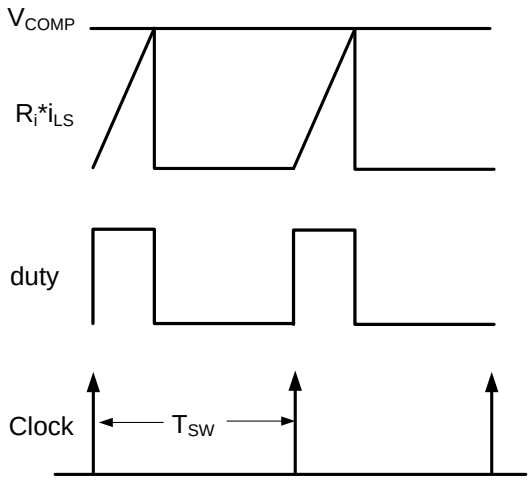


Figure 3. Constant-On-Time Peak-Current Control

The following paragraphs describe the selection process for the input capacitor C_{IN}, the output capacitor C_{OUT}, the inductor L, and the feedback resistor-divider (R_H and R_L).

Feedback Resistor-Divider R_H and R_L:

Choose RH and RL in the feedback resistor-divider to configure the output voltage. A value between 10kΩ and 1MΩ is recommended for both resistors to minimize power consumption under light loads. If V_{OUT} = 5.0V and R_H is chosen to be 470kΩ, then R_L can be calculated as 148.4kΩ using the following formula:

$$R_2 = \frac{1.2V}{V_{OUT} - 1.2V} R_1$$

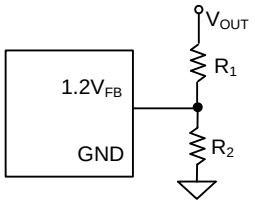


Figure 4. Feedback Resistor-Divider

Input Capacitor C_{IN}

Input filter capacitors reduce the ripple voltage on the input, filter the switched current drawn from the input supply, and reduce potential EMI. When selecting an input capacitor, be sure to select a voltage rating at least 20% greater than the maximum voltage of the input supply and a temperature rating higher than the system requirements. X5R or X7R series ceramic capacitors are most often selected due to their small size, low cost, surge-current capability, and high RMS current ratings over a wide temperature and voltage range. However, systems that are powered by a wall adapter or other long and therefore inductive cabling may be susceptible to significant inductive ringing at the input to the device. In these cases, consider adding some bulk capacitance like electrolytic, tantalum, or polymer type capacitors. Using a combination of bulk capacitors (to reduce overshoot or ringing) in parallel with ceramic capacitors (to meet the RMS current requirements) is helpful in these cases.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

The ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2\sqrt{3} \times L\, f_{SW} \times V_{OUT}}$$

For the best performance, select a typical X5R or better grade ceramic capacitor with a 6.3V rating and at least 22µF capacitance.

Li-Ion Battery Hot Plug Consideration

In the mass production stage, the Li-Ion battery will always hot plug between the IN and GND pins. The hot plug may lead to large voltage spikes, or even to IC EOS failure. To avoid this potential risk, place one 22µF ceramic capacitor in series with a 0.1Ω resistor to absorb the input voltage spike. With this solution, the voltage spike can be reduced from 6.12V to 5.2V. See Figures 5, 6, and 7 for more details.

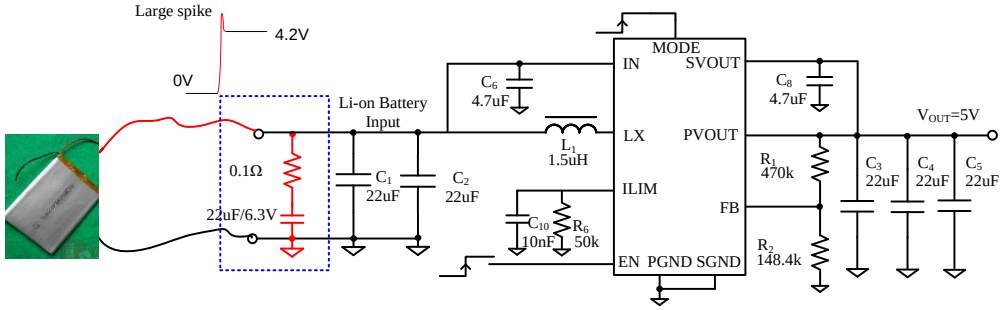


Figure 5. Voltage Spike Suppression

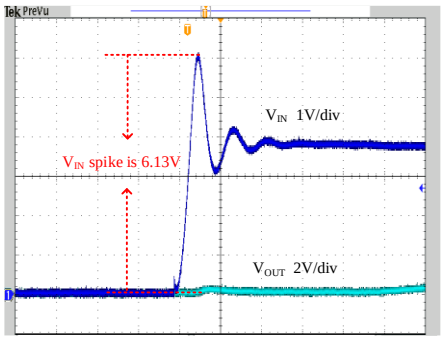


Figure 6. Voltage Spike without Suppression

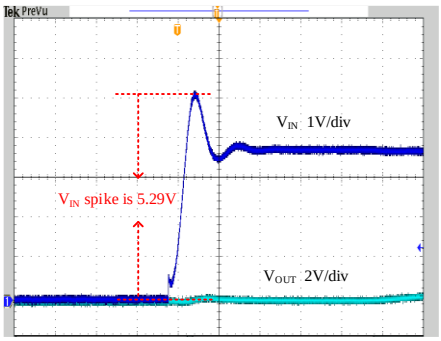


Figure 7. Voltage Spike with Suppression

Boost Inductor L

Consider the following when choosing this inductor:

- Choose the inductance to provide a ripple current that is approximately 40% of the maximum output current. The recommended inductance is calculated as:

$$L = \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \frac{(V_{OUT} - V_{IN})}{f_{SW} \times I_{OUT,MAX} \times 40\%}$$

  where f_{SW} is the switching frequency and I_{OUT_MAX} is the maximum load current.

  The SY20496 has high tolerance for ripple-current amplitude variation. As a result, the final choice of inductance can vary slightly from the calculated value with no significant performance impact.

- The saturation-current rating of the inductor must be selected to be greater than the peak inductor current under full-load conditions.

$$I_{SAT,MIN} > \left(\frac{V_{OUT}}{V_{IN}}\right) \times I_{OUT,MAX} + \frac{V_{IN}(V_{OUT} - V_{IN})}{2 \times f_{SW} \times L \times V_{OUT}}$$

- The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. Choose an inductor with DCR greater than 50mΩ to achieve a good overall efficiency.

Output Capacitor C_{OUT}

For applications where the design must meet stringent ripple requirements, the following considerations must be followed:

The output-voltage ripple at the switching frequency is caused by the inductor-current ripple (ΔI_L) on the output capacitor's ESR (ESR ripple), as well as the stored charge (capacitive ripple). When calculating total ripple, both should be considered.

$$V_{RIPPLE,\ ESR1} = I_{LPEAK} \times ESR$$

$$V_{RIPPLE,\ ESR2} = I_{LVALLEY} \times ESR$$

$$V_{RIPPLE,CAP} = \frac{I_{OUT} \times (1\text{-}D)}{C_{OUT} \times f_{SW}}$$

The capacitive ripple might be higher because the effective capacitance for ceramic capacitors decreases with the voltage across the terminals. The voltage derating is usually included as a chart in the capacitor datasheet, and the ripple can be recalculated after taking the target output voltage into account.

Inductor vs. Output Capacitor

Select the output capacitor C_{OUT} to handle the output ripple requirements. Both steady-state ripple and transient requirements must be taken into consideration when selecting C_{OUT}. For the best performance, use an X5R or better grade ceramic capacitor with a 10V rating and at least the capacitance shown in Table 1 to decouple the high-frequency current. Care should be taken to minimize the loop area formed by C_{OUT} and the OUT/GND pins. In some cases, adding a tantalum capacitor with a 16V rating and at least 100µF capacitance can be used to reduce the number of ceramic out capacitors.

All continuous-mode boost converters have a right-half-plane zero (RHP zero) due to the inductor being removed from the output during charging. In a converter with current-mode control, an inner current feedback loop allows the switch, inductor, and modulator to be lumped together into a small signal variable current source, as shown in Figure 8.

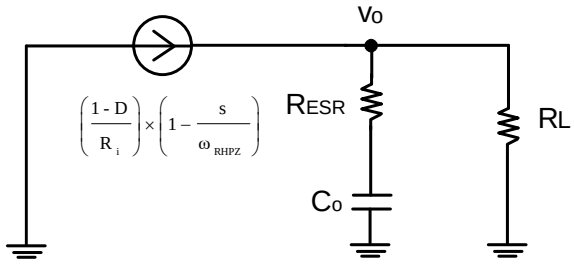


Figure 8. Current Feedback Loop

The power stage approximate transfer function is:

$$G_c(s) = \frac{(1-D) \times R_L}{R_i} \times \frac{\left(1 + \frac{s}{\omega_{ESR}}\right)\left(1 - \frac{s}{\omega_{RHPZ}}\right)}{1 + \frac{s}{\omega_p}}$$

where

$$\omega_{ESR} = \frac{1}{R_{ESR} C_O}$$

$$\omega_P = \frac{1}{(R_{ESR} + R_L) \times C_O}$$

$$\omega_{RHPZ} = \frac{R_L}{L} \times \left(\frac{V_{IN}}{V_{OUT}} \right)^2$$

As Equation 6 shows, the transfer function for boost conversion with current-mode control consists of one ESR zero, one RHP zero, and one pole. The RHP zero provides a 20dB/decade gain increase and 90 degrees of phase drop. Therefore, the bandwidth of the boost converter must be lower than f_{RHPZ}.

As shown in Equation 9, the RHP zero depends on R_L, L, and the duty cycle. Larger inductors lead to lower f_{RHPZ}, so bandwidth should be designed lower than f_{RHPZ}.

Some low-profile applications may benefit from using the ceramic capacitor solution, and some low-cost applications may benefit from using an electrolytic capacitor to reduce BOM cost.

Table 1. Inductance vs. Output Capacitor Selection

Inductance		Low-Profile Capacitor Application		Low-Cost Capacitor Application
Part Number	L(μH)	Part Number	C_{OUT} (μF)	C_{OUT} (μF)
SPM6530T-1R0M	1.0	C3216X5R1A226M	22μF/10V×2pcs	22μF/10V+100μF(E-cap)
SPM6530T-1R5M	1.5	C3216X5R1A226M	22μF/10V×3pcs	22μF/10V+100μF(E-cap)
SPM6530T-2R2M	2.2	C3216X5R1A226M	22μF/10V×4pcs	22μF/10V+100μF(E-cap)

Enable Operation

Pulling the EN pin high (>1.2V) enables normal operation. Pulling the EN pin low (<0.4V) will shut down the device. During shutdown mode, the SY20496 shutdown current drops to less than 1μA.

Mode Operation

When the MODE pin is pulled low (<0.4V), the SY20496 will operate in PFM (Pulse Frequency Modulation) mode to improve light-load efficiency. When the MODE pin is pulled high (> 1.2V), the SY20496 will work in FCCM (Forced Continuous Conduction) mode to improve output ripple.

Programmable Output Current-Limit Function

The SY20496 provides a programmable output current limit to protect the system from output overcurrent. The output current limit function can be programmed by an external resistor. This resistor is set by the calculation I_{LIM}(A) = 100k/R_{SET}(Ω). The minimum output current-limit is 0.8A and the current-limit accuracy is ±10%.

Adding a RC network placed in parallel with the I_{LIM} pin is recommended. The minimum allowed capacitor value of 10nF guarantees the stability of the output current-limit program loop.

Hard-Short Protection

When V_{OUT} is lower than V_{IN}, the IC will enter hard-short protection mode. In this mode, the PFET will turn off for 63ms to reduce the power dissipation, and then try to operate as a current source to charge the output capacitor for a duration of 9ms, to restart the operation, as shown in Figure 9.

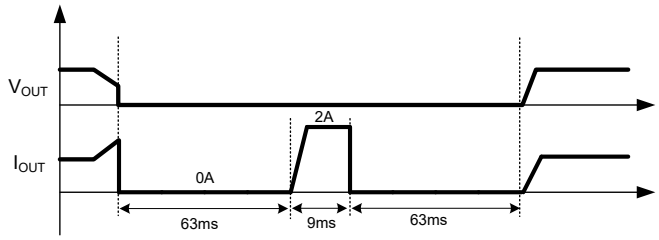


Figure 9. Hard-Short Protection

Overvoltage Protection

The SY20496 provides output overvoltage protection. If the output voltage exceeds V_{OVP} (typ. 6V), the device stops switching, and the main switch is turned off. When the output voltage returns to the normal operating range, the device resumes operation.

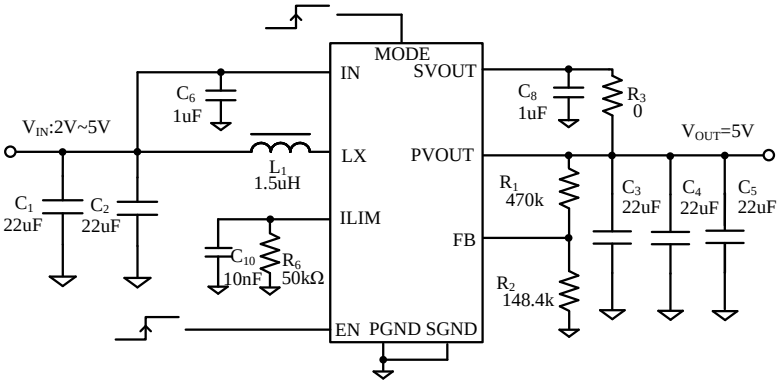
Overcurrent Protection

The SY20496 provides cycle-by-cycle overcurrent protection and turns off the main power MOSFET once the inductor current reaches the current-limit threshold. During overcurrent protection, the output voltage drops as a function of the load. As soon as the overload condition is removed, the converter resumes normal operation.

Thermal Protection

The SY20496 includes overtemperature protection circuitry to prevent overheating due to excessive power dissipation. This will shut down the device when the junction temperature exceeds 150°C. When the junction temperature cools down by approximately 20°C, the device will resume normal operation after a complete soft-start cycle. For continuous operation, provide adequate cooling so that the junction temperature does not exceed the thermal protection threshold.

Typical Application Schematic



Design Specifications

Input Voltage (V)	Output Voltage (V)	Output Current Limit (A)
2-5	5	2

BOM List

Reference Designator	Description	Part Number	Manufacturer
L1	1.5μH/10A	SPM6530T-1R5M	TDK
C1 ,C2	22μF/6.3V, 0805, X5R	C2012X5R1A106M	TDK
C3, C4 , C5	22μF/10V, 1206, X5R	C3216X5R1A226M	TDK
C6 , C8	1μF/16V, 0603, X5R	C1608X5R1C105M	TDK
C10	10nF/50V, 0603, X5R	C1608X5R1H103K	TDK
C7	NC		TDK
R_H	470kΩ, 0603, 1%		
R_L	150kΩ, 0603, 1%		

Recommended Components for Typical Applications

V_{OUT}(V)	R_L(kΩ)	R_H(kΩ)	L(μH)	C_{OUT}
5	470	150	1.5	3×22μF/10V/X5R,1206
3.3	510	300	1.5	3×22μF/10V/X5R,1206

Recommended PCB Layout

Follow these PCB layout guidelines for optimal performance and thermal dissipation:

- Place the following components as close as possible to the IC: C_{IN}, L, R_H, and R_L.
- To achieve the best thermal and noise performance, maximize the PCB copper area connecting to the GND pin. If board space allows, using a large copper pour connected to GND ground plane is recommended.
- C_{OUT} must be close to the PVOUT and PGND pins. Minimize the loop area formed by C_{IN} and GND.
- To minimize the output loop area, route the LX trace on the bottom or middle layer through a via.
- SVOUT is the power supply pin for the internal control circuit. Do not connect to the POUT pin directly. A 4.7μF ceramic capacitor is strongly recommended to decouple the SVOUT pin to the SGND pin. Use a copper trace to connect the SOUT pin to the output capacitor side.
- Minimize the PCB copper area associated with the LX pin to reduce EMI emissions.
- To avoid crosstalk, R_H, R_L, and the trace connecting to the FB pin must not be adjacent to the LX net on the PCB layout.

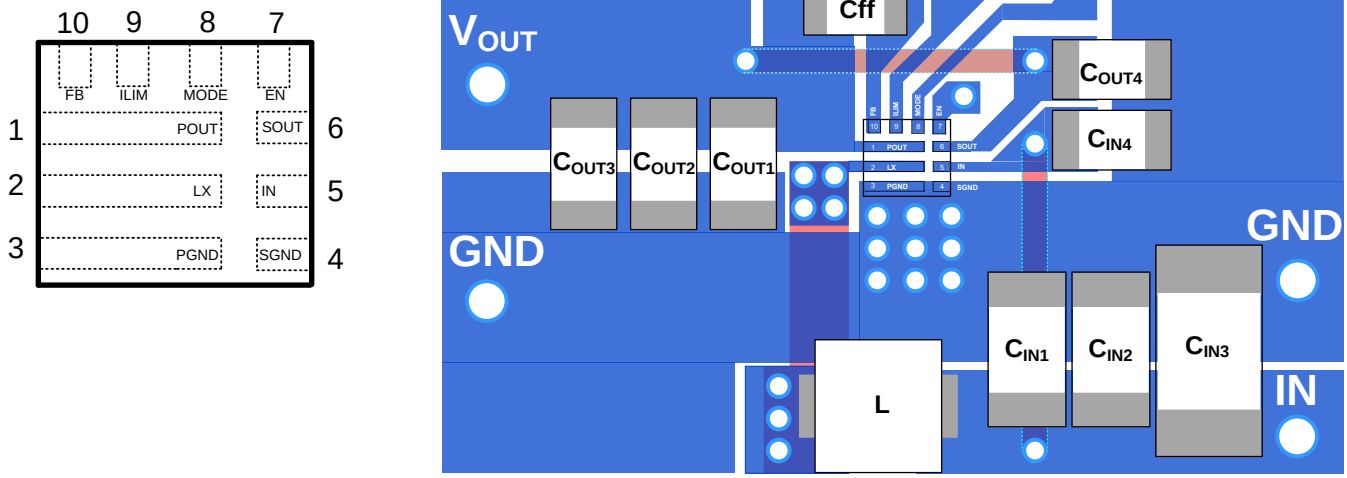
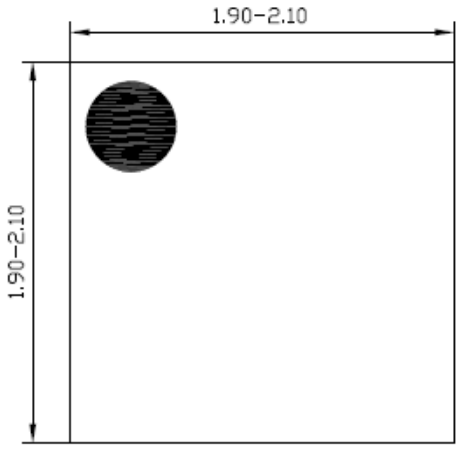
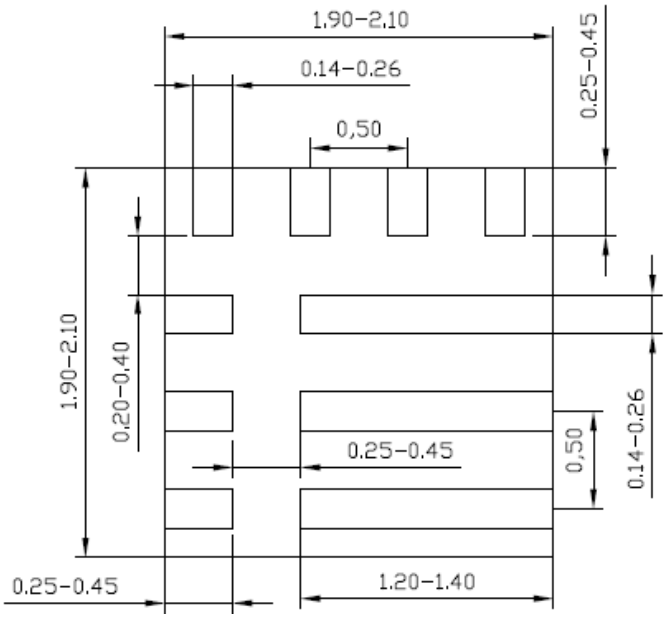


Figure 8. Suggested PCB Layout

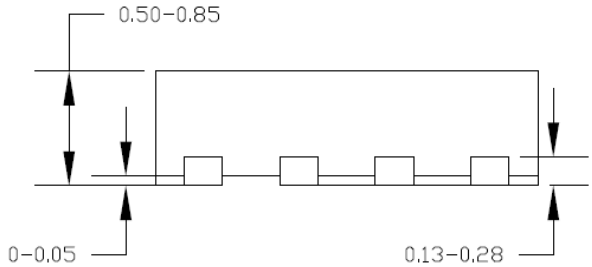
QFN2x2-10 Package Outline Drawing



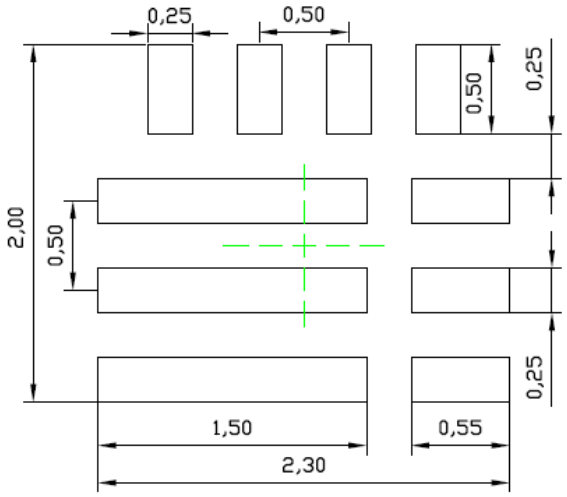
Top view



Side view A



Side view B

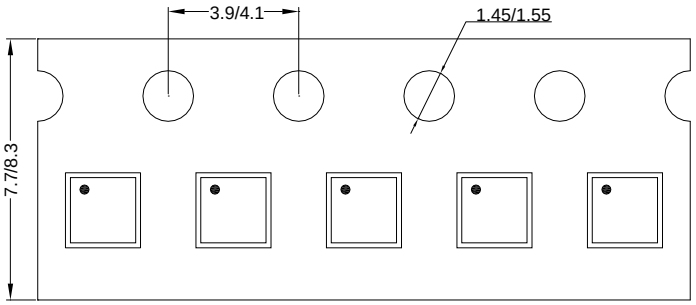


Recommended pad layout (reference only)

Note: *All dimensions are in millimeters and exclude mold flash and metal burr.*

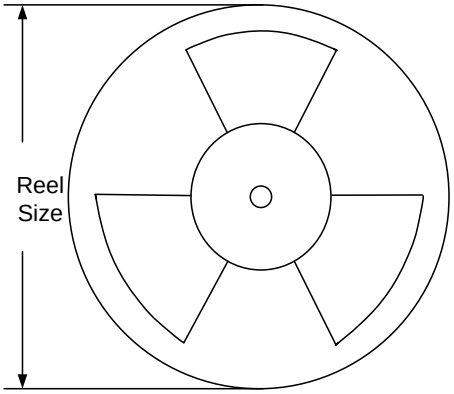
Taping and Reel Specification

QFN2x2 taping orientation



Feeding direction →

Carrier tape and reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel (pcs)
QFN2x2	8	4	7"	400	160	3000

Others: NA

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