SY21305A

High Efficiency 15A Step-Up Regulator with Accurate Output Current Limit

General Description

The SY21305A high efficiency synchronous step-up regulator operates using adaptive constant off-time and current mode control, and can deliver 15A current over a wide input voltage range from 3V to 16V. It integrates switches with low $R_{DS(ON)}$ to minimize conduction loss.

The SY21305A features cycle-by-cycle peak current limit, output short-circuit protection, and true shutdown. It also provides enable control and power-good indicator for system sequence control. The programmable pseudoconstant frequency reduces output voltage ripple and permits smaller external capacitors and inductor.

The SY21305A is available in a compact QFN4×4-18 package.

Features

- 3V to 16V Input Voltage Range
- Up to 15A Output Current
- Programmable Output Current Limit
- Low $R_{DS(ON)}$ for Internal N-Channel MOSFET: 9mΩ Main, 12mΩ Rectifier, 12mΩ Disconnection FET
- Programmable Pseudoconstant Frequency
- Enable Control
- Input Voltage UVLO
- Output Overvoltage Protection
- Overtemperature Protection
- Output Short-Circuit Protection
- True Shutdown Function
- RoHS-Compliant and Halogen-Free
- Compact QFN4mm×4mm-18 Package

Applications

- Power Bank
- High Power Application

Typical Application

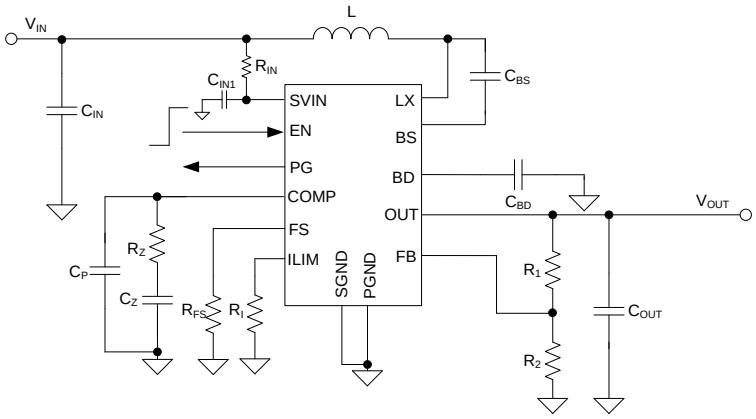


Figure 1. Typical Application Circuit

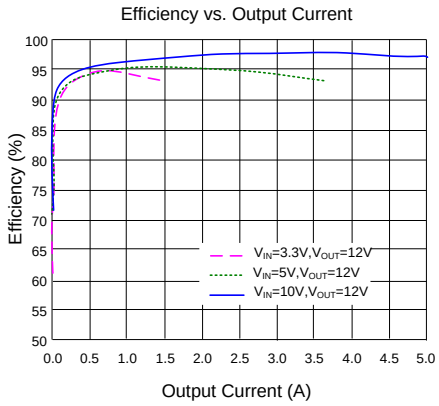


Figure 2. Efficiency vs. Output Current

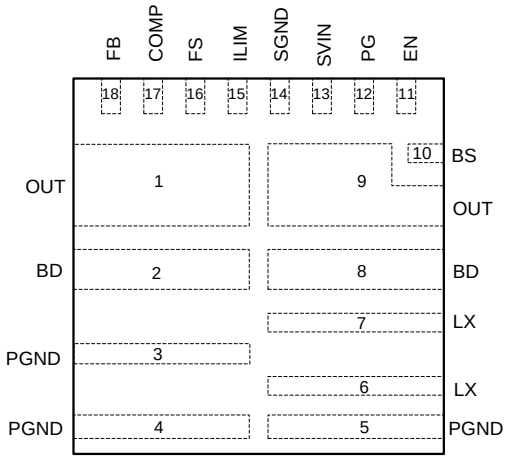
Ordering Information

Ordering Part Number	Package type	Top Mark
SY21305ARDC	QFN4×4-18 RoHS-Compliant and Halogen-Free	**BET*xyz***

Device code: BET

x = year code, y = week code, z = lot number code

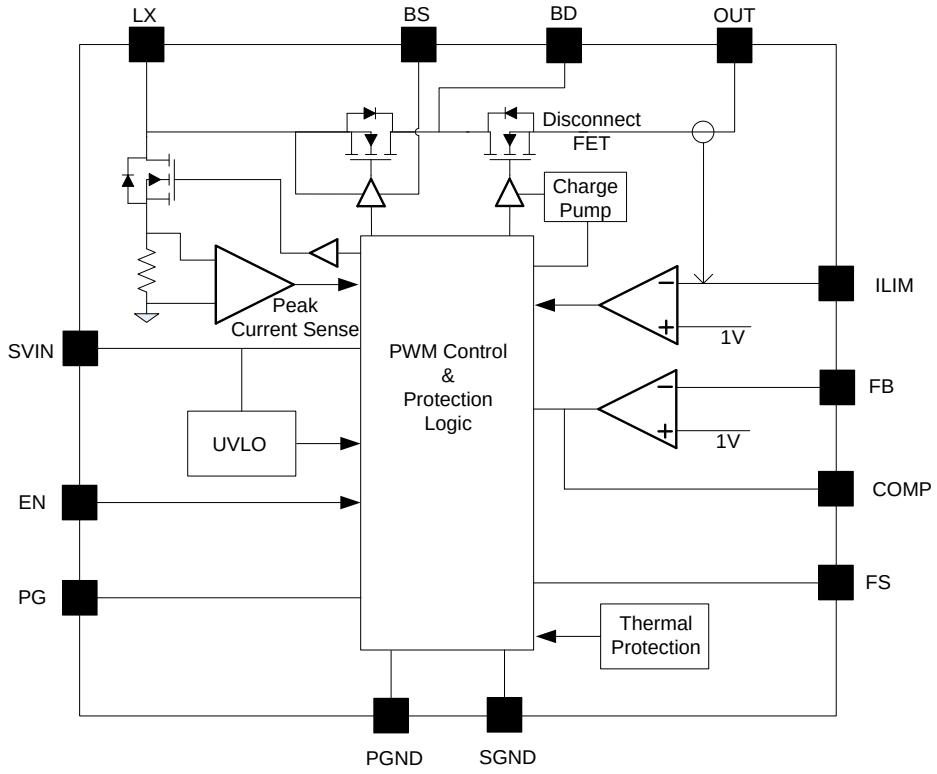
Pinout (top view)



Pin Description

Pin Number	Pin Name	Pin Description
1,9	OUT	Boost converter output pin.
2,8	BD	Connect to the drain of the internal disconnect FET with at least a 4.7μF ceramic capacitor to PGND.
3,4,5	PGND	Power ground pin.
6,7	LX	Inductor node. Connect an inductor from the power input to the LX pin.
10	BS	Bootstrap pin. Supply for rectifier FET's gate driver. Connect a 0.1μF ceramic capacitor between the BS pin and the LX pin.
11	EN	Enable control. Pull high to enable the regulator; pull low to disable the regulator. Do not leave floating.
12	PG	Power-good indicator. Open-drain output pulled low when the output is less than 90% of regulation voltage, high impendence otherwise.
13	SVIN	Device power supply pin. Decouple this pin to the SGND pin with a 2.2μF ceramic capacitor.
14	SGND	Signal ground pin.
15	ILIM	Output current limit program pin. Connect a resistor R_{LIM} from this pin to SGND to program the output current limitation threshold. $I_{LIM}(A) = 30(V)/ R_{LIM}(k\Omega)$
16	FS	Switching frequency setting pin. Connect a resistor from this pin to ground to program the switching frequency. $f_{SW}(kHz) = 1.4\times10^6/R_{FS}(\Omega)^{0.645}$
17	COMP	Loop compensation pin. Connect an RC network between this pin and ground to stabilize the control loop.
18	FB	Feedback pin. Connect to the center of the resistor voltage divider to program the output voltage. $V_{OUT} = 1V\times(R_1/R_2+1)$

Block Diagram



Absolute Maximum Ratings

Parameter (Note1)	Min	Max	Unit
SVIN, LX, EN, ILIM, OUT, BD, BS, FS, PG, COMP	-0.3	18	V
FB, BS-LX	-0.3	4	
LX, 10ns Duration	-3.5	260	
Lead Temperature (Soldering, 10 sec.)		260	°C
Junction Temperature, Operating	-40	150	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	30	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	3.2	
P_D Power Dissipation T_A = 25°C	3.4	W

Recommended Operating Conditions

Parameter (Note3)	Min	Max	Unit
SVIN	3	16	V
Junction Temperature, Operating	-40	125	°C
Ambient Temperature	-40	85	

Electrical Characteristics

(V_{IN} = 5V, V_{OUT} = 12V, I_{OUT} = 100mA, T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		3		16	V
Output Voltage Range	V_{OUT}		V_{IN}×1.1		16	V
Output OVP Threshold	V_{FB_OVP}	V_{FB} Rising	110%	115%	120%	V_{REF}
Quiescent Current	I_Q	V_{OUT} = 13V			230	μA
Shutdown Current	I_{SHDN}	EN = 0			5	μA
FB Leakage Current	I_{FB}		-50		50	nA
Main N-FET R_{ON}	$R_{DS(ON)\_M}$			9		mΩ
Rectified N-FET R_{ON}	$R_{DS(ON)\_R}$			12		mΩ
Disconnect N-FET R_{ON}	$R_{DS(ON)\_D}$			12		mΩ
Main N-FET Current Limit	$I_{LIM,PEAK}$		15		20	A
Switching Frequency	f_{SW}	R_{FS} = 390kΩ		345		kHz
Switching Frequency Programmable Range			250		1000	kHz
Feedback Reference Voltage	V_{REF}		0.985	1	1.015	V
IN UVLO Rising Threshold	$V_{IN,UVLO}$				2.85	V
UVLO Hysteresis	$V_{HYS,UVLO}$			0.2		V
EN Rising Threshold	V_{ENH}		1.5			V
EN Falling Threshold	V_{ENL}				0.4	V
Output Current Limit	I_{LIM}	R_{LIM} = 15kΩ		1		A
Output Current Limit Programmable Range	$I_{LIM,OUT}$	V_{OUT} <= 5V	1		5	A
		V_{OUT} > 5V	1		4	A
Minimum On-Time	$t_{ON,MIN}$			100		ns
Minimum Off-Time	$t_{OFF,MIN}$			120		ns
Error Amplifier Transconductance	g_m			100		μS
Current Sense Gain	R_i			75		mΩ
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			20		°C

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

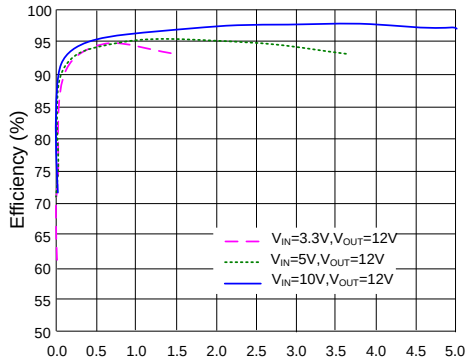
Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a two-layer Silergy Evaluation Board.

Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

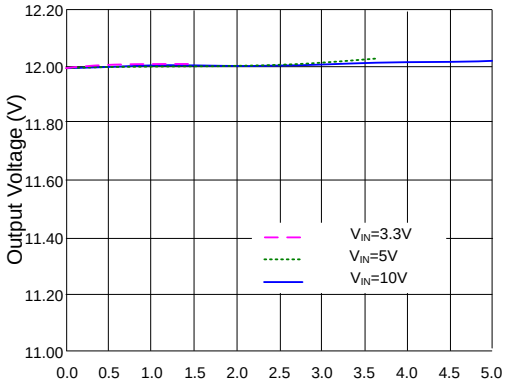
(T_A= 25ºC, V_{OUT} = 12V, f_{SW}=350kHz, L = 2.2μH, C_{OUT}= 44μF, unless otherwise specified.)

Efficiency vs. Output Current



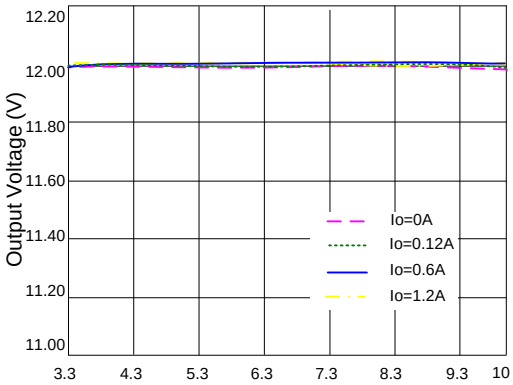
Output Current (A)

Load Regulation



Output Current (A)

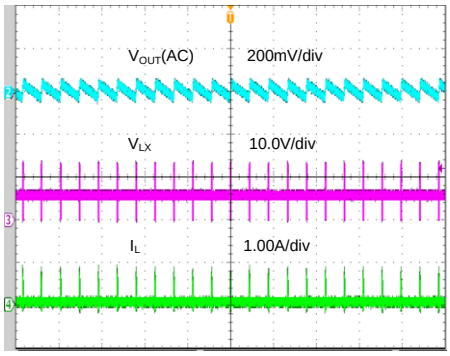
Line Regulation



Input Voltage (V)

Output Ripple

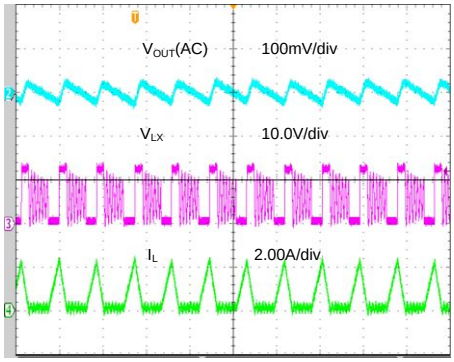
(V_{IN}=5V, V_{OUT}=12V, I_{OUT}=0A)



Time (10ms/div)

Output Ripple

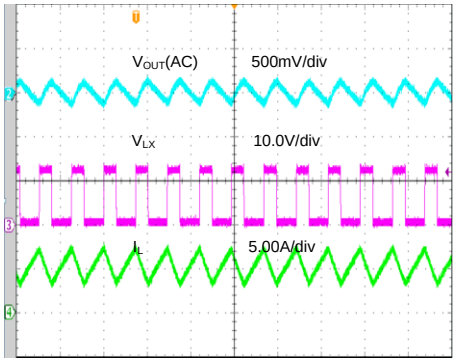
(V_{IN}=5V, V_{OUT}=12V, I_{OUT}=0.2A)



Time (4.00μs/div)

Output Ripple

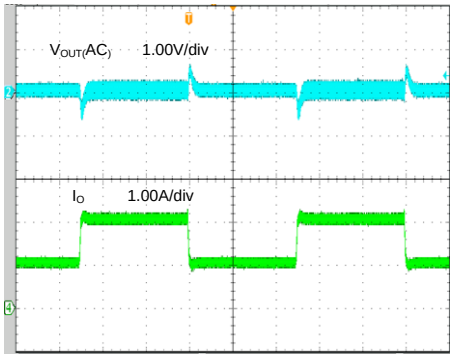
(V_{IN}=5V, V_{OUT}=12V, I_{OUT}=2A)



Time (4.00μs/div)

Load Transient

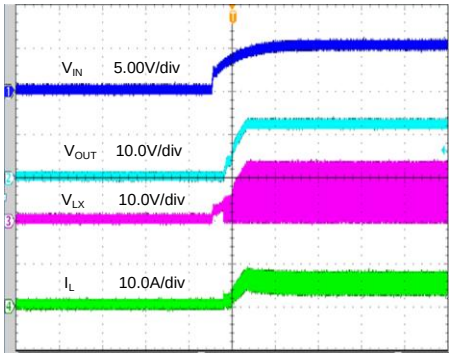
(V_{IN}=5V, V_{OUT}=12V, I_{OUT}=1-2A)



Time (400μs/div)

Startup from V_{IN}

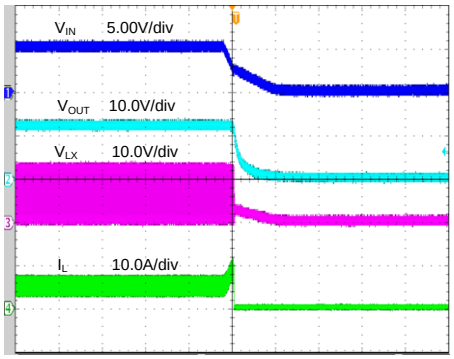
(V_{IN}=5V, V_{OUT}=12V, I_{OUT}=2A)



Time (4ms/div)

Shutdown from V_{IN}

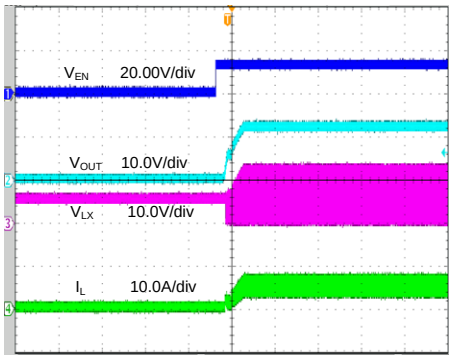
(V_{IN}=5V, V_{OUT}=12V, I_{OUT}=2A)



Time (800μs/div)

Startup from Enable

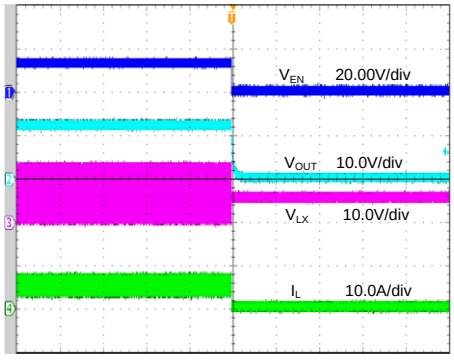
(V_{IN}=5V, V_{OUT}=12V, I_{OUT}=2A)



Time (4ms/div)

Shutdown from Enable

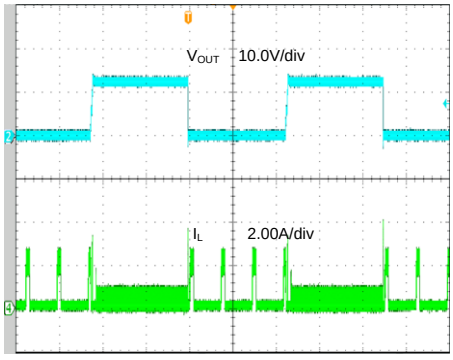
(V_{IN}=5V, V_{OUT}=12V, I_{OUT}=2A)



Time (4ms/div)

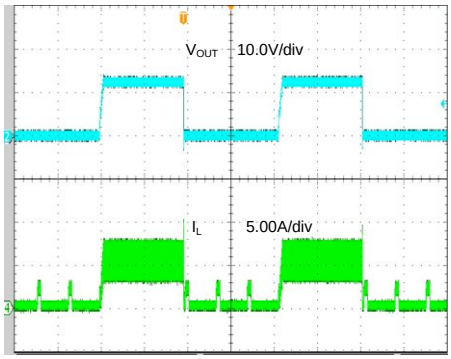
Short Circuit Protection

(V_{IN}=5V, V_{OUT}=12V, I_{OUT}=0A)



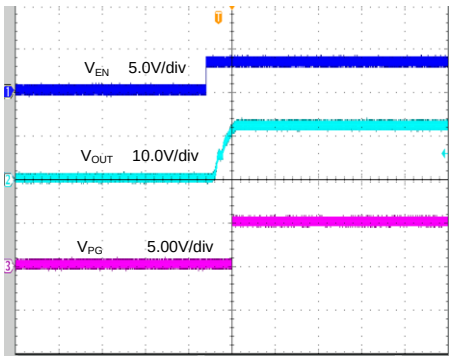
Time (20ms/div)

Short Circuit Protection
(V_{IN}=5V, V_{OUT}=12V, I_{OUT}=0A)



Time (20ms/div)

PG Signal
(V_{IN}=5V, V_{OUT}=12V, I_{OUT}=2A)



Time (20ms/div)

Detailed Description

The SY21305A high efficiency synchronous step-up regulator operates using adaptive constant off-time and current mode control, and can deliver 15A current over a wide input voltage range from 4.5V to 30V. It integrates switches with low $R_{DS(ON)}$ to minimize conduction loss.

The SY21305A features cycle-by-cycle peak current limit, output short-circuit protection, and true shutdown. It also provides enable control and power-good indicator for system sequence control. The programmable pseudoconstant frequency reduces output voltage ripple and permits smaller external capacitors and inductor.

Enable Operation

Driving the EN pin high (>1.5V) enables normal operation. Driving the EN pin low (<0.4V) will shut down the device. During shutdown mode, the SY21305A shutdown current drops to less than 5μA.

Switching Frequency

The switching frequency of the SY21305A in CCM (continuous conduction mode) can be programmed by adjusting an external resistor R_{FS} connected to FS pin:

$$f_{SW}(kHz) = 1.4 \times 10^6 / R_{FS}(\Omega)^{0.645}$$

Under light load conditions, the SY21305A linearly folds back the frequency, to maintain high efficiency.

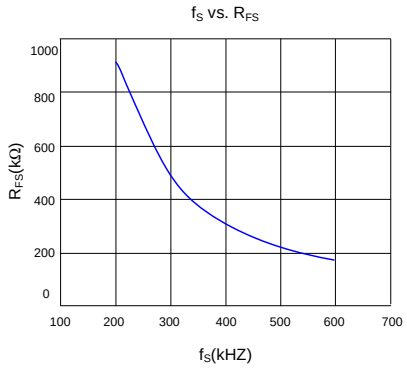


Figure 3. f_{SW} vs R_{FS}

Power-Good Indicator

PG is an open-drain output pin. This pin will be pulled to ground if the output voltage is lower than 90% of the regulation voltage. Otherwise, this pin will go to a high impedance state.

Loop Compensation

The SY21305A incorporates constant off-time current mode control with two feedback loops:

- The inner loop (current loop) does not require any external compensation component.
- The outer loop (voltage loop) is compensated with external components.

In most applications, a Type 2 or Type 2a compensation network, as shown in Figure 3, can be used to stabilize the voltage loop. Type 2 is most widely used, and it works fine for power stages lagging down to -90˚ and where the boost brought by the output capacitor ESR must be canceled. Type 2a is used where the output capacitor ESR effect can be neglected.

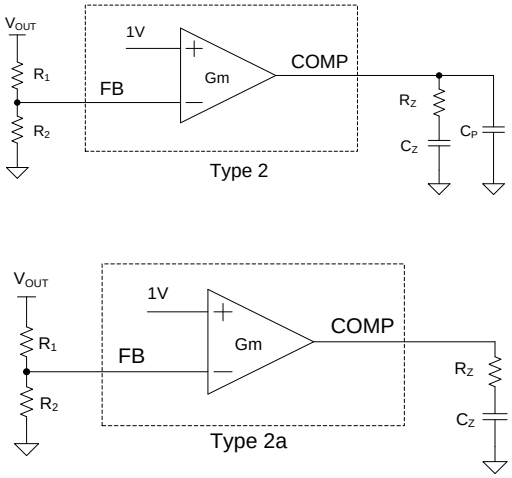


Figure 4. Compensation networks

Follow the steps below to calculate the value of external components for voltage loop compensation.

1. Select the crossover frequency f_C of the closed loop. For the tradeoff between stability and transient response of the system, the recommended crossover frequency is the minimum value of 1/5 of the right-half-plane zero (f_{RHPZ}) and 1/10 of the switching frequency. The system has faster response at higher crossover frequency.

$$f_{RHPZ} = \frac{(1 - D_{MAX})^2 \times V_{OUT}}{2\pi \times L \times I_{OUT}}$$

2. Select an R_Z value of the R-C series combination connected to the COMP pin:

$$R_Z = \frac{V_{OUT}}{g_M \times G_{fc} \times V_{REF}}$$

where g_m is the error amplifier transconductance, which is typically 50μS; G_{fc} is the gain of the power stage at crossover frequency.

$$G_{fc} = \frac{1 - D_{MAX}}{2\pi \times f_c \times C_{OUT} \times R_i}$$

where R_i is the current-sense resistance, which is typically 170mΩ.

3. Select a C_Z value of the R-C series combination connected to the COMP pin. The compensation zero decides the phase margin at the crossover frequency.
   Place a compensation zero at or before the dominant pole of R_L and C_O. R_L is the load resistance, which equals V_{OUT}/I_{OUT}.

$$C_Z = \frac{V_{OUT} \times C_{OUT}}{I_{OUT} \times R_Z}$$

4. A high frequency pole is recommended to attenuate the high frequency noise. Place this pole to cancel the ESR zero of C_{OUT}.

$$C_P = \frac{R_{ESR} \times C_O}{R_Z}$$

Fault Protection Modes

Output Current Limit

There are two feedback loops inside the regulator. When the voltage on ILIM pin reaches the 1V threshold, the current feedback loop will take over and regulate the output DC current to the target value.

$$I_{LIM}(A) = 15(V)/ R_{LIM}(k\Omega)$$

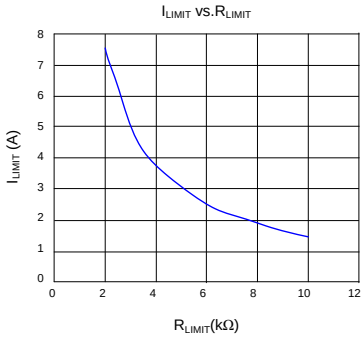


Figure 5. I_{LIMIT} vs R_{LIMIT}

Short-Circuit Protection

The SY21305A features hiccup mode short-circuit protection, which is triggered if the device is operated in current limit continuously and V_{OUT} drops below 2V. The device will shut down for approximately 12ms, and then restart with a complete soft-start cycle that is approximately 2ms. If the short-circuit condition remains, the 'hiccup' cycle of shutdown and restart will continue indefinitely.

Overtemperature Protection (OTP)

The SY21305A includes overtemperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. This will shut down switching operation when the junction temperature exceeds 150°C. Once the junction temperature cools down by approximately 15°C, the device will resume normal operation after a complete soft-start cycle. For continuous operation, provide adequate cooling so that the junction temperature does not exceed the OTP threshold.

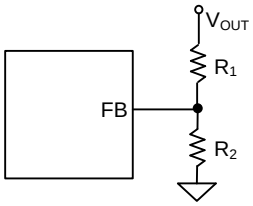
Application Information

The following paragraphs describe the selection process for the feedback resistor divider (R1 and R2), output current limit resistor R_{LIM}, switching frequency program resistor R_{FS}, input capacitor C_{IN}, output capacitors C_{BD} and C_{OUT}, boost inductor L, and external bootstrap capacitor.

Feedback Resistor Divider R1 and R2

Choose R1 and R2 to program the proper output voltage. Choose large resistance values between 10kΩ and 1MΩ for both R1 and R2 to minimize power consumption under light loads. If a value is chosen for R1, then R2 can be calculated as:

$$R2 = \frac{0.6V}{V_{OUT}\text{-}0.6V} R1$$



Input Capacitor C_{IN}

Input filter capacitors reduce the ripple voltage on the input, filter the switched current drawn from the input supply, and reduce potential EMI. When selecting an input capacitor, select a voltage rating at least 20% greater than the maximum voltage of the input supply and a temperature rating higher than the system requirements. X5R series ceramic capacitors are most often selected due to their

small size, low cost, surge-current capability, and high RMS current ratings over a wide temperature and voltage range. However, systems that are powered by a wall adapter or other long and therefore inductive cabling may be susceptible to significant inductive ringing at the input to the device. In these cases, consider adding some bulk capacitance like electrolytic, tantalum, or polymer type capacitors. Using a combination of bulk capacitors (to reduce overshoot or ringing) in parallel with ceramic capacitors (to meet the RMS current requirements) is helpful in these cases.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

$$I_{CIN\_RMS} = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{\sqrt[2]{3} \times L \times f_{SW} \times V_{OUT}}$$

For the best performance, select a typical X5R or better grade low ESR 10μF ceramic capacitor and place it as close as possible to the V_{IN} and PGND pins. Minimize the loop area formed by C_{IN}, V_{IN}, and the PGND pin.

The SVIN capacitor must be placed as close as possible to the SVIN and SGND pins. Minimize the loop area formed by C_{IN} and the SVIN/SGND pins. In this case, a 2μF low ESR ceramic capacitor is recommended.

Boost Output Capacitor C_{BD} and Disconnection FET Output Capacitor C_{OUT}

The boost output capacitor C_{BD} and disconnection FET output capacitor C_{OUT} are selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be considered when selecting these capacitors. For the best performance, it is recommended to use X5R or better grade ceramic capacitors with 25V rating and more than 22μF capacitance for both components.

Boost Inductor L

Consider the following when choosing this inductor:

1) Choose the inductance to provide a ripple current that is approximately 40% of the maximum output current. The recommended inductance is calculated as:

$$L = \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \frac{V_{OUT} - V_{IN}}{f_{SW}\, I_{OUT,MAX} \times 0.4}$$

where f_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY21305A has high tolerance for ripple current amplitude variation. As a result, the final choice of inductance can vary slightly from the calculated value with no significant performance impact.

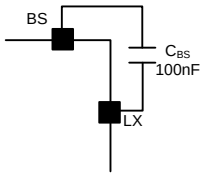
2) The inductor's saturation current rating must be greater than the peak inductor current under full load:

$$I_{SAT,MIN} = \left(\frac{V_{OUT}}{V_{IN}}\right) \times I_{OUT,MAX} + \frac{V_{IN}(V_{OUT} - V_{IN})}{2 \times f_{SW} \times L \times V_{OUT}}$$

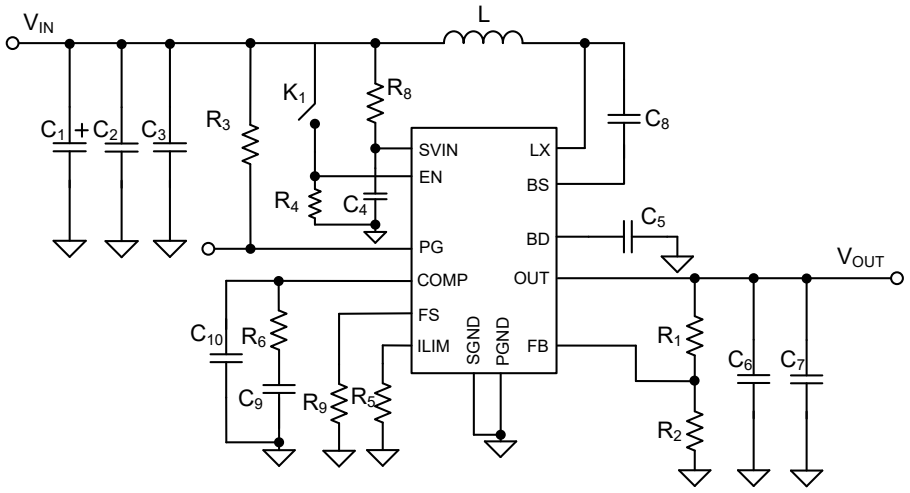
3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. Choose an inductor with DCR less than 10mΩ to achieve good overall efficiency.

External Bootstrap Capacitor

This capacitor provides the gate driver voltage for the internal rectifier. A 100nF low ESR ceramic capacitor connected between the BS pin and the LX pin is recommended.



Application Schematic



Design Specifications

Input Voltage (V)	Output Voltage (V)	Output Current Limit (A)
3-10	12	2

BOM List

Reference Designator	Description	Part Number	Manufacturer
C1	220μF/35V, Electrolytic Cap		
C2,C5,C6,C7	22μF/25V 1206	C3216X5R1E226M	TDK
C4	2.2μF/25V 1206	C3216X7R1E225K	TDK
C8	0.1μF/50V/X7R, 0603	C1608X7R1H104K	TDK
C9	1nF/50V 0603		
C10	22pF/50V 0603		
C3	SPARE		
R1	110k , 1%, 0603		
R2	10k , 1%, 0603		
R3	100k , 1%, 0603		
R4	1M Ω, 1%, 0603		
R5	5.1k , 1%, 0603		
R6	30KΩ, 1%, 0603		
R8	10Ω, 1%, 0603		
R9	390KΩ, 1%, 0603		
L1	Inductor 2.2μH/12A	PIMB104T-2R2MS	CYNTECH
U1	IC	SY21305A	SILERGY

Recommend Components for Typical Applications

V_{OUT}(V)	R1(kΩ)	R2(kΩ)	L(μH)	C_{OUT}
12	110	10	2.2	2×22μF/25V/X7R,1206
9	80.6	10	2.2	2×22μF/25V/X7R,1206
5	80.6	20	1	2×22μF/25V/X7R,1206

Layout Design

To achieve optimal design, follow these PCB layout considerations:

- Place C_{IN}, C_{BD}, C_{OUT}, L, R1, and R2 close to the IC
- To achieve the best thermal and noise performance, maximize the PCB copper area connecting to the GND pin. A ground plane is highly recommended if board space allows.
- C_{IN} must be close to pins SVIN and SGND. Minimize the loop area formed by C_{BD}, LX, and PGND.
- To reduce switching noise, minimize the PCB copper area connected to the LX pin.
- In order to reduce crosstalk, R1, R2, and the trace connected to the FB pin must not be adjacent to the LX net on the PCB layout.
- If the system chip interfacing with the EN pin has a high impedance state during shutdown mode, and the SVIN pin is connected directly to a power source such as a Li-ion battery, add a 1MΩ pulldown resistor between the EN and GND pins to prevent noise from falsely triggering the regulator during shutdown mode.

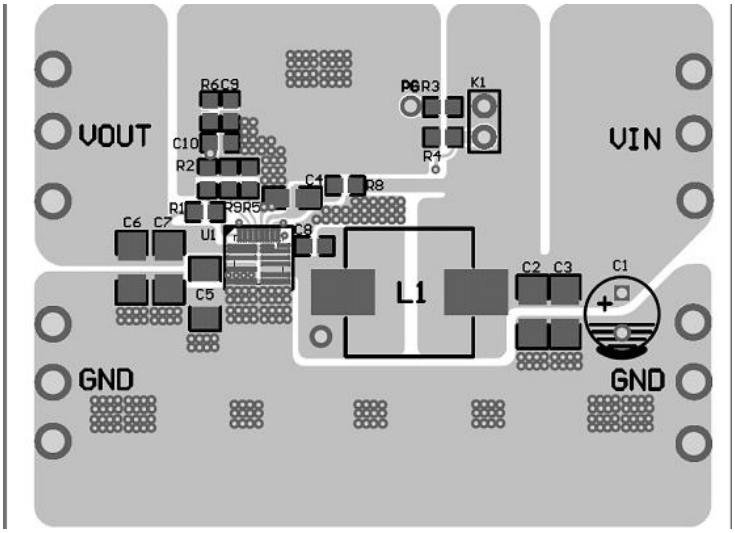
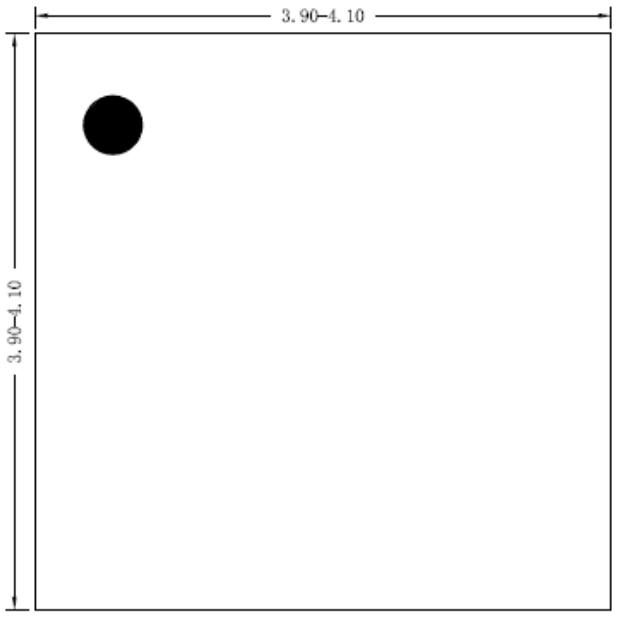
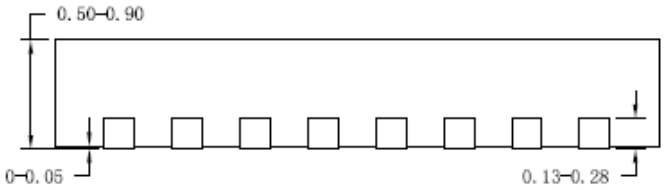


Figure 6. Suggested PCB Layout

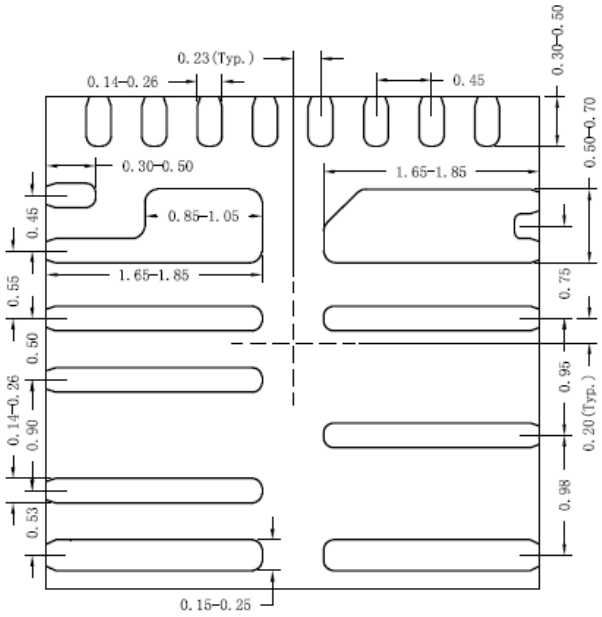
QFN4×4-18 Package Outline and PCB Layout



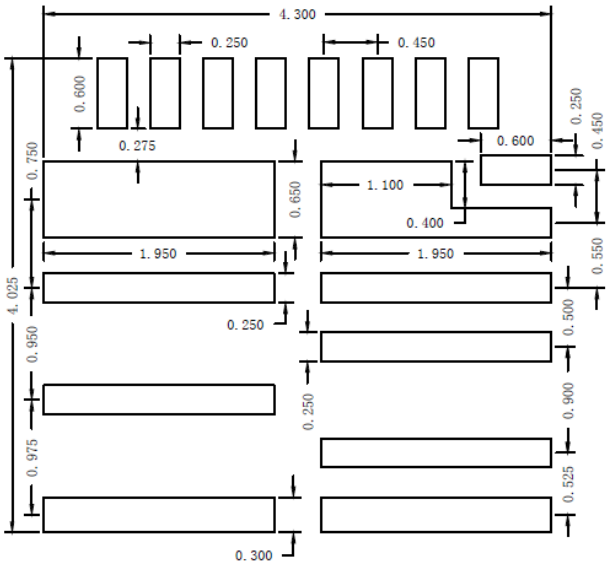
Top view



Side view



Bottom view

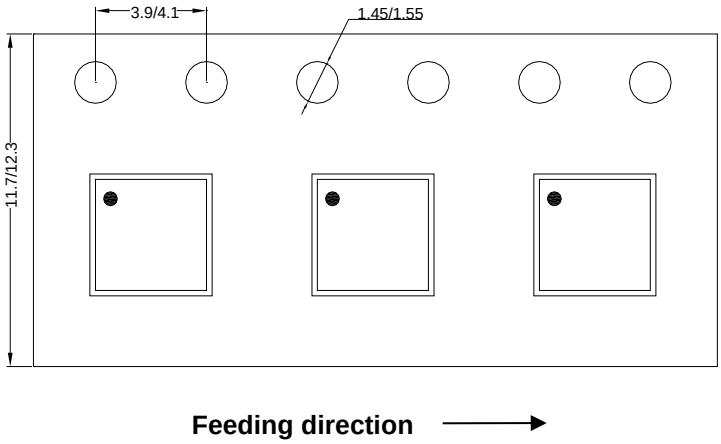


Recommended PCB layout (reference only)

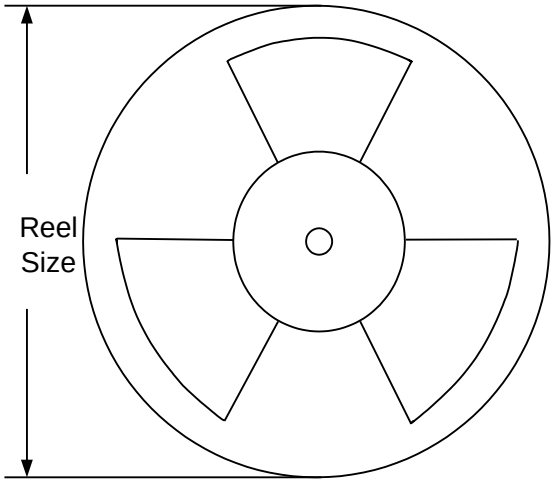
Note: *All dimensions are in millimeters and exclude mold flash and metal burr.*

Taping and Reel Specification

QFN4×4 taping orientation



Carrier tape and reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN4×4	12	8	13"	400	400	5000

Others: NA

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Apr.20, 2023	Revision 1.0	Language improvements for clarity.
Mar.05, 2019	Revision 0.9E	Add Recommended PCB layout ((Reference only) in Package Outline
Sep. 27, 2017	Revision 0.9D	1. Add "Error Amplifier Trans-conductance"& "Current Sense Gain" in EC table; 2. Correct the formula for Output Inductor L (page8); 3. Add "Loop Compensation" in "Applications Information".
June 20, 2017	Revision 0.9C	Add “ Output Voltage Range” in EC table.
May 31, 2017	Revision 0.9B	Update the data in EC table 1. update OVP threshold; 2. Add switching frequency programmable range.
Mar.15, 2017	Revision 0.9A	Update in EC table: 1. Add max. value for Main NFET Current Limit; 2. Add “Output Current Limit Programmable Range”.
Jan.06, 2017	Revision 0.9	Initial Release

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