SY21225

High Efficiency, 15A Synchronous Step Up Regulator with Accurate Output Current Limit

General Description

The SY21225 is a high efficiency synchronous boost regulator with programmable output current limit. The device uses adaptive constant off time and current mode control. The integrated low $R_{DS(ON)}$ switches minimize the conduction loss.

The SY21225 features cycle-by-cycle peak current limit, output short circuit protection and true shutdown. The device also provides enable control and a power good indicator which can be used for system power sequencing. Low output voltage ripple and small external inductor and capacitor sizes can be achieved with a resistor programmable pseudo-constant frequency.

The SY21225 is available in a 4 mm x 4mm QFN package.

Features

- Input Voltage Range: 4.5-30V
- Programmable Pseudo-Constant Frequency 200kHz to 1MHz
- Low $R_{DS(ON)}$ Internal Switches
  Main FET: 16mΩ
  Rectifier FET: 18mΩ
  Disconnect FET: 18mΩ
- True Shutdown Function
- Programmable Output Current Limit
- Internal Soft-start Limits the Inrush Current
- Input Voltage UVLO
- Over Temperature Protection
- Over Voltage Protection
- Output Short Circuit Protection
- Minimum ON Time: 100ns typical
- Minimum OFF Time: 120ns typical

Applications

- Power Bank
- High Power AP

Typical Applications

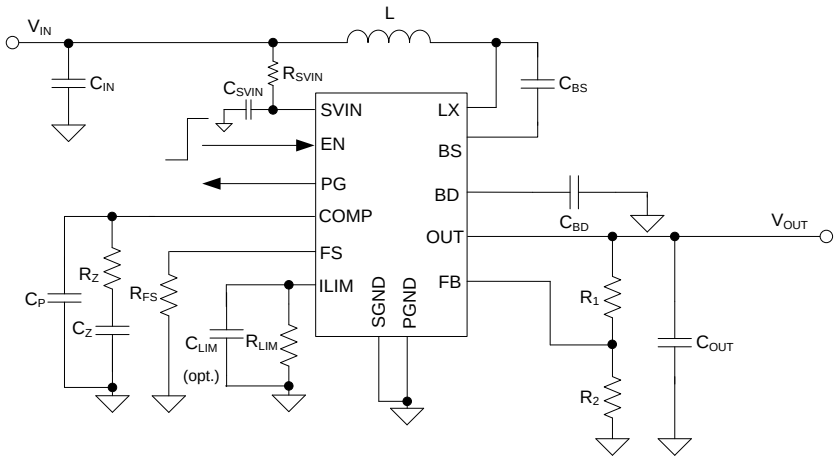


Figure1. Schematic Diagram

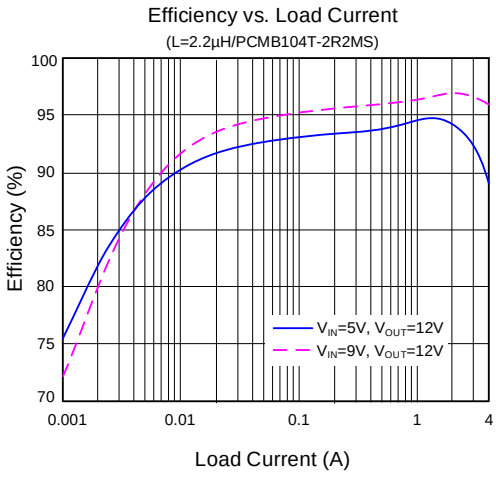


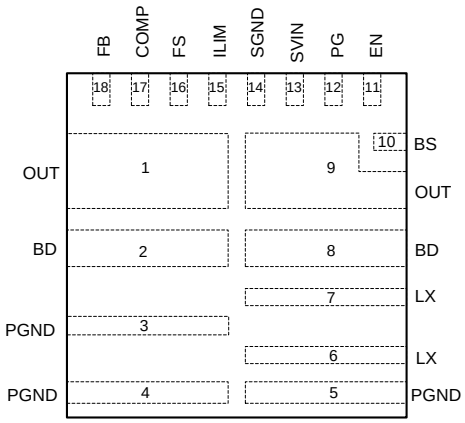
Figure2. Efficiency vs. Load Current

Ordering Information

Ordering Part Number	Package Type	Top Mark
SY21225RDC	QFN4×4-18 RoHS Compliant and Halogen Free	**AVZ*xyz***

x=year code, y=week code, z= lot number code

Pinout (top view)



Pin Description

Pin Name	Pin Number	Pin Description
OUT	1,9	The Boost converter output pin.
BD	2,8	Connect to the Drain of internal Disconnect FET. Bypass at least a 4.7μF ceramic capacitor to PGND.
PGND	3,4,5	Power ground pin.
LX	6,7	Inductor node. Connect an inductor from power input to the LX pin.
BS	10	Boot-strap pin. Supply Rectified FET's gate driver. Connect a 0.1μF ceramic capacitor between the BS pin and the LX pin.
EN	11	Enable control. Pull high to turn on the IC. Do not leave it floating.
PG	12	Power good indicator. Open drain output, driven low when the output < 90% of the target regulation voltage, high impendence otherwise.
SVIN	13	Device power supply pin. Decouple this pin to the SGND pin with a 2.2μF ceramic capacitor.
SGND	14	Signal ground pin.
ILIM	15	Output current limit program pin. Connect a resistor R_{LIM} from this pin to SGND to program output current limitation threshold. $I_{LIM}(A)=30(V)/ R_{LIM}(k\Omega)$
FS	16	Switching frequency configuration pin. Connect a resistor from this pin to ground to program the switching frequency. $f_{SW}(kHz)=1.4\times10^6/R_{FS}(\Omega)^{0.645}$.
COMP	17	Loop compensation pin. Connect a RC network across this pin and ground to stabilize the control loop.
FB	18	Feedback pin. Connect to the center of resistor voltage divider to program the output voltage: $V_{OUT}=1V\times(R_1/R_2+1)$

Block Diagram

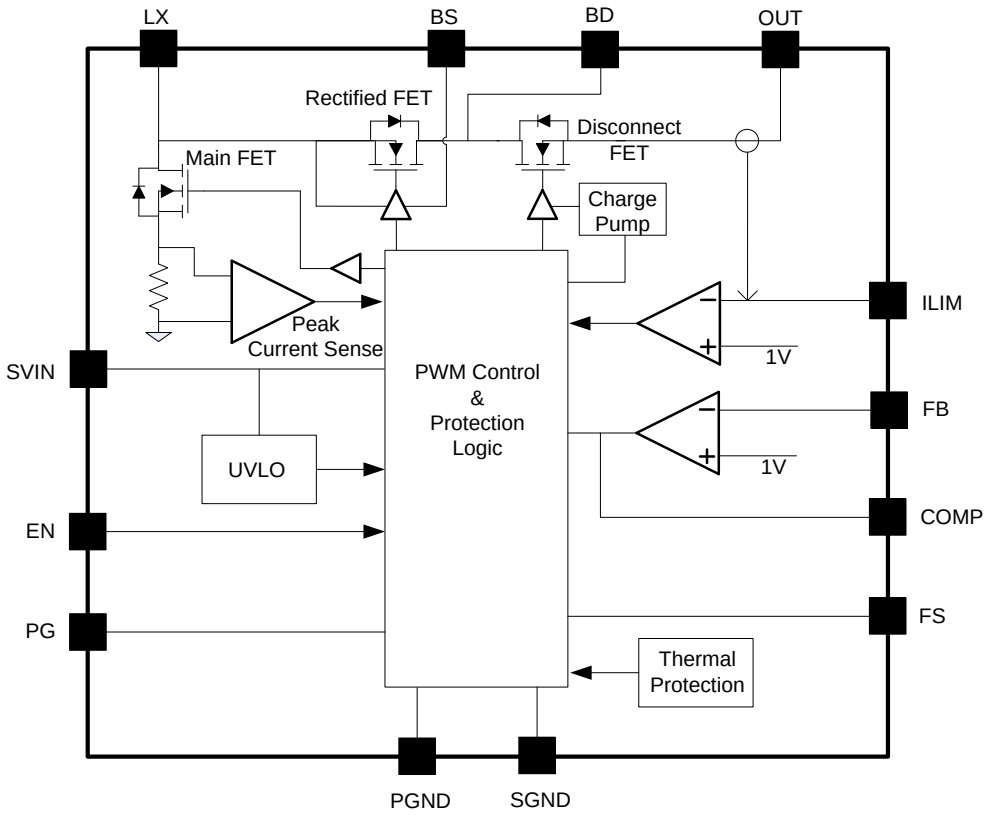


Figure3. Block Diagram

Absolute Maximum Ratings

Parameter (Note1)	Min	Max	Unit
SVIN, LX, EN, ILIM, OUT, BD, FS, PG, COMP	-0.3	33	V
FB, BS-LX	-0.3	4	
LX, 10ns Duration	-3.5	36	
Lead Temperature (Soldering, 10 sec.)		260	°C
Junction Temperature, Operating	-40	150	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note2)	Typ	Unit
θ_{JA} Junction-to-ambient Thermal Resistance	30	°C/W
θ_{JC} Junction-to-case Thermal Resistance	3.2	
P_D Power Dissipation T_A=25°C	3.4	W

Recommended Operating Conditions

Parameter (Note3)	Min	Max	Unit
SVIN	4.5	30	V
Junction Temperature, Operating	-40	125	°C
Ambient Temperature	-40	85	

Electrical Characteristics

(V_{IN} =5V, V_{OUT}=12V, I_{OUT}=100mA, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		4.5		30	V
Input UVLO Threshold	V_{UVLO}			4	4.35	V
UVLO Hysteresis	V_{HYS}			0.2		V
Quiescent Current	I_Q	V_{OUT}=13V			230	μA
Shutdown Current	I_{SHDN}	EN=0			5	μA
Feedback Reference Voltage	V_{REF}		0.985	1	1.015	V
FB Input Current	I_{FB}	V_{FB}=2V	-50		50	nA
Main FET RON	$R_{DS(ON),M}$			16		mΩ
Rectifier FET RON	$R_{DS(ON),R}$			18		mΩ
Disconnect FET RON	$R_{DS(ON),D}$			18		mΩ
EN Rising Threshold	V_{ENH}		1.5			V
EN Falling Threshold	V_{ENL}				0.4	V
Min ON Time	$t_{ON,MIN}$			100		ns
Min OFF Time	$t_{OFF,MIN}$			120		ns
Switching Frequency	f_{SW}	R_{FS}=390kΩ		345		kHz
Switching Frequency Programmable Range			200		1000	kHz
Power Good Threshold	V_{PG}	V_{FB} Rising (Good)		90		$\%V_{REF}$
Power Good Hysteresis	$V_{PG,HYS}$			2.5		$\%V_{REF}$
Power Good Delay	$t_{PG,RISING}$	Low to high		40		μs
	$t_{PG,FALLING}$	High to low		30		μs
Power Good Output Low	V_{PGL}	I_{PG}=4mA		0.15		V
BD Over Voltage Threshold	V_{OVP}	V_{FB} Rising	31			V
BD Over Voltage Hysteresis	$V_{OVP,HYS}$			0.5		V
BD OVP Delay	$t_{OVP,DLY}$			5		μs
Output Under Voltage Protection Threshold	V_{UVP}			2		V
Output UVP Delay	$t_{UVP,\ DLY}$			2		us
Hic-cup ON Time	$t_{UVP,\ ON}$			2		ms
Hic-cup OFF Time	$t_{UVP,\ OFF}$			12		ms
Main N-FET Current Limit	$I_{LIM,PEAK}$		15		21	A
Output Current Limit Programmable Range	$I_{LIM,OUT}$		1		4	A
Output Current Limit Accuracy	$I_{LMT,ACC}$		-25		25	%
Output Current Limit Reference Voltage	V_{LIM}			1		V
Error Amplifier Trans-conductance	g_m			100		μS
Current Sense Gain	R_i			75		mΩ
Thermal Shutdown Temperature	T_{SD}			150		˚C
Thermal Shutdown Hysteresis	T_{HYS}			15		˚C

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a two-layer Silergy Evaluation Board.

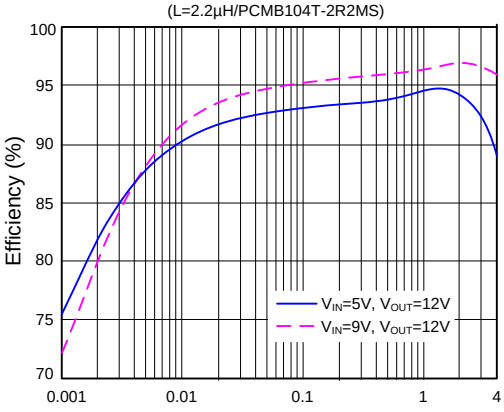
Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

(T_A= 25℃, V_{OUT} = 12V, f_{SW}=350kHz, L = 2.2μH, C_{OUT}= 44μF, unless otherwise specified.)

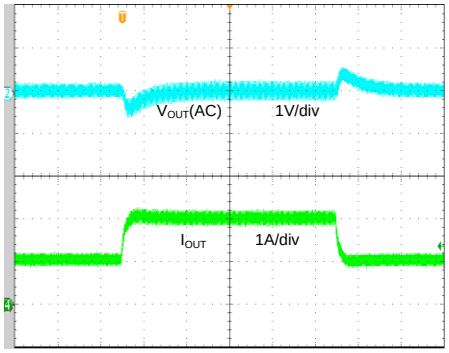
Efficiency vs. Load Current

(L=2.2μH/PCMB104T-2R2MS)



Load Transient

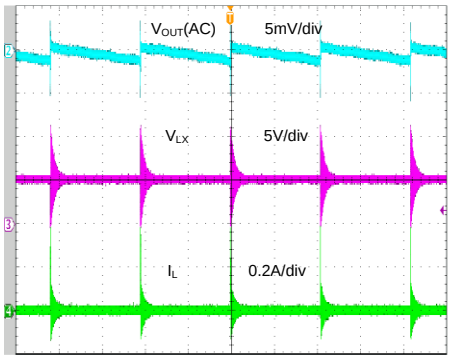
(V_{IN}=5V, V_{OUT}=12V, I_O=1 ~ 2A)



Time (200μs/div)

Output Ripple

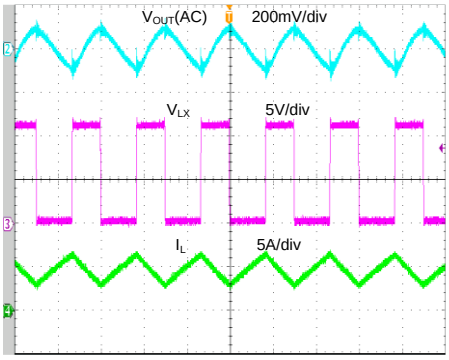
(V_{IN}=5V, V_{OUT}=12V, I_O=0A)



Time (40μs/div)

Output Ripple

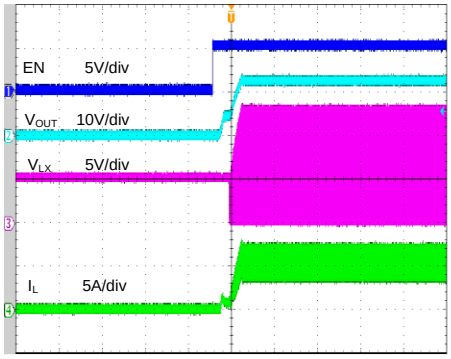
(V_{IN}=5V, V_{OUT}=12V, I_O=2A)



Time (2μs/div)

Startup from Enable

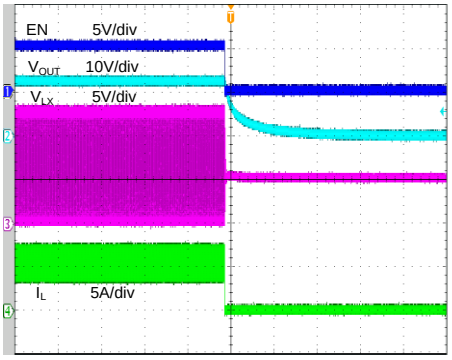
(V_{IN}=5V, V_{OUT}=12V, I_O=2A)



Time (4ms/div)

Shutdown from Enable

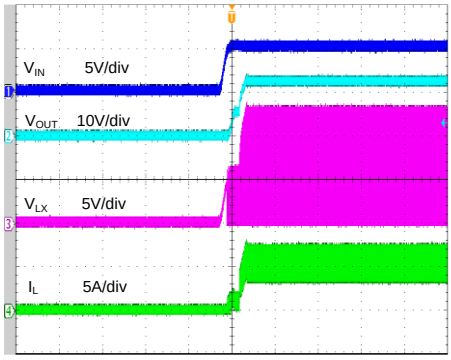
(V_{IN}=5V, V_{OUT}=12V, I_O=2A)



Time (400μs/div)

Startup from V_{IN}

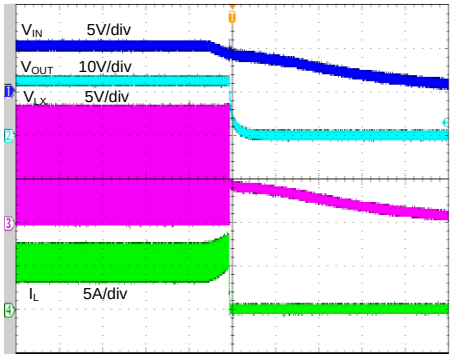
(V_{IN}=5V, V_{OUT}=12V, I_O=2A)



Time (4ms/div)

Shutdown from V_{IN}

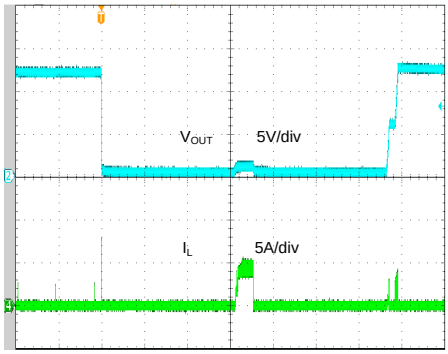
(V_{IN}=5V, V_{OUT}=12V, I_O=2A)



Time (2ms/div)

Short Circuit Protection

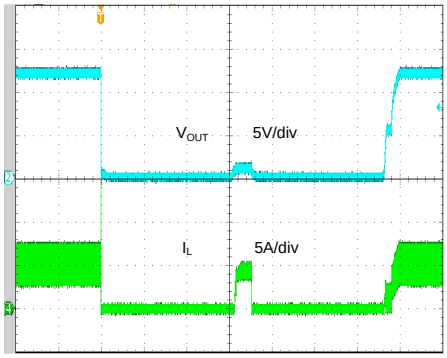
(V_{IN}=5V, V_{OUT}=12V, I_O=0A ~ short)



Time (4ms/div)

Short Circuit Protection

(V_{IN}=5V, V_{OUT}=12V, I_O=2A ~ short)



Time (4ms/div)

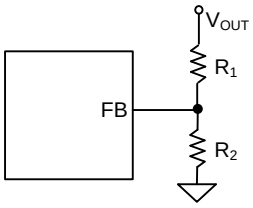
Applications Information

The following paragraphs provide information on the selection of the input capacitor C_{IN}, the output capacitor C_{OUT}, the output current limiting resistor R_{LIM}, the switching frequency programming resistor R_{FS}, the inductor L and the feedback resistors (R_1 and R_2).

Feedback Resistor divider R_1 and R_2

Choose R_1 and R_2 to program the proper output voltage. To minimize the power consumption under light load, it is desirable to choose large resistance values for both R_1 and R_2. A value between 10k and 1M is recommended for both resistors. If R_1=200k is chosen, then R_2 can be calculated to be:

$$R_2 = \frac{R_1}{V_{OUT} - 1}(\Omega)$$



Input Capacitor C_{IN}

The ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2\sqrt{3} \times L \times f_{SW} \times V_{OUT}}(A)$$

To minimize the system switching noise, place a typical X5R or better grade ceramic capacitor close to the inductor and PGND pin. Care should be taken to minimize the loop area formed by CIN, VIN, and the PGND pins. A 10μF low ESR ceramic capacitor is recommended for most applications.

Input Capacitor C_{SVIN}

The SVIN capacitor must be placed close to the SVIN and SGND pins. Care should be taken to minimize the loop area formed by the capacitor and the SVIN/SGND pins. A 2.2μF low ESR ceramic capacitor is recommended for most applications.

Adding the resistor RSVIN with a value of 10 Ω between the VIN pin and the device power input SVIN is recommended.

Boost Output Capacitor C_{BD} and Disconnection FET Output Capacitor C_{OUT}

The Boost Output capacitor C_{BD} and disconnection FET Output capacitor C_{OUT} are selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into account when selecting these capacitors. For the best performance, it is recommended to use a X5R or better grade ceramic capacitors with 25V rating and more than 22μF capacitance.

Boost Inductor L

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum average input current. The inductance is calculated as:

$$L = \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \frac{(V_{OUT} - V_{IN})}{f_{SW} \times I_{OUT\_MAX} \times 40\%}(H)$$

Where f_{SW} is the switching frequency and I_{OUT_MAX} is the maximum load current.

The SY21225 regulator is less sensitive to the ripple current variations. Consequently, the final choice of inductance can be slightly different than the calculated value without significantly impacting the performance.

2) The saturation current rating of an inductor must be selected to guarantee an adequate margin to the peak inductor current under full load conditions.

$$I_{SAT,\,MIN} > \left(\frac{V_{OUT}}{V_{IN}}\right) \times I_{OUT,\,MAX} + \frac{V_{IN}(V_{OUT} - V_{IN})}{2 \times f_{SW} \times L \times V_{OUT}}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirements. It is desirable to choose an inductor with DCR<10mΩ to achieve a good overall efficiency.

Switching Frequency

The switching frequency of the SY21225 in CCM can be programmed by adjusting the external resistor R_{FS} connected to FS pin:

$f_{SW}(kHz) = 1.4 \times 10^6 / R_{FS}(\Omega)^{0.645}$.

Under light load conditions, the SY21225 linearly reduces the switching frequency to maintain overall high efficiency.

Enable Operation

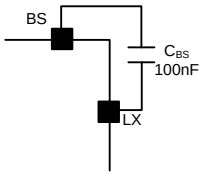
Pulling the EN pin low (<0.4V) disables the device operation. Driving the EN pin high (>1.5V) turns on the device, and a soft start cycle is initiated.

Power Good Indication

PG is an open-drain output pin. The output is driven low if the output voltage is lower than 90% of the regulation target. Otherwise this pin will go into high impedance state.

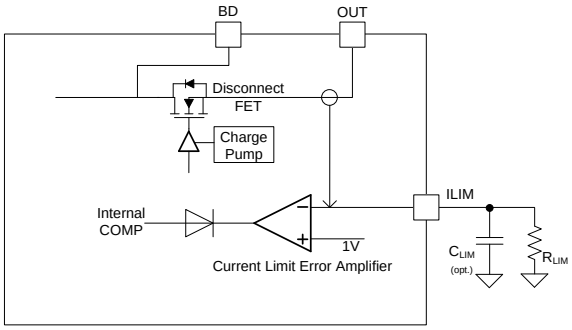
External Bootstrap Capacitor

This capacitor provides the gate driver voltage for the internal rectifier switch. A 100nF low ESR ceramic capacitor connected between the BS and the LX pins is recommended.



Output Current Limit

The SY21225 senses the Disconnect FET current which is fed to the ILIM pin. Simultaneously, a resistor on ILIM converts this current signal to a voltage signal that is fed to the negative input of the current-limit error amplifier. The current-limit amplifier output clamps VCOMP if the output current signal is higher than the current limit threshold. As a result, the output current is limited by the internal COMP signal, and the output voltage decreases.



C_{LIM} is used for current limit signal filtering. A 10pF ceramic capacitor is recommended. R_{LIM} is used for output current limit setting. The output current limit can be programmed using the following the equation:
$I_{LIM}(A)=30(V)/ R_{LIM}(k\Omega)$.

Short-circuit Protection

The SY21225 integrates a hic-cup mode short circuit protection function. If the device is operated in current limit continuously and V_{OUT} drops below 2V, the short-circuit protection mode will be initiated. The device will shut down for approximately 12ms, and then restart with a complete soft-start cycle that is approximately 2ms. The device operates in this state until the short condition disappears.

Main FET Current Limit

The SY21225 provides a fixed cycle-by-cycle switching peak current limit. During each cycle, the internal current sensing circuit monitors the Main FET current. When the sensed current reaches the 15A (typ.) current limit, the Main FET turns off.

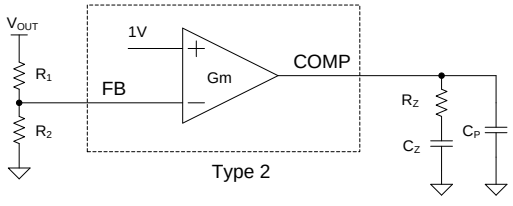
Over-temperature Protection (OTP)

The SY21225 includes over-temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. This will shut down switching operation when the junction temperature exceeds 150°C. Once the junction temperature cools down by approximately 15°C the IC will resume normal operation after a complete soft-start cycle. For continuous operation, provide adequate cooling so that the junction temperature does not exceed the OTP threshold.

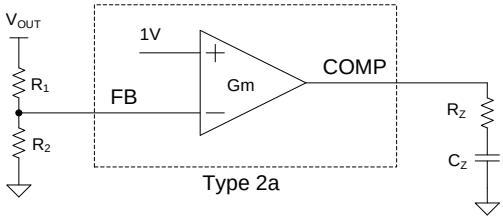
Loop Compensation

The SY21225 incorporates constant off time current mode control scheme. The current mode control scheme has two feedback loops. The inner current loop does not require any external compensation component. The outer voltage loop is compensated using external components.

In most applications, a Type 2 or Type 2a compensation networks shown below can be used to stabilize the voltage loop. The Type 2 is the most widely used and is recommended for power stages lagging down to -90˚ and where the voltage increase caused by the output capacitor ESR must be canceled. Type 2a is used in cases where the output capacitor ESR effect can be neglected.



Type 2



Type 2a

The steps below can be used to calculate the value of external components for voltage loop compensation.

1. Select the crossover frequency fc of the closed loop. It is recommended that the crossover frequency is chosen to be the minimum value of 1/5 of right half plane zero

(f_{RHPZ}) and 1/10 of switching frequency for a tradeoff between stability and transient response of the system. The system has faster response at higher crossover frequencies.

$$f_{RHPZ} = \frac{(1-D_{MAX})^2 \times V_{OUT}}{2\pi \times L \times I_{OUT}}$$

2. Select a Rz value of the R-C series combination connected to the COMP pin.

$$R_Z = \frac{V_{OUT}}{g_m \times G_{fc} \times V_{REF}}$$

Where g_m is the error amplifier trans-conductance, which is typically 100uS; G_{fc} is gain of the power stage at crossover frequency.

$$G_{fc} = \frac{(1-D_{MAX})}{2\pi \times fc \times C_{OUT} \times R_i}$$

Where R_i is the current sense gain, which is typically 75mΩ.

3. Select a Cz value of the R-C series combination connected to the COMP pin. The compensation zero decides phase margin at the crossover frequency. Place a compensation zero at or before the dominant pole of R_L and C_O. R_L is the load resistance, which equals to V_{OUT}/I_{OUT}.

$$C_Z = \frac{V_{OUT} \times C_{OUT}}{I_{OUT} \times R_Z}$$

4. A high frequency pole is recommended to attenuate the high frequency noise. Place this pole to cancel the ESR zero of C_{OUT}

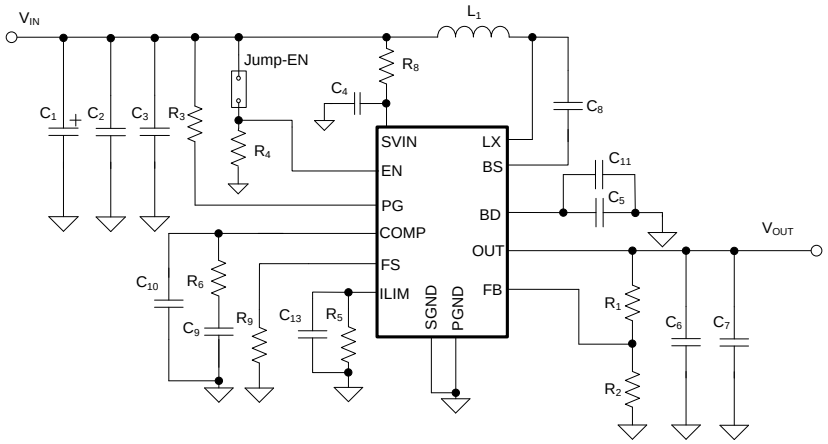
$$C_P = \frac{R_{ESR} \times C_O}{R_Z}$$

Soft Start Circuit

The SY21225 includes a soft-start circuit that is used to limit the in-rush current during the device power up sequence. Using the recommended output capacitors for the BD and OUT pins the typical soft-start time is about 2ms. When larger capacitance and output current are used on the output, the soft-start time will proportionally increase.

Typical Design

Typical Schematic



Design Specifications

Input Voltage (V)	Output Voltage (V)	Output Current Limit (A)
4.5-10	12	3

BOM List

Reference Designator	Description	Part Number	Manufacturer
C_1	220μF/35V, Electrolytic Capacitor		
C_3, C_5, C_6, C_7, C_{11}	22μF/25V.1206	C3216X5R1E226M	
C_4	2.2μF/25V, 1206	C3216X7R1E225K	
C_8	100nF/50V, 0603	C1608X7R1H104K	
C_9	1nF/50V, 0603	C1608C0G1H102J	
C_{10}	22pF/50V, 0603	C1608C0G1H220J	
C_{13}	10pF/50V,0603	C1608C0G1H100D	
R_1	110kΩ, 0603		
R_2	10kΩ, 0603		
R_3	100kΩ, 0603		
R_4	1MΩ, 0603		
R_5	7.5kΩ, 0603		
R_6	30kΩ, 0603		
R_8	10Ω, 0603		
R_9	390kΩ, 0603		
L_1	2.2μH/12A	PIMB104T-2R2MS	

Recommend Table for Typical Applications

V_{OUT}(V)	R_H(kΩ)	R_L(kΩ)	L(μH)	C_{OUT}
12	110	10	2.2	2*22μF/25V/X7R,1206
24	230	10	2.2	2*22μF/25V/X7R,1206

Layout Design

To achieve a higher efficiency and better noise immunity, following components should be placed close to the IC: C_{IN}, C_{BD}, C_{OUT}, L, R_1 and R_2.

1) It is desirable to maximize the PCB copper area connecting to PGND pin to achieve a better thermal performance and noise immunity. A designated ground plane layer is highly recommended.

2) C_{SVIN} must be close to SVIN and SGND pins. The loop area formed by C_{SVIN}, SVIN and SGND pins must be minimized.

3) C_{BD} must be close to BD and the PGND pins. The loop area formed by $C_{BD,}$ BD and the PGND pins must be minimized.

4) The PCB copper area associated with the LX pin must be minimized to improve the noise immunity.

5) The components R_1 and R_2 and the trace connecting to the FB pin must NOT be adjacent to the LX node on the PCB layout to minimize the noise coupling to FB pin.

6) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the SVIN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull-down 1MΩ resistor across the EN and SGND pins to prevent noise from falsely turning on the regulator while in shutdown mode.

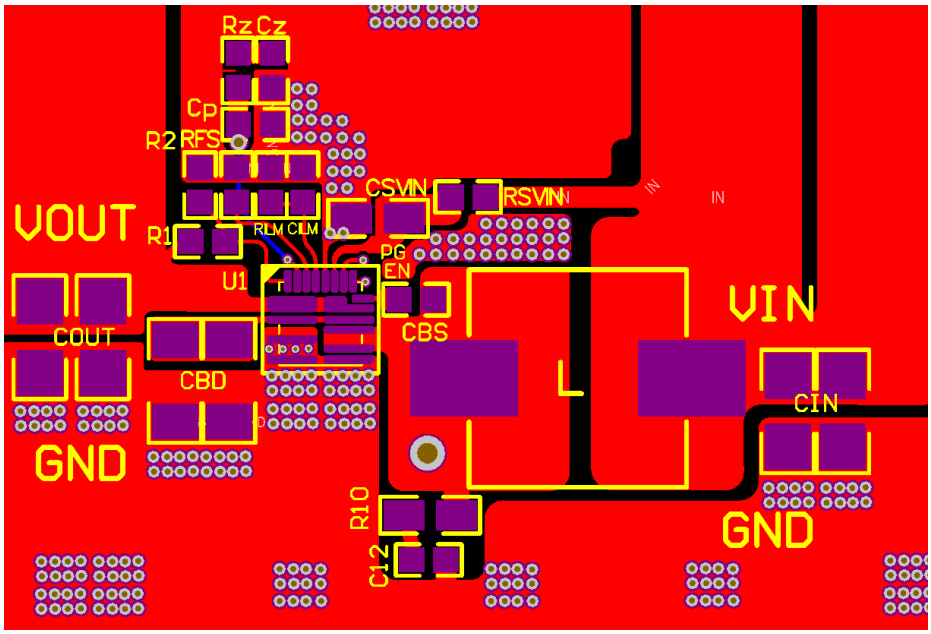
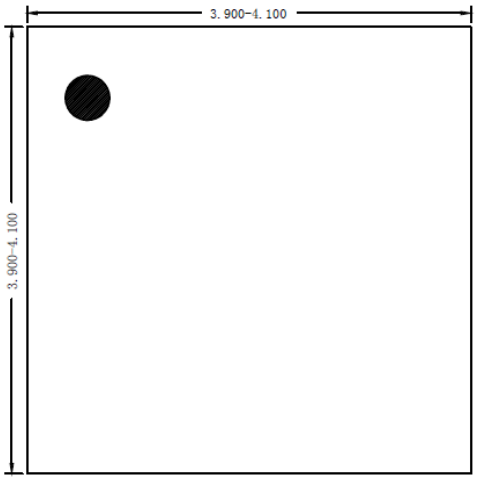


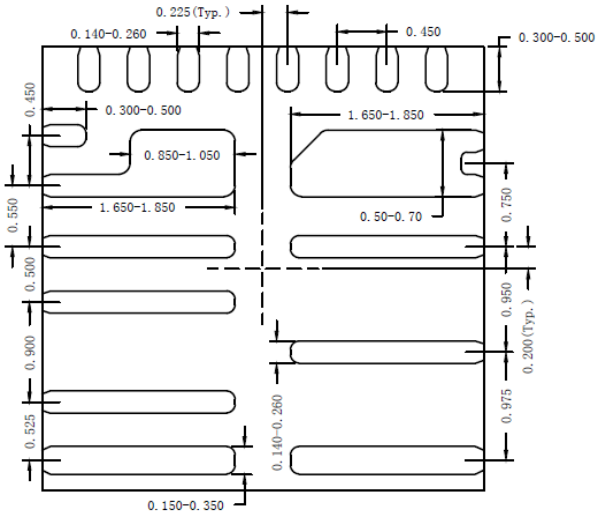
Figure4. PCB Layout Suggestion

QFN4×4-18 Package Outline Drawing

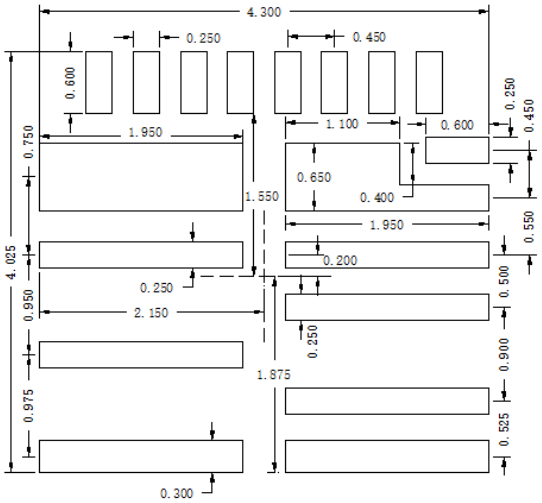


Top View

Side View



Bottom View



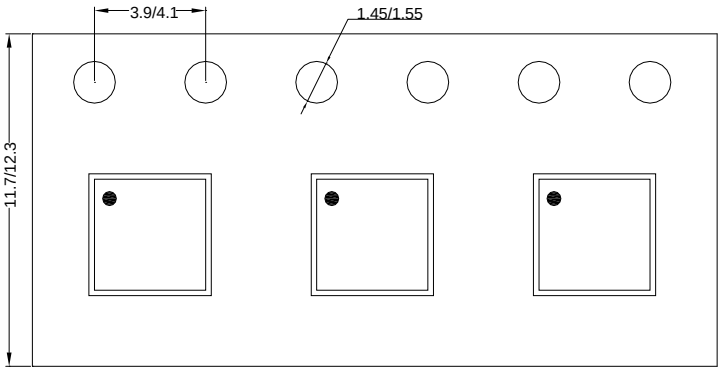
Recommended PCB layout
(Reference only)

Notes: All dimensions in millimeter and exclude mold flash & metal burr;
The center of PCB diagram refers to chip body center.

Taping & Reel Specification

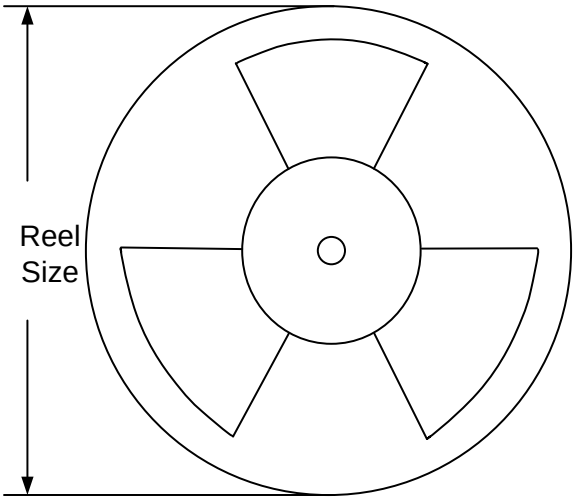
1. Taping orientation

QFN4×4



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN4×4	12	8	13"	400	400	5000

3. Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Apr.20, 2023	Revision 1.0	Language improvements for clarity.
Nov.05, 2019	Revision 0.9	Initial Release

IMPORTANT NOTICE

1. **Right to make changes.** Silergy and its subsidiaries (hereafter Silergy) reserve the right to change any information published in this document, including but not limited to circuitry, specification and/or product design, manufacturing or descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to Silergy's standard terms and conditions of sale.

2. Applications. Application examples that are described herein for any of these products are for illustrative purposes only. Silergy makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Buyers are responsible for the design and operation of their applications and products using Silergy products. Silergy or its subsidiaries assume no liability for any application assistance or designs of customer products. It is customer's sole responsibility to determine whether the Silergy product is suitable and fit for the customer's applications and products planned. To minimize the risks associated with customer's products and applications, customer should provide adequate design and operating safeguards. Customer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Silergy assumes no liability related to any default, damage, costs or problem in the customer's applications or products, or the application or use by customer's third-party buyers. Customer will fully indemnify Silergy, its subsidiaries, and their representatives against any damages arising out of the use of any Silergy components in safety-critical applications. It is also buyers' sole responsibility to warrant and guarantee that any intellectual property rights of a third party are not infringed upon when integrating Silergy products into any application. Silergy assumes no responsibility for any said applications or for any use of any circuitry other than circuitry entirely embodied in a Silergy product.

3. **Limited warranty and liability.** Information furnished by Silergy in this document is believed to be accurate and reliable. However, Silergy makes no representation or warranty, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. In no event shall Silergy be liable for any indirect, incidental, punitive, special or consequential damages, including but not limited to lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges, whether or not such damages are based on tort or negligence, warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, Silergy' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Standard Terms and Conditions of Sale of Silergy.

4. **Suitability for use.** Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Silergy components in its applications, notwithstanding any applications-related information or support that may be provided by Silergy. Silergy products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of a Silergy product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Silergy assumes no liability for inclusion and/or use of Silergy products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

5. **Terms and conditions of commercial sale**. Silergy products are sold subject to the standard terms and conditions of commercial sale, as published at http://www.silergy.com/stdterms, unless otherwise agreed in a valid written individual agreement specifically agreed to in writing by an authorized officer of Silergy. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Silergy hereby expressly objects to and denies the application of any customer's general terms and conditions with regard to the purchase of Silergy products by the customer.

6. **No offer to sell or license**. Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights. Silergy makes no representation or warranty that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right. Information published by Silergy regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from Silergy under the patents or other intellectual property of Silergy.

For more information, please visit: www.silergy.com