

General Description

SY205221DWC is a low-capacitance transient voltage suppressor (TVS) designed to provide electrostatic discharge (ESD) protection for high-speed data interfaces. With a typical capacitance of 0.5pF, SY205221DWC is designed to protect against over-voltage and over-current transient events. It complies with IEC 61000-4-2 (ESD ($\pm 20\text{kV}$ air, $\pm 20\text{kV}$ contact discharge), IEC 61000-4-5 (surge) (4A, 8/20 μs).

The combined features of low capacitance, ultra-small size, and high ESD robustness make SY205221DWC ideal for high-speed data port and high-frequency line (e.g., HDMI & antenna line) applications, such as cellular phones and HD visual devices.

Each SY205221DWC device can protect one high-speed data line. The SY205221DWC is available in a small DFN1.0x0.6-2L package.

Features

- Low Clamping Voltage
- Low Capacitance: 0.5pF (Typical)
- Transient Protection for High-speed Data Lines
 - IEC 61000-4-2 (ESD) $\pm 20\text{kV}$ (Air) $\pm 20\text{kV}$ (Contact)
 - IEC 61000-4-5 (Surge) 4A (8/20 μs)
- Package Optimized for High-Speed Lines
- Ultra-Small Package (1.0mmx0.6mmx0.55mm)
- Protects One Data, Control, or Power Line
- Low Leakage Current: 0.1 μA @ V_{RWM} (Typical)
- Each I/O pin can withstand over 1000 ESD strikes for $\pm 8\text{kV}$ contact discharge.

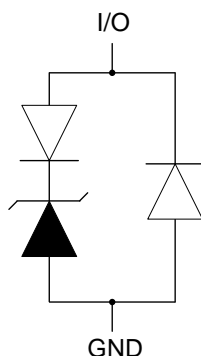
Applications

- Serial ATA
- PCI Express
- Desktops, Servers, and Notebooks
- Cellular Phones
- MDDI Ports
- USB 2.0 Power and Data Line Protection
- Display Ports
- High-Definition Multi-Media Interface (HDMI)
- Digital Visual Interfaces (DVI)

Mechanical Characteristics

- DFN1.0x0.6-2 package
- Marking: Device code, date code
- Packaging: Tape and Reel

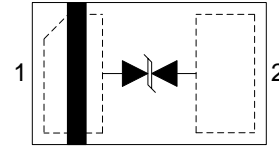
Circuit Diagram



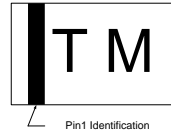
Ordering Information

Pinout (Top View)

Part Number	Package Type	Top Mark
SY205221DWC	DFN1.0x0.6-2 RoHS Compliant and Halogen Free	TM



Marking Codes



Note 1: "T" is device code, fixed.

Note 2: "M" is date code.

Absolute Maximum Rating				
Parameter	Symbol	Min	Max	Unit
Maximum Peak Pulse Current (8/20μs)	I_{PP}		4	A
Maximum Peak Pulse Power (8/20μs)	P_{PK}		50	W
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	-20	20	kV
Operating Temperature	T_{OPT}	-55	+125	°C
Storage Temperature	T_{STG}	-55	+150	°C

Electrical Characteristics $T_A = 25^\circ\text{C}$						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Nominal Reverse Working Voltage	V_{RWM}				5.5	V
Reverse Leakage Current @ V_{RWM}	I_R	$V_{RWM} = 5.5\text{V}$, $T = 25^\circ\text{C}$ Between I/O and GND		0.1	1.0	μA
Reverse Breakdown Voltage @ I_T	V_{BR}	$I_T = 1\text{mA}$ Between I/O and GND	6.0	8.0	9.0	V
Clamping Voltage @ I_{PP}	V_C	$I_{PP} = 1\text{A}$, $t_p = 8/20\mu\text{s}$, Between I/O and GND			10	V
Clamping Voltage @ I_{PP}	V_C	$I_{PP} = 4\text{A}$, $t_p = 8/20\mu\text{s}$, Between I/O and GND			12.5	V
Dynamic Resistance	R_{DYN}	Dynamic Resistance		0.4		Ω
Parasitic Capacitance	C_{ESD}	$V_R = 0\text{V}$, $f = 1\text{MHz}$ Between I/O and GND		0.5	0.8	pF

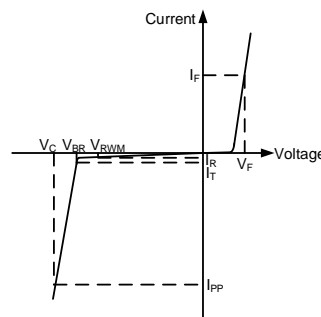
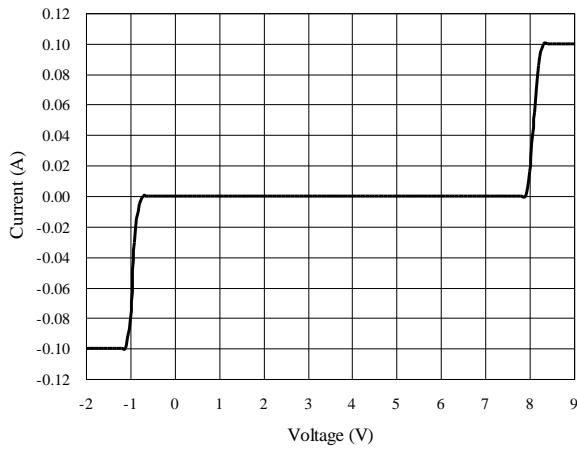


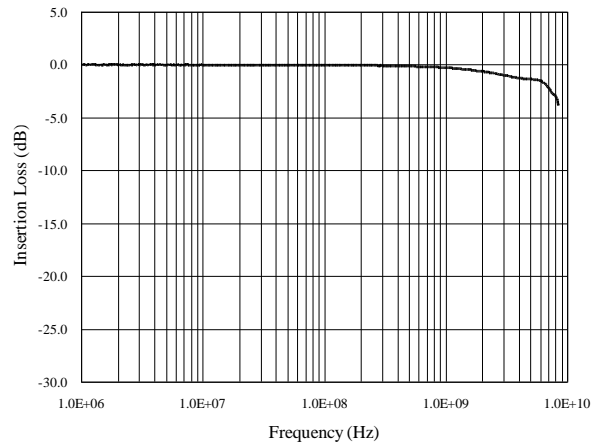
Figure 1. Uni-directional TVS

Typical Performance Characteristics

Voltage Sweeping of I/O to GND

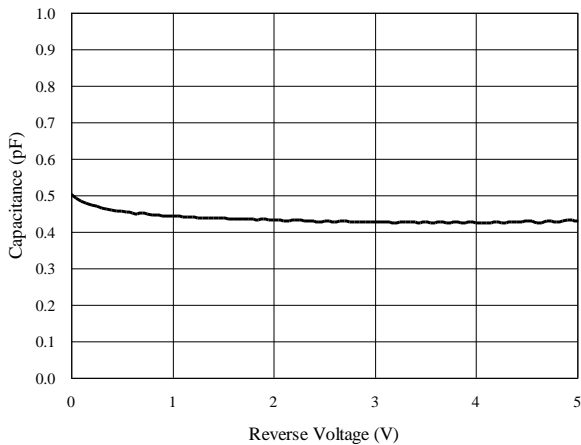


Insertion Loss S21 of I/O to GND

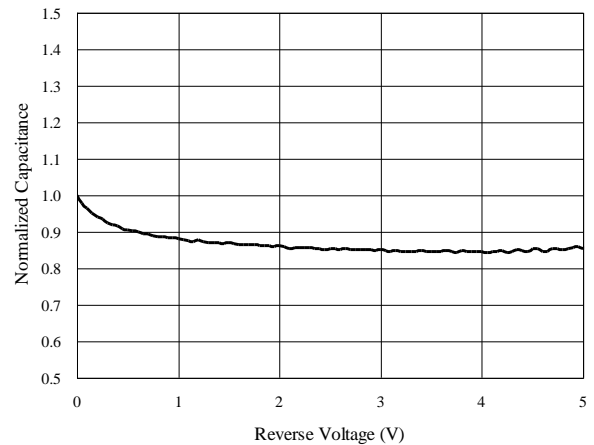


Capacitance vs. Voltage of I/O to GND (f = 1MHz)

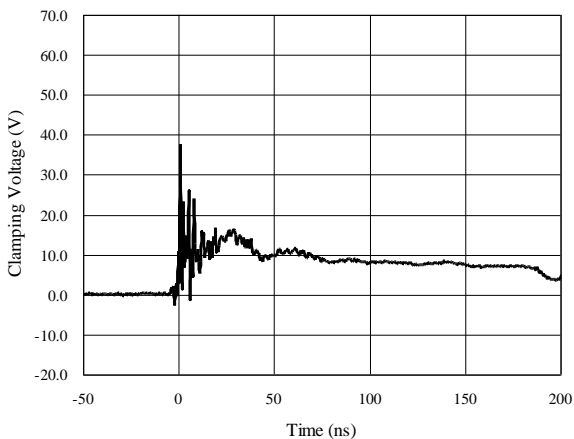
Capacitance vs. Reverse Voltage



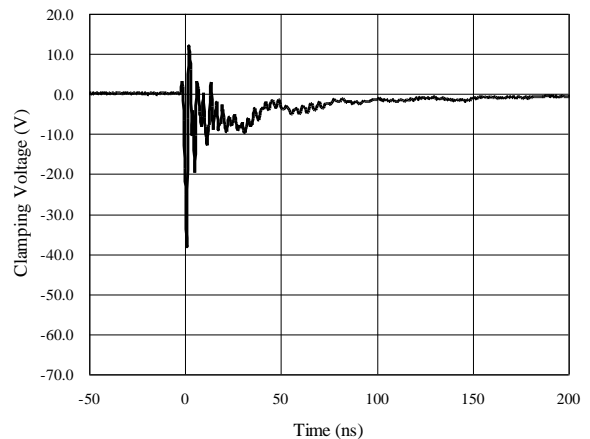
Normalized Capacitance vs. Reverse Voltage



ESD Clamping of I/O to GND (+8kV Contact per IEC 61000-4-2)



ESD Clamping of I/O to GND (-8kV Contact per IEC 61000-4-2)



Application Information

SY205221DWC is designed to protect one uni-directional data line against over-voltage and over-current transient events by clamping it to an acceptable reference.

The SY205221DWC pin connections are shown in Figure 2. The protected line is connected to Pin1. Pin2 is connected to the GND, which should connect to a ground plane on the board. All path lengths connected to pins of SY205221DWC should be as short as possible to minimize the parasitic inductance.

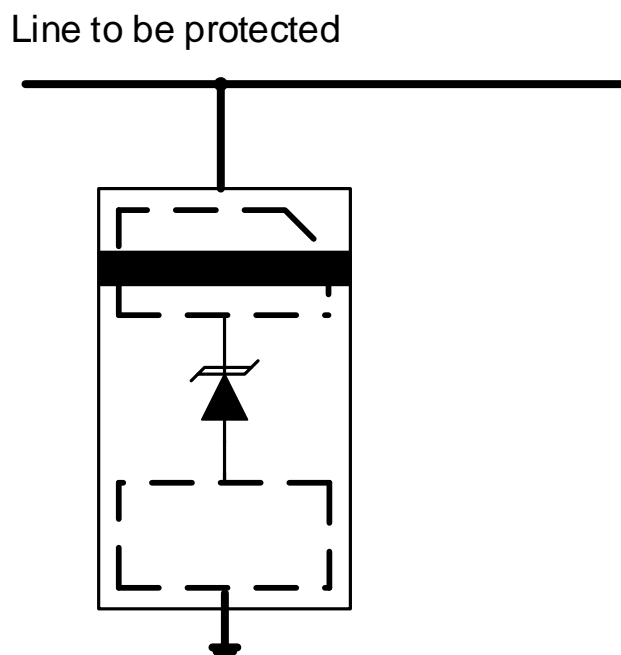


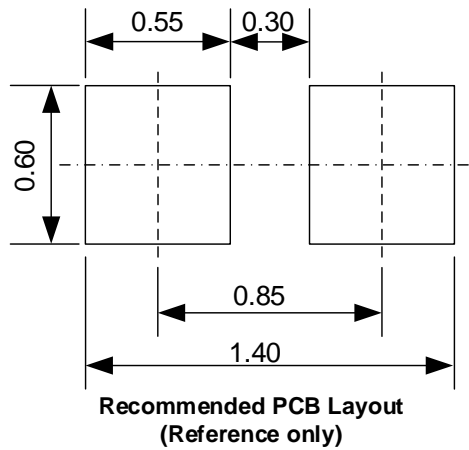
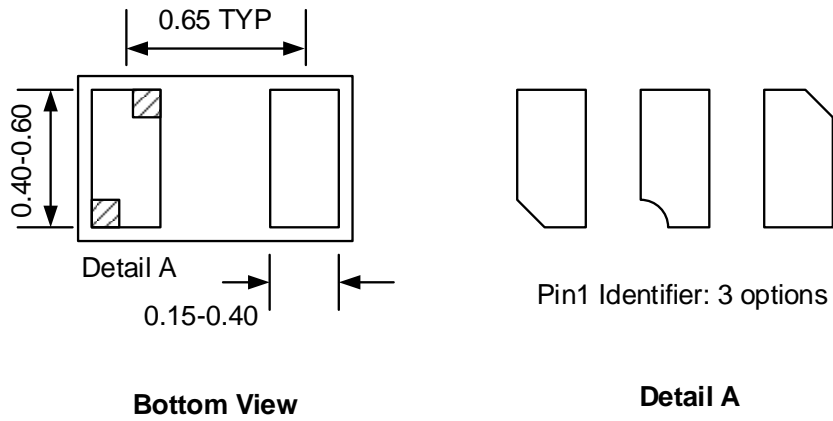
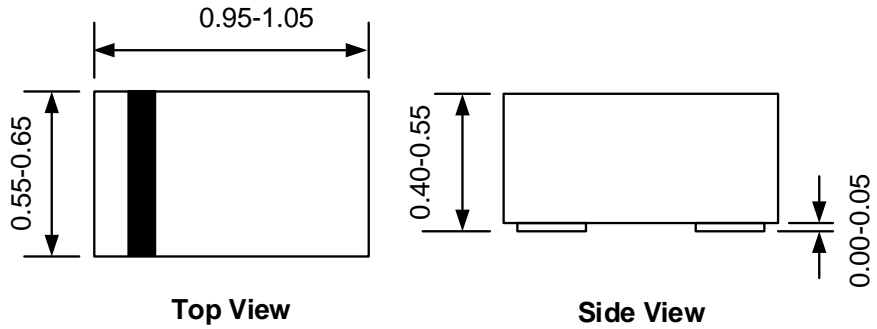
Figure 2. ESD/ Surge Protection Circuit

PCB Layout Guidelines

For optimum ESD protection and circuit performance, the following PCB layout guidelines are recommended:

- Place SY205221DWC as close to the connector port as possible.
- Use a large via to connect the SY205221DWC pin to the ground.
- Avoid running signals near board edges.
- The SY205221DWC should be placed near the protected line.
- The distance between the SY205221DWC ground pin and the GND reference path should be as short as possible.

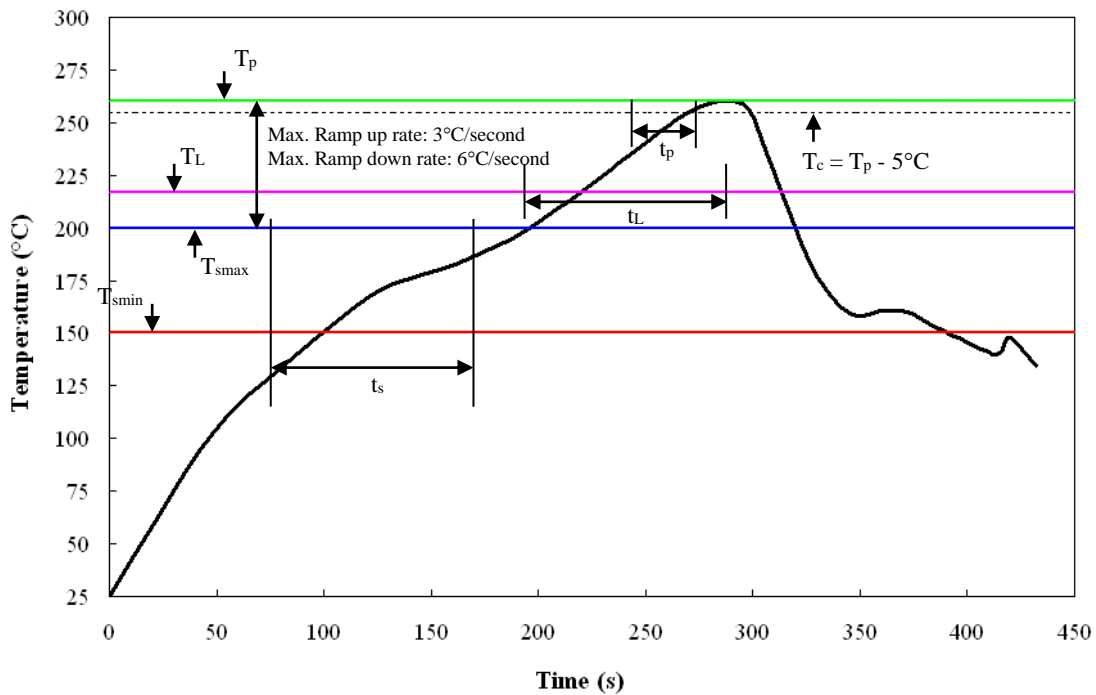
DFN1.0x0.6-2 Package Outline



Note: All dimensions are in millimeters and exclude mold flash and metal burr.

Reflow Profile

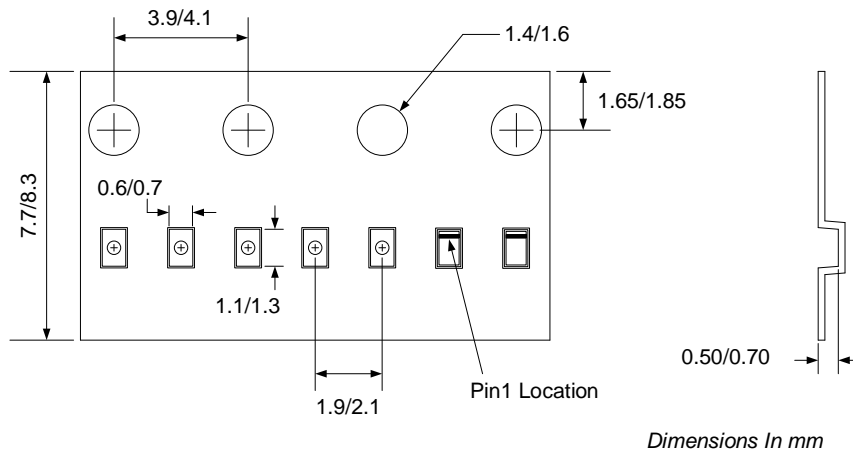
Profile Feature	Pb-Free Assembly
Temperature min (T_{smin})	150°C
Temperature max (T_{smax})	200°C
Time (T_{smin} to T_{smax}) (t_s)	60-120 seconds
Average ramp-up rate (T_{smax} to T_p)	3°C/second max.
Liquidous temperature (T_L)	217°C
Time at liquidous (t_L)	60-120 seconds
Peak package body temperature (T_p)	260°C
Time (t_p) within 5°C of the specified Classification temperature (T_c)	30 seconds
Average ramp-down rate (T_p to T_{smax})	6°C/second max.
Time from 25°C to peak temperature	6 minutes max.



Reflow Profile

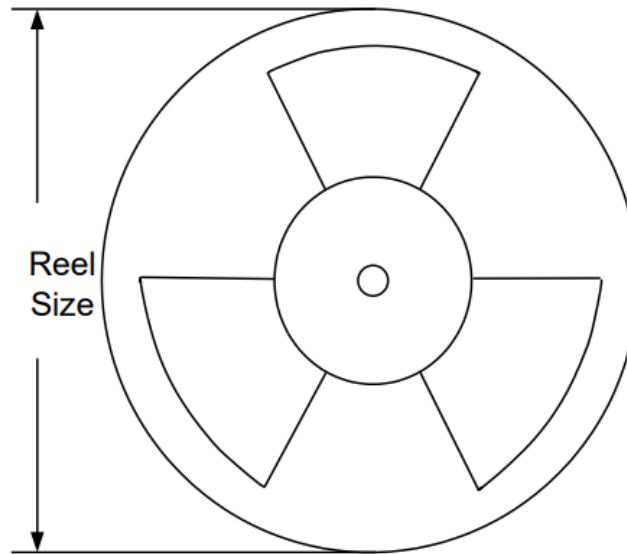
Tape and Reel Specification

DFN1.0x0.6-2 Taping Orientation



Feeding direction →

Carrier Tape & Reel Specification for Packages



Package Types	Tape Width (mm)	Pocket Pitch (mm)	Reel Size (in)	Qty per Reel(pcs)
DFN1.0x0.6-2	8	2	7"	10000



Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Revision Number	Revision Date	Description	Pages changed
0.9	04/01/2014	Initial Release	
1.0	04/01/2015	Production Release	



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