SY20011

400nA Low I_Q, 5.5V, 500mA, 1MHz Synchronous Buck Converter

General Description

The SY20011 high-efficiency 1MHz synchronous Buck converter operates over a wide input voltage range from 2.5V to 5.5V and is capable of delivering up to 500mA output current. It integrates a top FET and a bottom FET with very low $R_{DS(ON)}$ to minimize conduction loss.

The SY20011 adopts a constant on-time and ripple-based control strategy to achieve fast transient responses. The input and output capacitors, the inductor, and the resistor-divider components must be selected for the targeted application specifications.

The device uses only 400nA quiescent current (typ, STB=0) and only 10nA (typ.) in shutdown mode. This makes it ideal in the design of products that use very small batteries, and where battery life is critical.

The SY20011 is available in a space-saving, low-profile DFN2×2-8 package.

Features

- Low $R_{DS(ON)}$ for Internal Switches: 170mΩ Top, 120mΩ Bottom
- 2.5 ~ 5.5V Input Voltage Range
- Up to 500mA Output Current
- Low 400nA Quiescent Current (typ., STB=0)
- High 1MHz Switching Frequency Minimizes Required External Components
- Constant On-Time and Ripple-Based Control
- Internal Soft-Start Limits Inrush Current
- 100% Dropout Operation
- Power-Good Indicator
- Hiccup Mode for Short-Circuit Protection
- Output Auto-Discharge Function
- RoHS-Compliant and Halogen-Free
- Compact DFN2×2-8 Package

Applications

- Battery-Powered Applications
- Consumer and Portable Medical Products
- Wearable Products and IoT

Typical Application

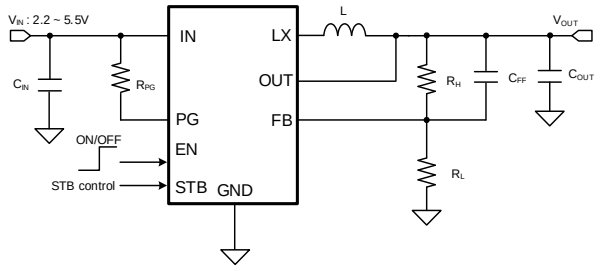


Figure 1. Schematic Diagram

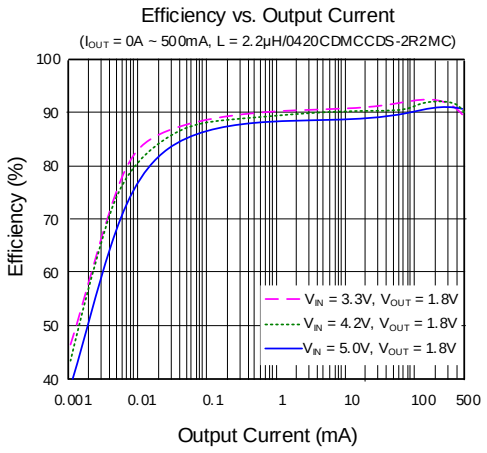


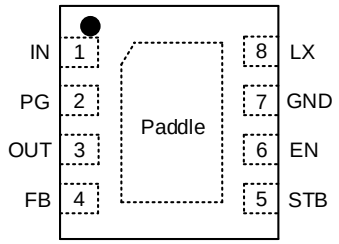
Figure 2. Efficiency vs. Output Current

Ordering Information

Ordering Part Number	Package type	Top Mark
SY20011DFC	DFN2×2-8 RoHS-Compliant, Halogen-Free	**Wtxyz**

x = year code, y = week code, z = lot number code

Pinout (top view)



(DFN2x2-8)

Pin Description

Pin No	Pin Name	Pin Description
1	IN	Power input pin. Decouple this pin to the GND pin with at least a 10μF ceramic capacitor.
2	PG	Power-good indicator. Open-drain output when the output voltage is above 90% of the regulation point.
3	OUT	Output pin for stable operation. Connect to the output of the Buck convertor.
4	FB	Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{OUT} = 1.2V \times (1 + R_H/R_L)$.
5	STB	Standby mode selection pin. STB = low: deep standby function is enabled, $I_Q = 400nA$. STB = high: deep standby function is disabled, $I_Q = 15\mu A$.
6	EN	Enable control pin. Pull high to turn on the device and pull low to turn off the device. Do not leave this pin floating.
7	GND	Power ground pin.
8	LX	Inductor pin. Connect this pin to the switching node of inductor.

Block Diagram

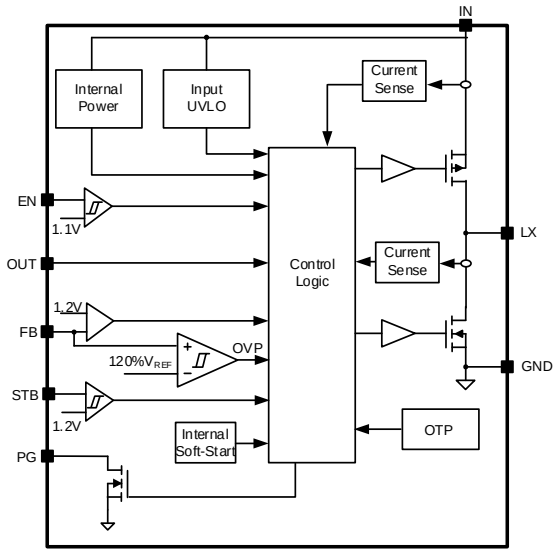


Figure 3. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
IN	-0.3	6	V
EN, FB, PG, OUT, STB	-0.3	IN + 0.6	
LX	-0.3	6	
LX, 40ns duration	-3	7	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering,10s)		260	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	85	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	45	
P_D Power Dissipation T_A = 25°C	1.1	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
IN	2.5	5.5	V
Output Voltage	1.2	5.5	
Output Current		500	mA
Junction Temperature	-40	125	°C

Electrical Characteristics

(V_{IN} = 5V, V_{OUT} = 1.8V, L = 2.2μH, C_{OUT} = 10μF, T_J = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input	Voltage	V_{IN}		2.2		5.5	V
	UVLO Rising Threshold	$V_{IN,UVLO}$				2.2	
	UVLO Hysteresis	$V_{IN,HYS}$			150		mV
	Quiescent Current	I_Q	V_{FB} = 115% × V_{REF}, STB = Low		400	600	nA
			V_{FB} = 115% × V_{REF}, STB = High		15		μA
	Shutdown Current	I_{SHDN}	V_{EN} = 0V		10	100	nA
Output	Reference Voltage	V_{REF}		1.182	1.2	1.218	V
	Turn-On Delay Time	$t_{ON,DLY}$	From EN high to LX start switching		0.4		ms
	UVP Threshold	V_{UVP}	V_{OUT} threshold		1		V
	UVP Delay	$t_{UVP,DLY}$			20		μs
	UVP Hiccup On-Time	$t_{HICCUP,ON}$			0.25		ms
	UVP Hiccup Off-Time	$t_{HICCUP,OFF}$			0.25		
	Discharge On-Resistance	R_{DIS}			10		Ω
MOSFET	Top FET $R_{DS(ON)}$	$R_{DS(ON)1}$			280		mΩ
	Bottom FET $R_{DS(ON)}$	$R_{DS(ON)2}$			120		
	Top FET Current Limit Threshold	$I_{LMT,TOP}$		0.9		1.5	A
	Bottom FET Current Limit Threshold	$I_{LMT,BOT}$		0.5			
Enable (EN)	Input Voltage High	$V_{EN,H}$		1.1			V
	Input Voltage Low	$V_{EN,L}$				0.4	
Power-Good	Thresholds	$V_{PG,R}$	V_{FB} rising, good		90		%V_{REF}
	Delay	$t_{PG,F}$	V_{FB} falling, not good		20		μs
COT	Switching Frequency	f_{SW}	I_{OUT} = 500mA, CCM		1		MHz
	Minimum On-Time	$t_{ON,MIN}$			80		ns
	Maximum Duty Cycle	D_{MAX}		100			%
OTP	Temperature	T_{OTP}			150		°C
	Temperature Hysteresis	T_{HYS}			15		

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} of the SY20011DFC is measured in the natural convection at T_A = 25°C on a 2oz two-layer Silergy evaluation board. Pin 8 is the case position for SY20011DFC θ_{JC} measurement.

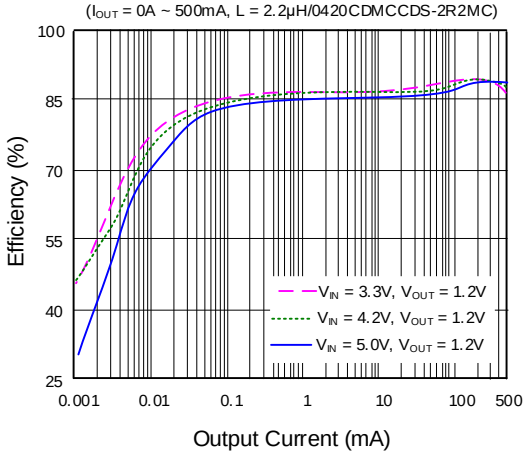
Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

(SY20011DFC, T_A = 25°C, V_{IN} = 5V, V_{OUT} = 1.8V, L = 2.2μH, C_{OUT} = 10μF, unless otherwise noted)

Efficiency vs. Output Current

(I_{OUT} = 0A ~ 500mA, L = 2.2μH/0420CDMCCDS-2R2MC)



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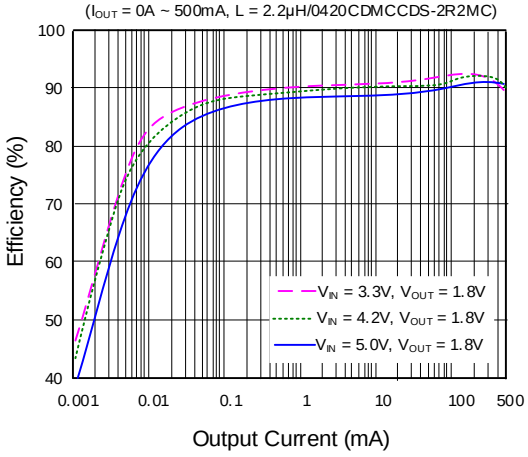
(I_{OUT} = 0A ~ 500mA, L = 2.2μH/0420CDMCCDS-2R2MC)



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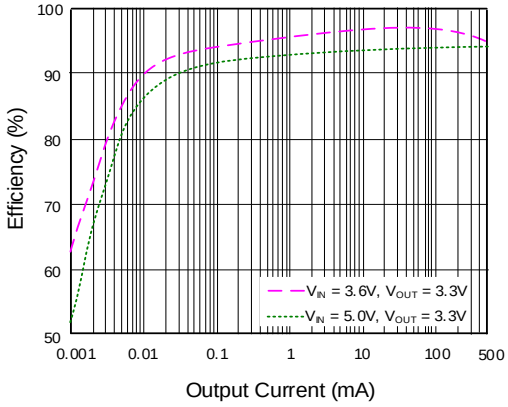
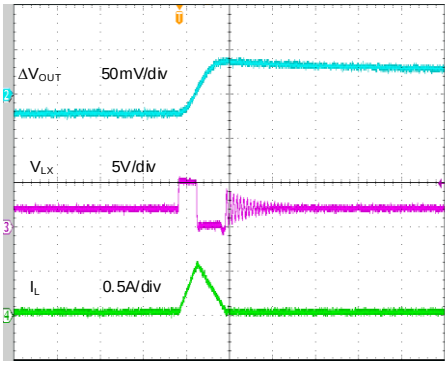
(I_{OUT} = 0A ~ 500mA, L = 2.2μH/0420CDMCCDS-2R2MC)



Output Ripple

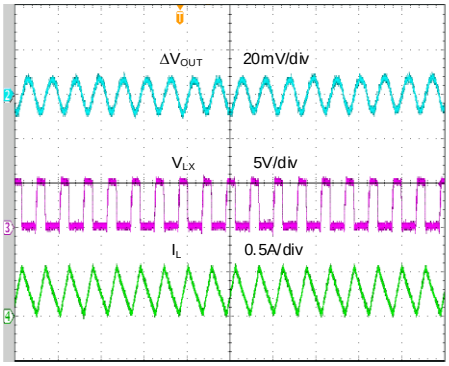
(V_{IN} = 5.0V, V_{OUT} = 1.8V, I_{OUT} = 0A)



Time 1μs/div)

Output Ripple

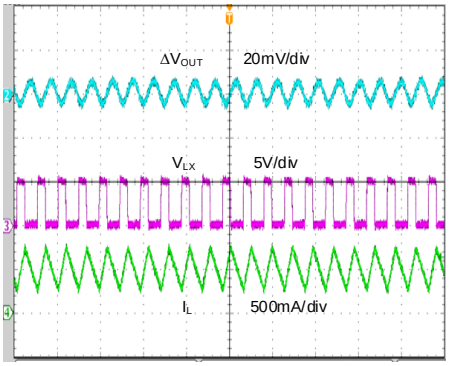
(V_{IN} = 5.0V, V_{OUT} = 1.8V, I_{OUT} = 250mA)



Time (2μs/div)

Output Ripple

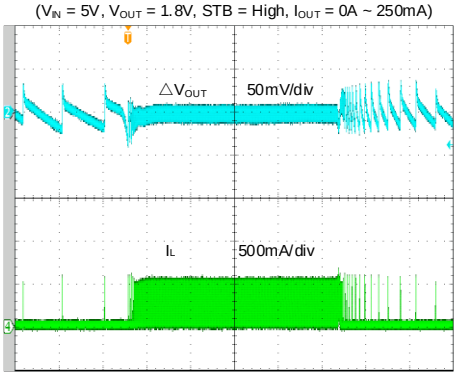
(V_{IN} = 5.0V, V_{OUT} = 1.8V, I_{OUT} = 500mA)



Time (1μs/div)

Load Transient

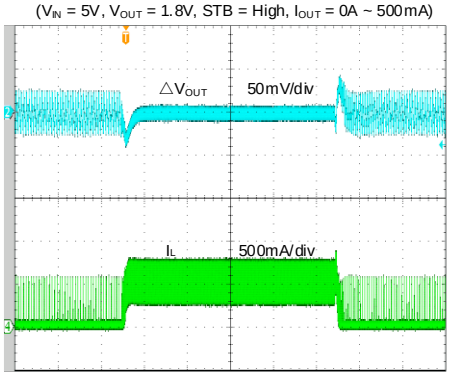
(V_{IN} = 5V, V_{OUT} = 1.8V, STB = High, I_{OUT} = 0A ~ 250mA)



Time (100μs/div)

Load Transient

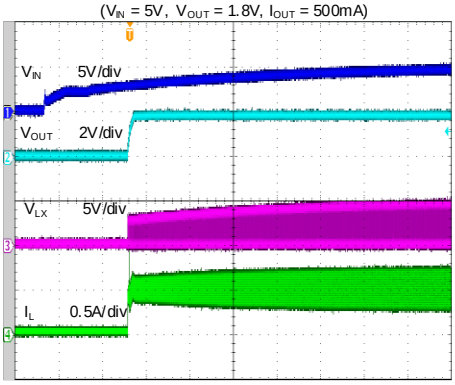
(V_{IN} = 5V, V_{OUT} = 1.8V, STB = High, I_{OUT} = 0A ~ 500mA)



Time (100μs/div)

Startup from V_{IN}

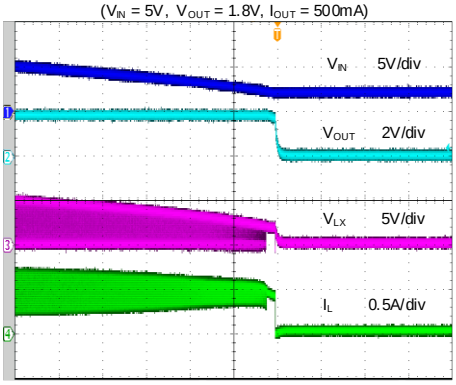
(V_{IN} = 5V, V_{OUT} = 1.8V, I_{OUT} = 500mA)



Time (800μs/div)

Shutdown from V_{IN}

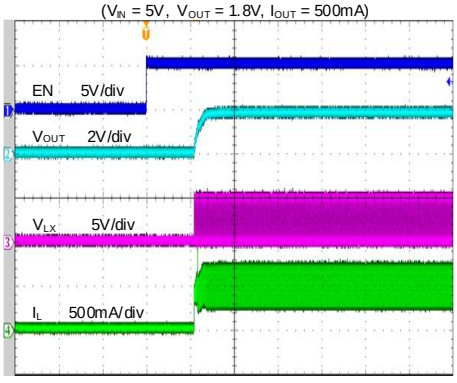
(V_{IN} = 5V, V_{OUT} = 1.8V, I_{OUT} = 500mA)



Time (800 μs/div)

Startup from Enable

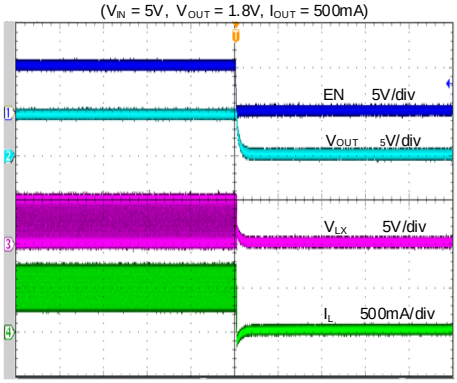
(V_{IN} = 5V, V_{OUT} = 1.8V, I_{OUT} = 500mA)



Time (400μs/div)

Shutdown from Enable

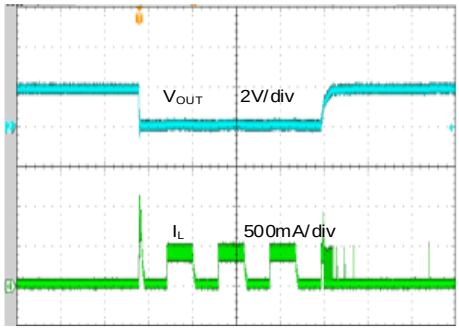
(V_{IN} = 5V, V_{OUT} = 1.8V, I_{OUT} = 500mA)



Time (400μs/div)

Short Circuit Protection

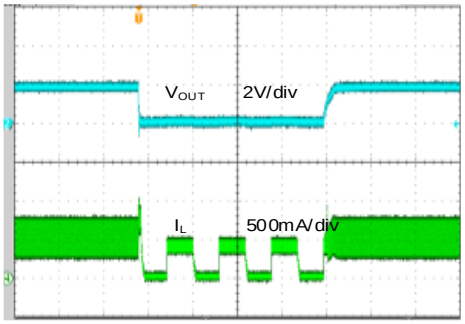
(V_{IN} = 5.0V, V_{OUT} = 1.8V,I_{OUT} = 0A ~ Short)



Time (400μs/div)

Short Circuit Protection

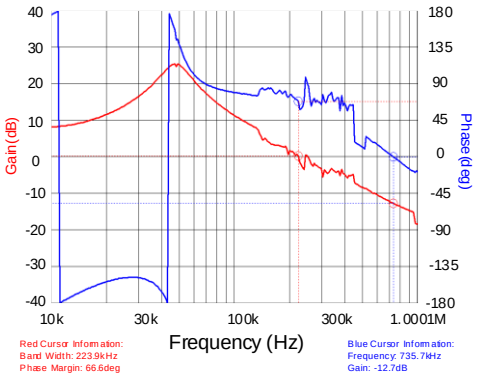
(V_{IN} = 5.0V, V_{OUT} = 1.8V,I_{OUT} = 500mA ~ Short)



Time (400μs/div)

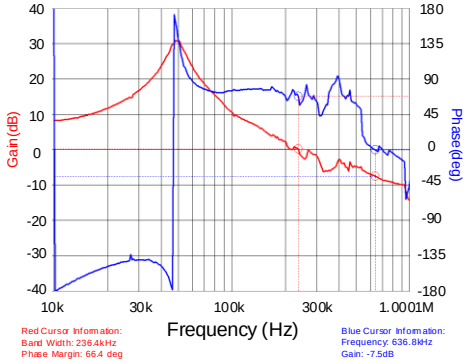
Bode Plot

(V_{IN} = 5.0V, V_{OUT} = 1.2V, I_{OUT} = 500mA)



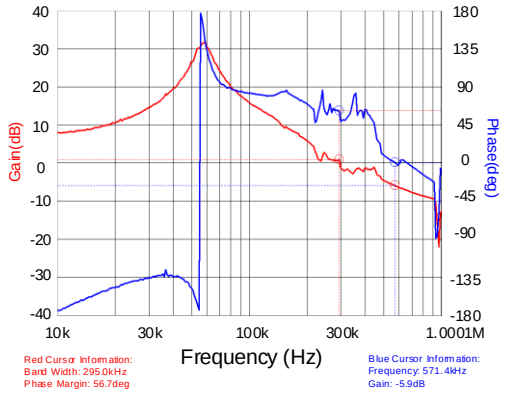
Bode Plot

(V_{IN} = 5.0V, V_{OUT} = 1.8V, I_{OUT} = 500mA)



Bode Plot

(V_{IN} = 5.0V, V_{OUT} = 3.3V, I_{OUT} = 500mA)



Detailed Description

The SY20011 is a high-efficiency 1MHz synchronous Buck converter capable of delivering up to 500mA output current. It can operate over a wide input voltage range from 2.2V to 5.5V, and integrates a top FET and bottom FET with very low $R_{DS(ON)}$ to minimize conduction loss.

Constant On-Time and Ripple-Based Control

The SY20011 adopts a constant on-time and ripple-based control strategy. The output voltage is fed back directly, and the inductor current ripple information obtained is constructed as a voltage ramp. When this ramp reaches internal V_{COMP}, the bottom FET will turn off and the top FET will turn on for a fixed period of time (constant t_{ON}). t_{ON} is internally calculated according to the input voltage, output voltage, and desired switching frequency (f_{SW}):

$$t_{ON} = \frac{V_{OUT}}{f_{SW} \times V_{IN}}$$

The top FET turns off after a period of t_{ON}. This instant-PWM architecture achieves fast transient response for high step-down applications and high efficiency at light loads.

Enable Control

The EN input is a high-voltage-capable input with logic-compatible threshold. When EN is driven higher than 1.1V, normal device operation is enabled. When driven to lower than 0.4V, the device will shut down, reducing input current to less than 0.1μA (max.).

Power-Good Indicator

The power-good indicator is an open-drain output controlled by a window comparator connected to the feedback signal. If V_{FB} is greater than $V_{PG,R}$ and less than V_{OVP} for at least the power-good delay time (low to high), PG will be high-impedance. Otherwise, it will be pulled low. PG should be connected to V_{IN} or another voltage source through a resistor (e.g.,10kΩ~100kΩ).

STB Pin Function

Two different quiescent current levels can be selected using the STB pin. If STB is set to logic high, the quiescent current is 15μA (typ.). If STB is set to logic low, the quiescent current can be decreased to 400nA, and an extra 3μs delay time is needed when the SY20011 wakes up from standby mode. As a side effect, the transient performance will be reduced, and the output undershoot will be higher under a fast load ramp.

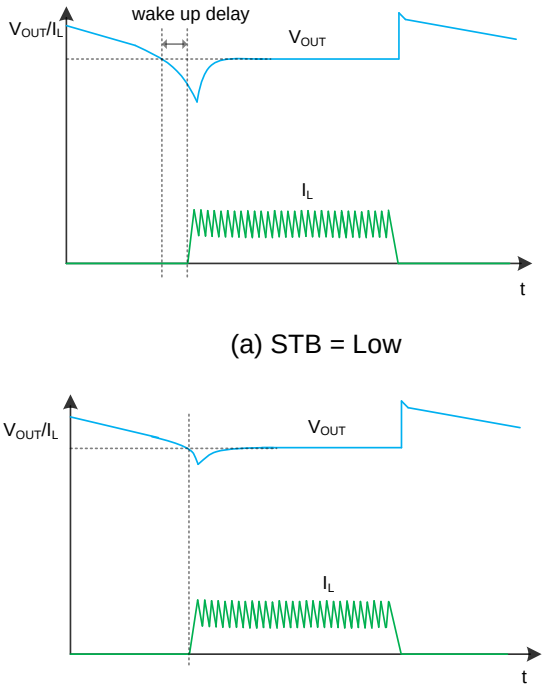


Figure 4. Load Transient Response

Bypass Mode

The SY20011 enters 100% bypass mode when the input voltage is close to the output voltage. Once the input voltage falls below the bypass threshold V_{TH-}, the SY20011 top FET turns on for bypass mode. Because the output is connected to the input, the output voltage tracks the input voltage minus the voltage drop across the internal top FET and inductor caused by the inductor current. When the input voltage increases and exceeds the bypass threshold V_{TH+}, the SY20011 will exit bypass mode. See Figure 5 for details.

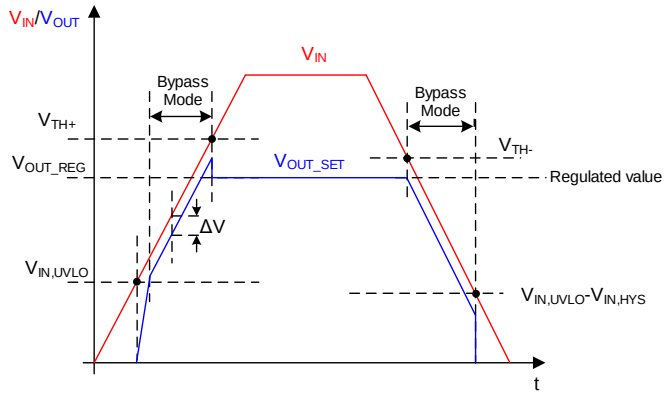


Figure 5. Bypass Mode Transition

V_{TH+}, V_{TH-}, and ΔV can be calculated as follows:

$$V_{TH+} = V_{OUT\_SET} \times 1.03\% + I_{OUT} \times (R_{DCR} + R_{DS(ON)1})$$

$$V_{TH-} = V_{OUT\_SET} + I_{OUT} \times (R_{DCR} + R_{DS(ON)1}$$

$$\Delta V = I_{OUT} \times (R_{DCR} + R_{DS(ON)1})$$

Fault-Protection Modes

Output Current Limit

With load current increasing, as soon as the top FET current exceeds the peak current limit threshold, the top FET will turn off and the bottom FET will turn on until the bottom FET current decreases below the bottom current limit threshold. If the top current limit is triggered twice, the valley current limit threshold will fold back to 65% to protect the device from being damaged.

Output Undervoltage Protection (UVP)

If V_{OUT} is less than 1V for approximately 20μs (when the output short-circuits or the load current is much higher than the maximum current capacity), the output undervoltage protection (UVP) will be triggered, and the device will enter the hiccup protection mode. The hiccup on-time is 0.25ms, and the hiccup off-time is 0.25ms. If the output fault conditions are removed, the device will return to normal operation after the subsequent hiccup off-time.

To avoid output overshoot, the internal soft-start circuit voltage V_{SS} will be pulled low temporarily when V_{FB} exceeds the UVP threshold with the output fault conditions removed during hiccup on-time, and then the V_{SS} will rise smoothly to ramp the output to the desired voltage during a new soft-start cycle.

Overtemperature Protection (OTP)

The SY20011 includes overtemperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. This will shut down the device when the junction temperature exceeds 150°C. Once the junction temperature cools by approximately 15°C, the device will resume normal operation after a complete soft-start cycle. For continuous operation, provide adequate cooling so that the junction temperature will not exceed the OTP threshold.

Application Information

The following paragraphs describe the selection process for the input capacitor C_{IN}, output capacitor C_{OUT}, output inductor L, and feedback resistors R_H and R_L.

Feedback Resistor-Divider R_H and R_L

Choose R_H and R_L to program the proper output voltage. A value between 10MΩ and 50MΩ is recommended for both resistors. If R_L is chosen as 20MΩ, then R_H can be calculated as follows:

$$R_H = \frac{(V_{OUT} - 1.2\,V) \times R_L}{1.2V}$$

Input Capacitor C_{IN}

For the best performance, select a typical X5R or a better grade ceramic capacitor with a 6.3V rating, and greater than 10μF capacitance. The capacitor should be placed as close as possible to the device, while also minimizing the loop area formed by C_{IN} and the IN/GND pins. When selecting an input capacitor, ensure that its voltage rating is at least 20% greater than the maximum voltage of the input supply. X5R or X7R dielectric types are the most often selected due to their small size, low cost, surge current capability, and high RMS current rating over a wide temperature and voltage range.

In situations where the input rail is supplied through long wires, it is recommended to add some bulk capacitance like electrolytic, tantalum or polymer type capacitors to

reduce the overshoot and ringing caused by the added parasitic inductance.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1-D)}$$

The worst-case condition occurs at D = 0.5, then

$$I_{CIN\_RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplicity, use an input capacitor with an RMS current rating greater than 50% of the maximum load current.

The input capacitor value determines the input voltage ripple of the converter. If there is a voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification.

Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated using the formula:

$$V_{CIN\_RIPPLE,CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1-D)$$

The worst-case condition occurs at D = 0.5, then

$$V_{CIN\_RIPPLE,CAP,MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. A single 10µF X5R capacitor is sufficient in most applications.

Output Inductor L

Consider the following when choosing this inductor:

1) Choose the inductance to provide a ripple current that is approximately 40% of the maximum output current. The recommended inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT} / V_{IN,MAX})}{f_{sw} \times I_{OUT,MAX} \times 0.4}$$

where f_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY20011 has high tolerance for ripple current amplitude variation. As a result, the final choice of inductance can vary slightly from the calculated value with no significant performance impact.

2) The inductor's saturation current rating must be greater than the peak inductor current under full load:

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{2 \times f_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. Use an inductor with DCR less than 50mΩ to achieve good overall efficiency.

Output Capacitor C_{OUT}

Select the output capacitor C_{OUT} to handle the output ripple requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting the component. For the best performance, use an X5R or a better grade ceramic capacitor with a 6.3V rating, and capacitance greater than 22µF.

For applications where the design must meet stringent ripple requirements, the following considerations must be followed:

The output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔI_L) on the output capacitor's ESR (ESR ripple), as well as the stored charge (capacitive ripple).

When calculating total ripple, consider both.

$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

The capacitive ripple might be higher because the effective capacitance for ceramic capacitors decreases with the voltage across the terminals. The voltage

derating is usually included as a chart in the capacitor datasheet, and the ripple can be recalculated after taking the target output voltage into account.

The recommended inductance and output capacitance are shown in Table 1.

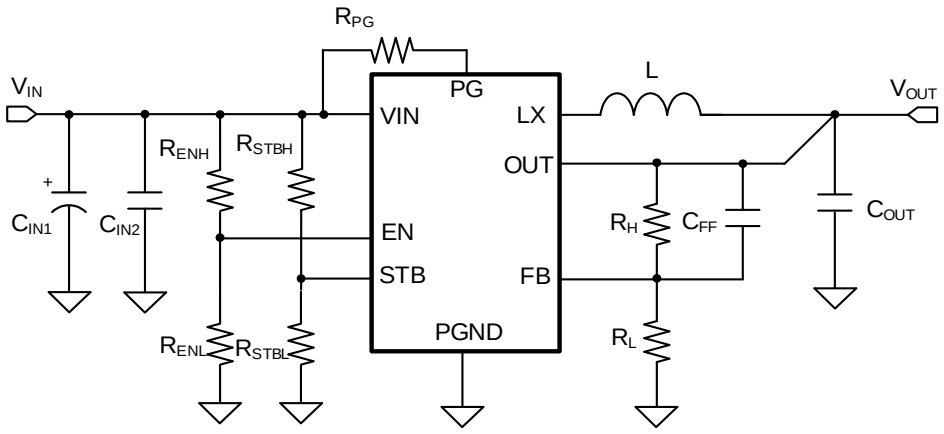
Table 1. Inductance vs. Output Capacitor Selection

L	C_{OUT}				
	10μF	22μF	80μF	120μF	350μF
2.2μH	✓	✓	✓	✓	✓
4.7μH	✓	✓	✓	✓	×
6.8μH	✓	✓	✓	×	×

Load Transient Considerations

The SY20011 integrates compensation components to achieve good stability and fast transient responses. In some applications, adding a ceramic capacitor (feedforward capacitor C_{FF}) in parallel with R_H may further speed up the load transient response. It is recommended for applications with large load transient step requirements.

Application Schematic (V_{OUT} = 1.8V)



BOM List

Reference Designator	Description	Part Number	Manufacturer
C_{IN1}	100μF/25V (electrolytic capacitor)		
C_{IN2}	10μF/6.3V, 0603, X5R	C1608X5R0J106M	TDK
C_{OUT}	10μF/6.3V, 0603, X5R	C1608X5R0J106M	TDK
C_{FF}	10pF/50V, 0603, C0G	C1608C0G1H100D	TDK
L	2.2μH	0420CDMCCDS-2R2MC	Sumida
R_H	10MΩ, 1%, 0603		
R_L	20MΩ, 1%, 0603		
R_{PG}	100kΩ, 1%, 0603		
R_{ENH}, R_{STBH}	1kΩ, 1%, 0603		
R_{ENL}, R_{STBL}	1MΩ, 1%, 0603		

Layout Design

Follow these PCB layout guidelines for optimal performance and thermal dissipation:

Input Capacitors: Place the input capacitors as close as possible to the IN and GND pins, minimizing the loop formed by these connections. The input capacitor should be connected to the IN and GND by wide copper plane.

Output Capacitors: Connect the C_{OUT} negative terminal to the GND pin using wide copper traces instead of vias, in order to achieve better accuracy and stability of output voltage.

Feedback Network: Place the feedback components (R_H, R_L, and C_{FF}) as close to the FB pin as possible. Avoid routing the feedback line near LX, or other high-frequency signals as it is noise-sensitive. Use a Kelvin connection to connect with C_{OUT} rather than the inductor output terminal.

LX Connection: Keep the LX area small to prevent excessive EMI, while providing a wide copper trace to minimize parasitic resistance and inductance.

Control Signals: It is not recommended to connect control signals directly to V_{IN}. A resistor in a range of 1kΩ to 1MΩ should be used if the lines are pulled high to V_{IN}.

GND Vias: Place an adequate number of vias on the GND layer around the device for better thermal performance. The exposed GND pad should be connected to a copper area larger than its size. Place multiple GND vias on it for heat dissipation.

PCB Board: To achieve the best thermal and noise performance, maximize the PCB copper area connecting to the GND pin. A ground plane is highly recommended if board space allows. Connect the ground pad to a large copper area to enhance thermal performance.

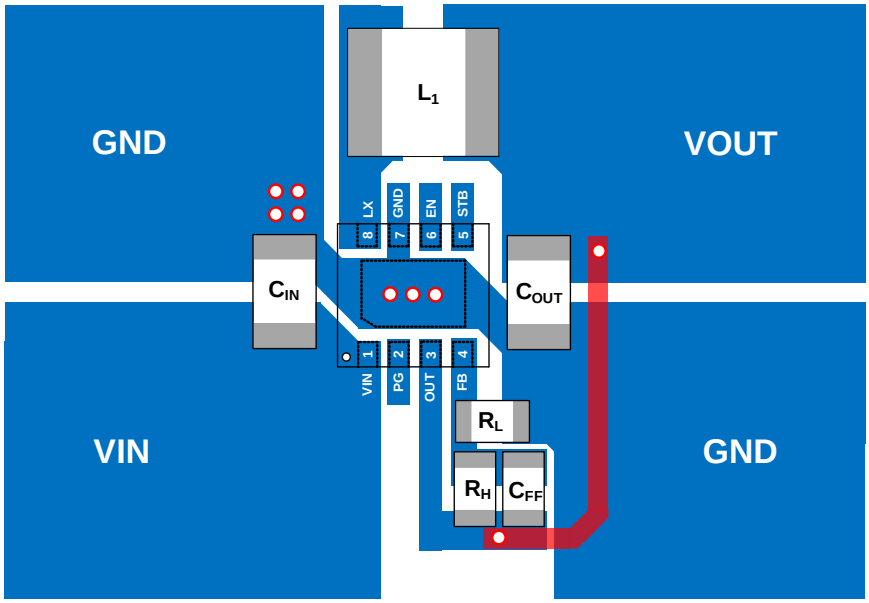
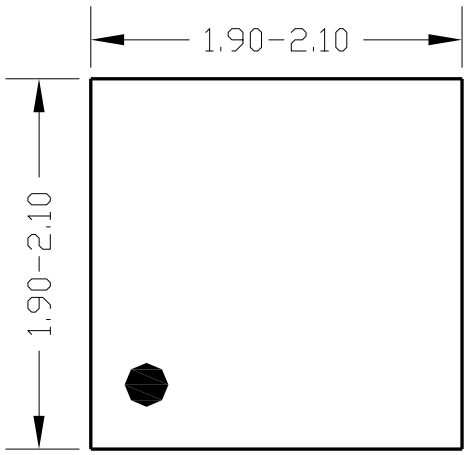
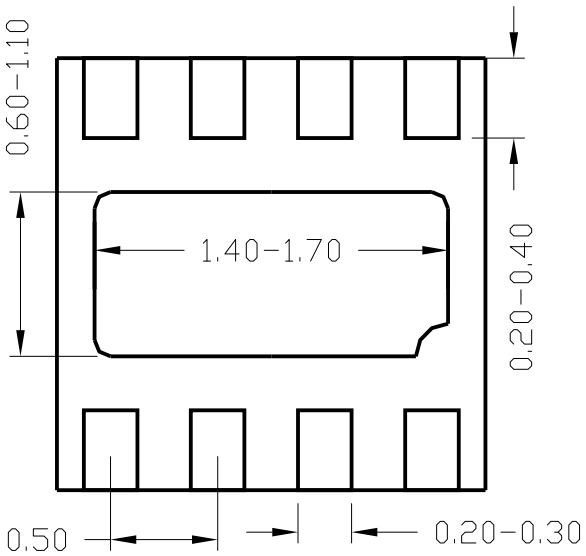


Figure 6. Suggested PCB Layout

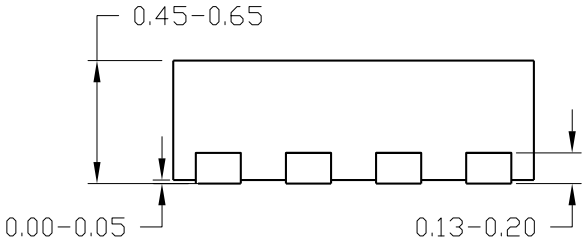
DFN2×2-8 Package Outline Drawing



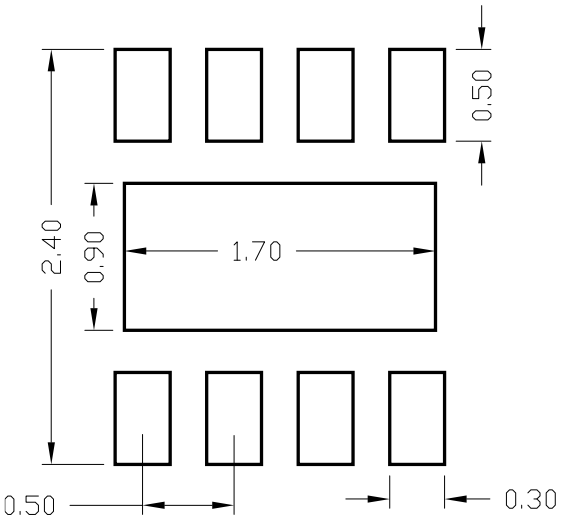
Bottom view



Top view



Side View

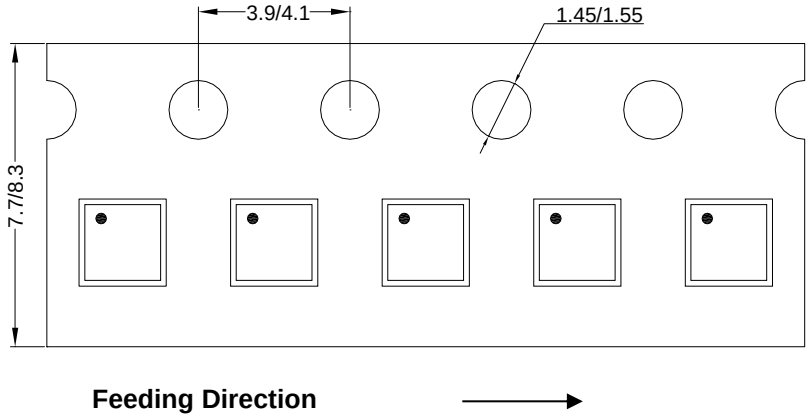


Recommended PCB layout
(Reference only)

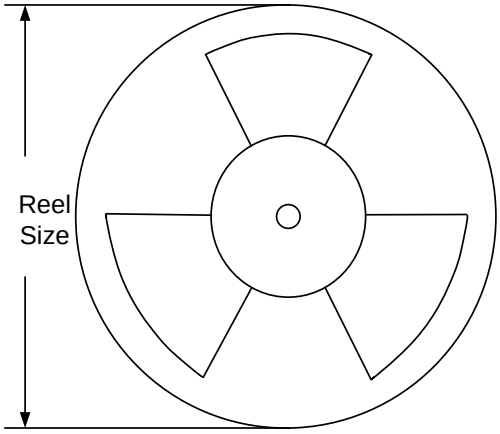
Note: *All dimensions are in millimeters and exclude mold flash and metal burr.*

Taping and Reel Specification

DFN2×2 Taping Orientation



Carrier Tape and Reel Specification for Packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel (pcs)
DFN2×2	8	4	7"	400	160	3000

Others: NA

Revision History

The revision history provided is for informational purposes only and is believed to be accurate; however, it is not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change
Jun. 11, 2020	Revision 0.9	Initial Release
Jun. 11, 2021	Revision 1.0	Production Release

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