SY20112

High-Efficiency, 5.5V, 3A, 1.2MHz Synchronous Step-Down Regulator

General Description

The SY20112 high-efficiency 1.2MHz synchronous step-down DC/DC regulator operates over a wide input voltage range of 2.5V to 5.5V and can deliver an output current up to 3A with a low quiescent current of 50μA. To minimize conduction loss, it integrates a main switch and a synchronous switch with very low $R_{DS(ON)}$.

The SY20112 adopts constant off-time and peak current mode control. The SY20112 is highly integrated, so only the input and output capacitors, inductor, and resistor-divider components need to be selected for the targeted application specifications.

The SY20112 is available in a space-saving, low-profile SOT563 package.

Features

- 2.5V~5.5V Input Voltage Range
- Up to 3A Output Current
- Constant Off-time and Peak Current Mode Control
- Low $R_{DS(ON)}$ for Internal Switches: 100mΩ Top, 60mΩ Bottom
- Low 50μA Quiescent Current
- High 1.2MHz Switching Frequency Minimizes Required External Components
- Internal Soft-Start Limits Inrush Current
- 100% Dropout Operation
- Power-Good Indicator
- Hiccup Mode for Short-Circuit Protection
- Output Auto-Discharge Function
- RoHS-Compliant and Halogen-Free
- Compact SOT563 Package

Applications

- Set-Top Box
- USB Dongle
- Media Player
- Smartphone

Typical Application

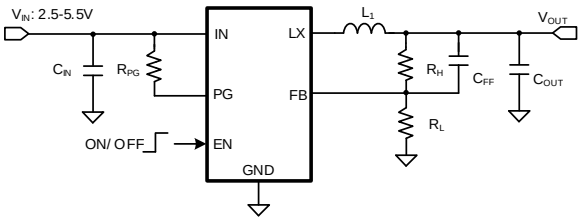


Figure 1. Schematic Diagram

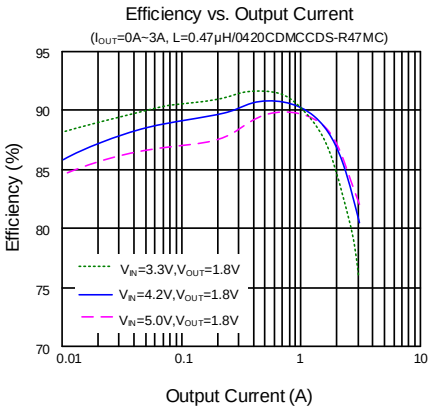


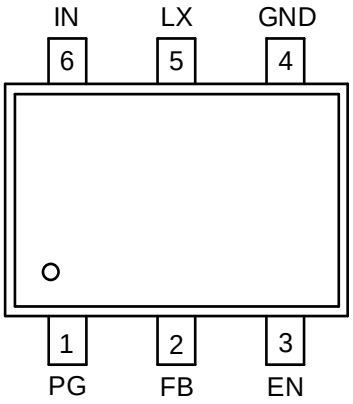
Figure 2. Efficiency vs. Output Current

Ordering Information

Ordering Part Number	Package type	Top Mark
SY20112ARC	SOT-563 RoHS-Compliant, Halogen-Free	**fQ*xyz***

x = year code, y = week code, z = lot number code

Pinout (top view)



Pin Description

Pin No	Pin Name	Pin Description
1	PG	Power-good indicator (open-drain output). The PG pin is high-impedance if the output is between 90% and 120% of the regulation voltage; otherwise, it is driven low. Connect a pull up resistor to the input.
2	FB	Output Feedback Pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{OUT}=0.6\times(1+R_H/R_L)$.
3	EN	Enable control pin. Pull high to turn on. Do not leave floating.
4	GND	Ground pin.
5	LX	Inductor pin. Connect this pin to the switching node of the inductor.
6	IN	Input pin. Decouple this pin from the GND pin with a minimum 10μF ceramic capacitor.

Block Diagram

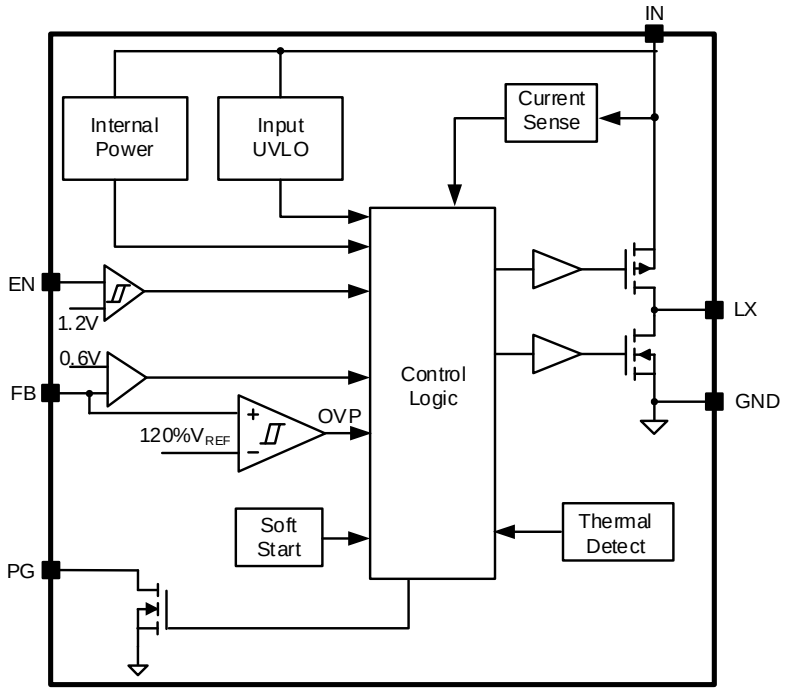


Figure 3. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
IN	-0.3	6	V
EN, FB, PG	-0.3	IN + 0.6	
LX	-0.3	6	
LX, 40ns duration	-3	7	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering,10s)		260	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	70	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	8	
P_D Power Dissipation T_A = 25°C	1.4	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
IN	2.5	5.5	V
Output Voltage	0.6	5.5	
Output Current		3	A
Junction Temperature	-40	125	°C

Electrical Characteristics

(V_{IN} = 5V, V_{OUT} = 1.8V, L = 0.47μH, C_{OUT} = 22μF, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input	Voltage	V_{IN}		2.5		5.5	V
	UVLO, rising	$V_{IN,UVLO}$				2.5	V
	UVLO, hysteresis	$V_{IN,HYS}$			150		mV
	Quiescent current	I_Q	V_{FB} = 105% × V_{REF}		50	70	uA
	Shutdown current	I_{SHDN}	V_{EN} = 0V		0.1	1	μA
Output	Reference voltage	V_{REF}	I_{OUT} = 1A, CCM	0.591	0.6	0.609	V
	FB input current	I_{FB}	V_{EN} = 2V, V_{FB} = 1V	-50	0	50	nA
	Turn-on delay time	$t_{ON,DLY}$	From EN high to LX start switching		0.3		ms
	Soft-start time	t_{SS}	V_{OUT} from 0% to 100%		0.7		ms
	UVP threshold	V_{UVP}			50		%V_{REF}
	UVP delay	$t_{UVP,DLY}$			10		μs
	UVP hiccup on time	$t_{HICCUP,ON}$			1.45		ms
	UVP hiccup off time	$t_{HICCUP,OFF}$			1.45		ms
	Discharge on resistance	R_{DIS}			60		Ω
MOSFET	Top FET $R_{DS(ON)}$	$R_{DS(ON)1}$			125		mΩ
	Bottom FET $R_{DS(ON)}$	$R_{DS(ON)2}$			100		mΩ
	Top FET Current Limit	$I_{LMT,TOP}$		3			A
Enable (EN)	Input voltage high	$V_{EN,H}$		1.2			V
	Input voltage low	$V_{EN,L}$				0.4	V
	Input current	I_{EN}	V_{EN} = 2V			2	μA
Power-Good	Thresholds	$V_{PG,R}$	V_{FB} rising, good		90		%
		$V_{PG,F}$	V_{FB} rising, fault		120		%
	Delay	$t_{PG,R}$	V_{FB} rising, good		2		μs
		$t_{PG,F}$	V_{FB} falling, fault		20		μs
COT	Switching frequency	f_{SW}	I_{OUT} = 1A, CCM		1.2		MHz
	Minimum on-time	$t_{ON,MIN}$			60		ns
	Maximum duty cycle	D_{MAX}		100			%
OTP	Temperature	T_{OTP}			160		°C
	Temperature Hysteresis	T_{HYS}			20		°C

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} of SY20112ARC is measured in the natural convection at T_A = 25°C on a 2OZ two-layer Silergy evaluation board. Pin 5 is the case position for SY20112ARC θ_{JC} measurement.

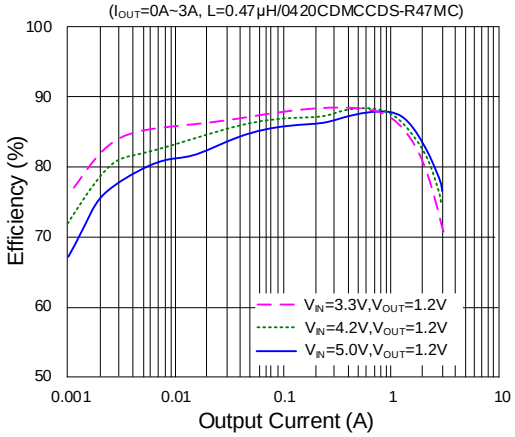
Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

(SY20112ARC, T_A = 25°C, V_{IN} = 5V, V_{OUT} = 1.8V, L = 0.47μH, C_{OUT} = 22μF, unless otherwise noted)

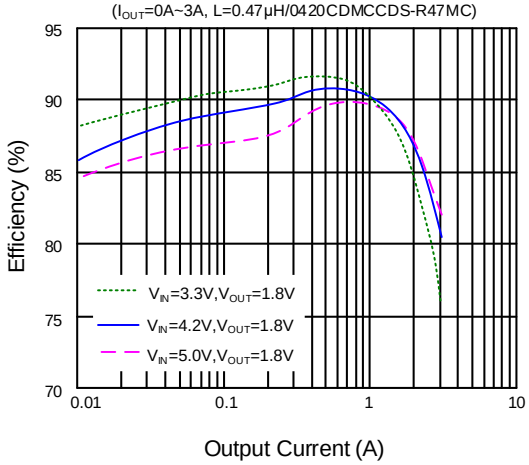
Efficiency vs. Output Current

(I_{OUT}=0A~3A, L=0.47μH/0420CDMCCDS-R47MC)



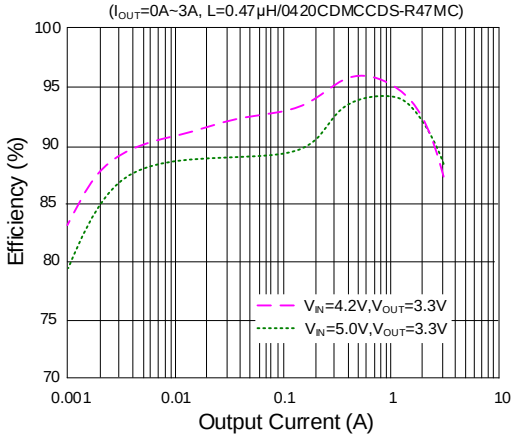
Efficiency vs. Output Current

(I_{OUT}=0A~3A, L=0.47μH/0420CDMCCDS-R47MC)



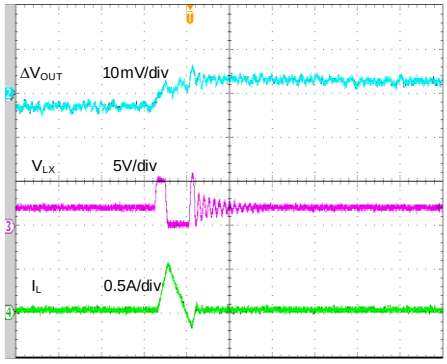
Efficiency vs. Output Current

(I_{OUT}=0A~3A, L=0.47μH/0420CDMCCDS-R47MC)



Output Ripple

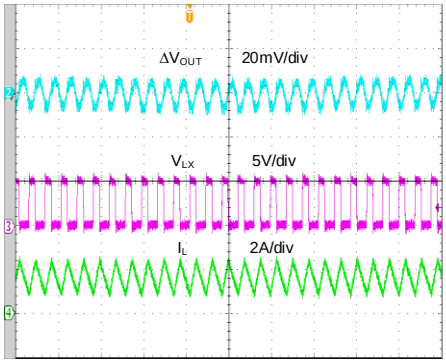
(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=0A)



Time (400ns/div)

Output Ripple

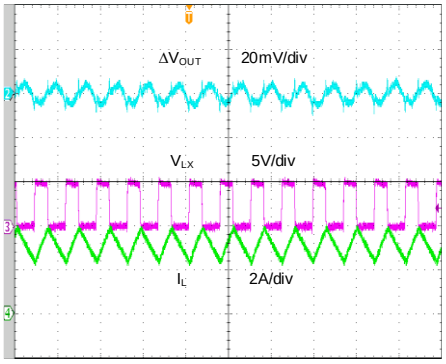
(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=1.5A)



Time (2μs/div)

Output Ripple

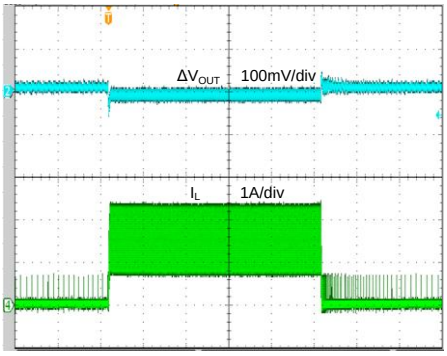
(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=3A)



Time (1μs/div)

Load Transient

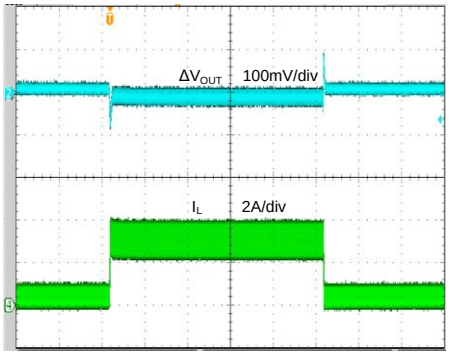
(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=0A ~ 1.5A)



Time (400μs/div)

Load Transient

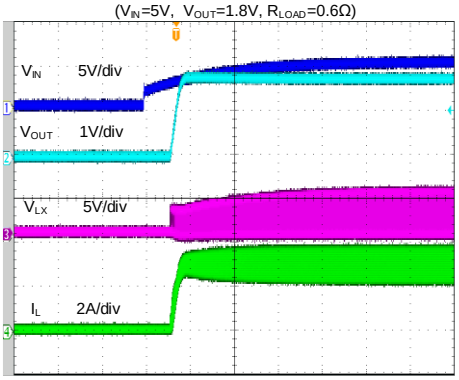
(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=0.3A ~ 3A)



Time (400μs/div)

Startup from V_{IN}

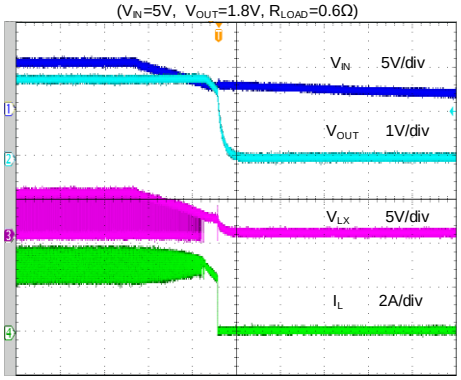
(V_{IN}=5V, V_{OUT}=1.8V, R_{LOAD}=0.6Ω)



Time (2ms/div)

Shutdown from V_{IN}

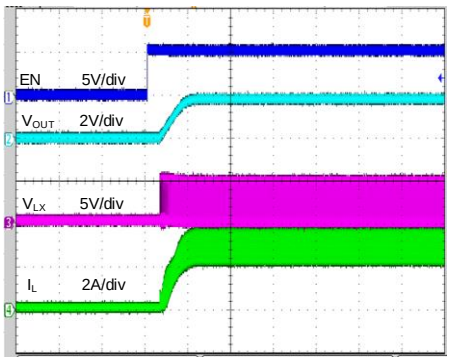
(V_{IN}=5V, V_{OUT}=1.8V, R_{LOAD}=0.6Ω)



Time (100μs/div)

Startup from Enable

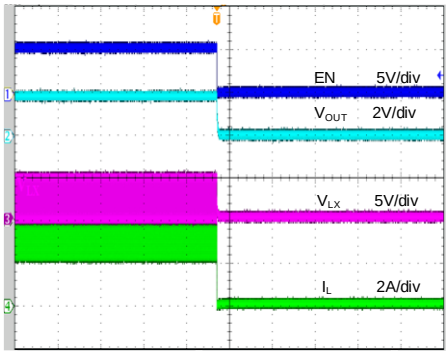
(V_{IN}=5.0V, V_{OUT}=1.8V, R_{LOAD}=0.6Ω)



Time (800μs/div)

Shutdown from Enable

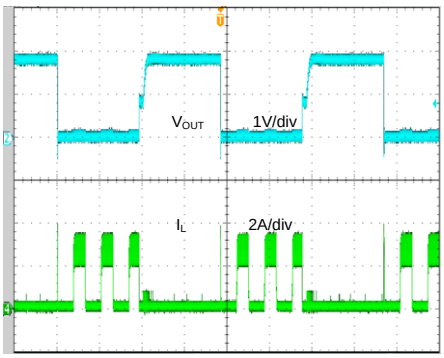
(V_{IN}=5.0V, V_{OUT}=1.8V, R_{LOAD}=0.6Ω)



Time (800μs/div)

Short Circuit Protection

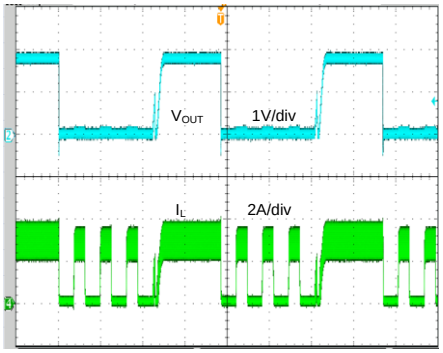
(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=0A ~ Short)



Time (4ms/div)

Short Circuit Protection

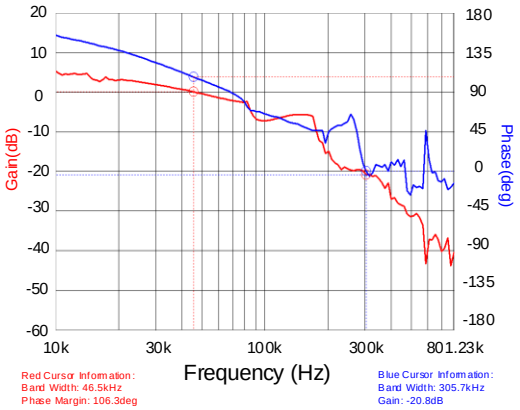
(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=3A ~ Short)



Time (4ms/div)

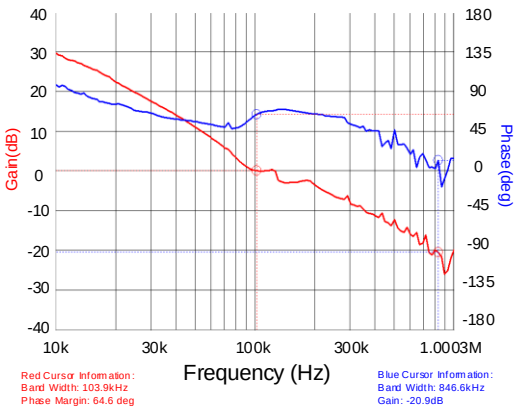
Bode Plot

(V_{IN}=5V, V_{OUT}=1.2V, I_{OUT}=3A)



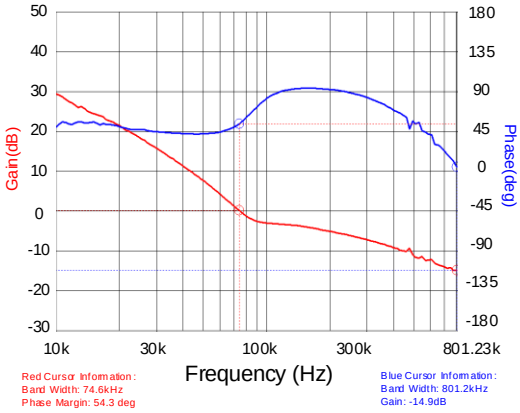
Bode Plot

(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=3A)



Bode Plot

(V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=3A)



Detailed Description

The SY20112 high-efficiency 1.2MHz synchronous step-down DC/DC regulator operates over a wide input-voltage range of 2.5V to 5.5V and can deliver an output current up to 3A with a low quiescent current of 50 μA. To minimize conduction loss, it integrates a main switch and a synchronous switch with very low $R_{DS(ON)}$.

Constant-off-time Architecture

The SY20112 employs a constant-off-time and peak-current-mode control strategy. When the top FET's current-sense signal reaches internal V_{COMP}, the top FET turns off and the bottom FET turns on for a fixed period of time (constant t_{OFF}). t_{OFF} is internally calculated according to the input voltage, output voltage, and desired switching frequency (f_{SW}):

$$t_{OFF} = \frac{1 - V_{OUT}/V_{IN}}{f_{SW}}$$

The bottom FET turns off after a period of t_{OFF}.

Enable Control

The EN input is a high-voltage capable input with logic-compatible threshold. When EN is driven above 1.2V, normal device operation is enabled. When driven to less than 0.4V, the device will shut down, reducing input current to less than 2μA.

Output Power-Good Indicator

The power good indicator is an open drain output controlled by a window comparator connected to the feedback signal. If V_{FB} is greater than $V_{PG,R}$ and less than V_{OVP} for at least the power good delay time (low to high), PG will be high-impedance. Otherwise, it is pulled low. PG should be connected to V_{IN} or a voltage source through a resistor (e.g., 10kΩ~100kΩ).

Fault Protection Modes

Output Current Limit

With load current increasing, as soon as the high-side FET current exceeds the peak current-limit threshold, the high-side FET will turn off. If the load current continues to increase, the output voltage will drop.

Output Under Voltage Protection (UVP)

If V_{OUT} is less than approximately 50% of the target output voltage for 10μs when the output short circuits or the load current is much higher than the maximum current capacity, the output under voltage protection (UVP) will be triggered, and the device will enter into hiccup protection mode. The hiccup on-time is 1.45ms, and the hiccup off-time is 1.45ms. If the output fault condition is removed, the device will return to normal operation in the subsequent hiccup on time.

To avoid output overshoot, the internal soft-start circuit voltage V_{SS} is pulled low temporarily when V_{FB} exceeds the UVP threshold if the output fault conditions are removed during hiccup on-time, and then the V_{SS} rises smoothly to ramp the output to the desired voltage during a new soft-start cycle.

Output Overvoltage Protection (OVP)

If the output voltage rises above the feedback regulation level, the high-side power switch naturally remains off, and the low-side synchronous rectifier remains on until the inductor current reaches zero and the switching actions are suppressed. The switching actions are resumed once the feedback is lower than the reference voltage.

Over Temperature Protection (OTP)

Instant-PWM includes over temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The device will shutdown when the junction temperature exceeds 160°C. Once the junction temperature cools by approximately 20°C, the device will resume normal operation after a complete soft-start cycle. For continuous operation, provide adequate cooling so that the junction temperature does not exceed the OTP threshold.

Application Information

The SY20112 is highly integrated, so only the following components need to be selected for the targeted application specifications: input capacitor C_{IN}, output capacitor C_{OUT}, output inductor L, and feedback resistors R_H and R_L.

Feedback Resistor-Divider R_H and R_L

Choose R_H and R_L to program the proper output voltage. A value between 1kΩ and 1MΩ is recommended for both resistors. If R_L is chosen as 120kΩ, then R_H can be calculated as follows:

$$R_H = \frac{(V_{OUT} - 0.6\,V) \times RL}{0.6V}$$

Input Capacitor C_{IN}

For the best performance, select a typical X5R or better grade ceramic capacitor with a 10V rating, and greater than 10μF capacitance. The capacitor should be placed as close as possible to the device, while also minimizing

the loop area formed by C_{IN} and the IN/GND pins. When selecting an input capacitor, ensure that its voltage rating is at least 20% greater than the maximum voltage of the input supply. X5R or X7R dielectric types are the most often selected due to their small size, low cost, surge current capability, and high RMS current rating over a wide temperature and voltage range.

In situations where the input rail is supplied through long wires, it is recommended to add some bulk capacitance like electrolytic, tantalum or polymer type capacitors to reduce the overshoot and ringing caused by the added parasitic inductance.
Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1-D)}$$

The worst-case condition occurs at D = 0.5, then

$$I_{CIN\_RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.
The input capacitor value determines the input voltage ripple of the converter. If there is a voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification.
Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated using the formula:

$$V_{CIN\_RIPPLE,CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1-D)$$

The worst-case condition occurs at D = 0.5, then

$$V_{CIN\_RIPPLE,CAP,MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. A single 10µF X5R capacitor is sufficient in most applications.

Output Inductor L
There are several considerations in choosing this inductor:

1) Choose the inductance to provide a ripple current that is approximately 40% of the maximum output current. The recommended inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{f_{sw} \times I_{OUT,MAX} \times 0.4}$$

where f_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

2) The saturation current rating of the inductor must be greater than the peak inductor current under full-load conditions:

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{2 \times f_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is recommended to choose an inductor with DCR less than 50mΩ to achieve good overall efficiency.

Output Capacitor C_{OUT}
Select the output capacitor C_{OUT} to handle the output ripple requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting the component. For the best performance, use an X5R or better grade ceramic capacitor with a 6.3V rating, and capacitance greater than 22µF.
For applications where the design must meet stringent ripple requirements, the following considerations must be followed:
The output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔI_L) on the output capacitor's ESR (ESR ripple), as well as the stored charge (capacitive ripple).
When calculating total ripple, consider both.

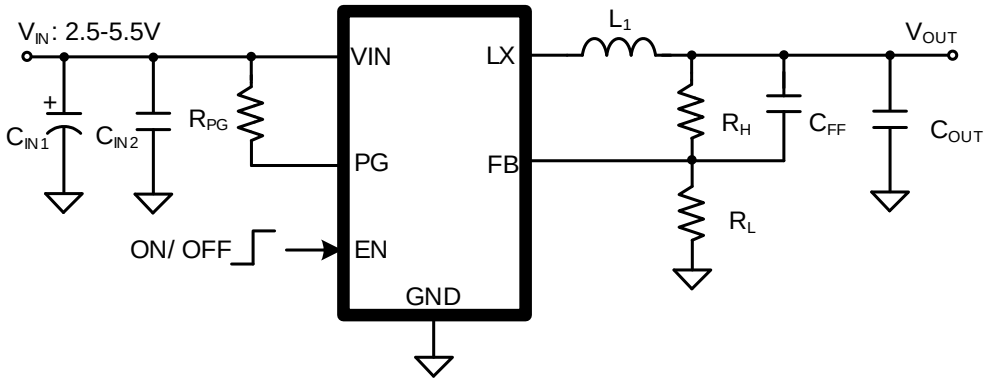
$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

The capacitive ripple might be higher because the effective capacitance for ceramic capacitors decreases with the voltage across the terminals. The voltage derating is usually included as a chart in the capacitor datasheet, and the ripple can be recalculated after taking the target output voltage into account.

Load-Transient Considerations
The SY20112 integrates the compensation components to achieve good stability and fast transient responses. In some applications, adding a ceramic capacitor (feed-forward capacitor C_{FF}) in parallel with R_H may further speed up the load-transient responses, and is therefore recommended for applications with large load-transient step requirements.

Application Schematic (V_{OUT} = 1.8V)



BOM List

Reference Designator	Description	Part Number	Manufacturer
L_1	0.47µH	0420CDMCCDS-R47MC	Sumida
C_{IN1}	100µF/25V(electrolytic capacitor)		
C_{IN2}	22µF/6.3V, 0805, X5R	C2012X5R0J226M	TDK
C_{OUT}	22µF/6.3V, 0805, X5R	C2012X5R0J226M	TDK
C_{FF}	22pF/50V, 0603, C0G	C1608C0G1H220J	TDK
R_H	100kΩ, 1%, 0603		
R_L	49.9kΩ, 1%, 0603		
R_{PG}	100kΩ, 0603		

Recommended Component Values for Typical Applications

V_{OUT}(V)	R_H(kΩ)	R_L(kΩ)	C_{FF}(pF)	L/(Rated/Saturating Current)	C_{OUT}
1.2	49.9	49.9	22	0.47µH/(8.1A/11A)	22µF/6.3V, 0805, X5R
1.8	100	49.9	22	0.47µH/(8.1A/11A)	22µF/6.3V, 0805, X5R
3.3	100	22.1	22	0.47µH/(8.1A/11A)	22µF/6.3V, 0805, X5R

Layout Design

Follow these PCB layout guidelines for optimal performance and thermal dissipation:

- **Input Capacitors:** Place the input capacitors very close to IN and GND pins, minimizing the loop formed by these connections. The input capacitor should be connected to the IN and GND by wide copper plane.
- **Output Capacitors:** Connect the C_{OUT} negative terminal to the GND pin using wide copper traces instead of vias, in order to achieve better accuracy and stability of output voltage.
- **Feedback Network:** Place the feedback components (R1, R2, and C_{FF}) as close to the FB pin as possible. Avoid routing the feedback line near LX, or other high-frequency signals as it is noise-sensitive. Use a Kelvin connection to connect with C_{OUT} rather than the inductor output terminal.
- **LX Connection:** Keep the LX area small to prevent excessive EMI, while providing a wide copper trace to minimize parasitic resistance and inductance.
- **Control Signals:** It is not recommended to connect control signals directly to V_{IN}. A resistor in a range of 1kΩ to 1MΩ should be used if the lines are pulled high to V_{IN}.
- **GND Vias:** Place an adequate number of vias on the GND layer around the device for better thermal performance. The exposed GND pad should be connected to a copper area larger than its size. Place four GND vias on it for heat dissipation.
- **PCB Board:** To achieve the best thermal and noise performance, maximize the PCB copper area connecting to the GND pin. A ground plane is highly recommended if board space allows. Connect the ground pad to a large copper area to enhance thermal performance.

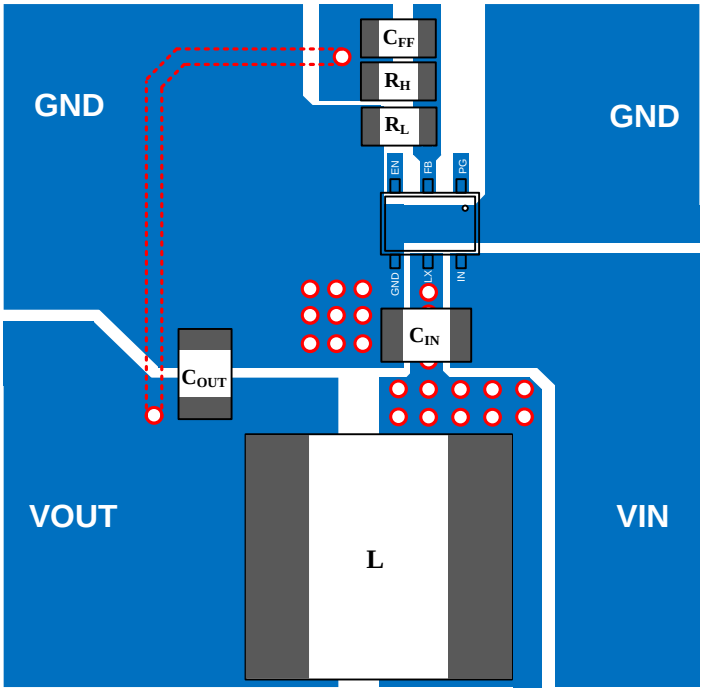
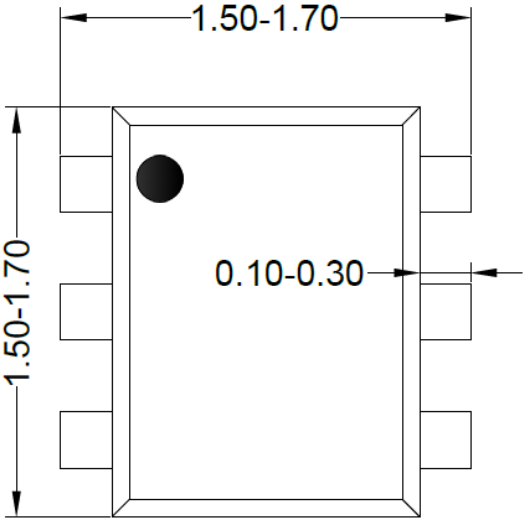
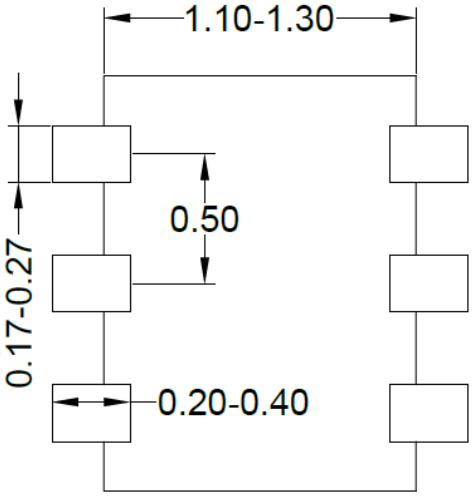


Figure 3. Suggested PCB Layout

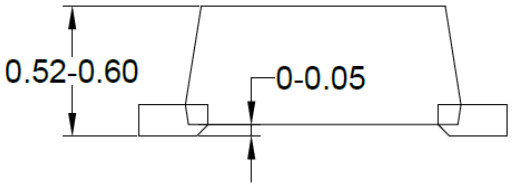
SOT563 Package Outline Drawing



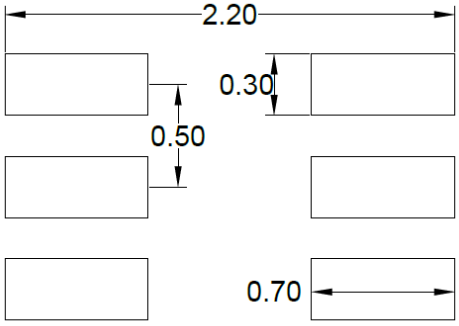
Top view



Bottom view



Side View



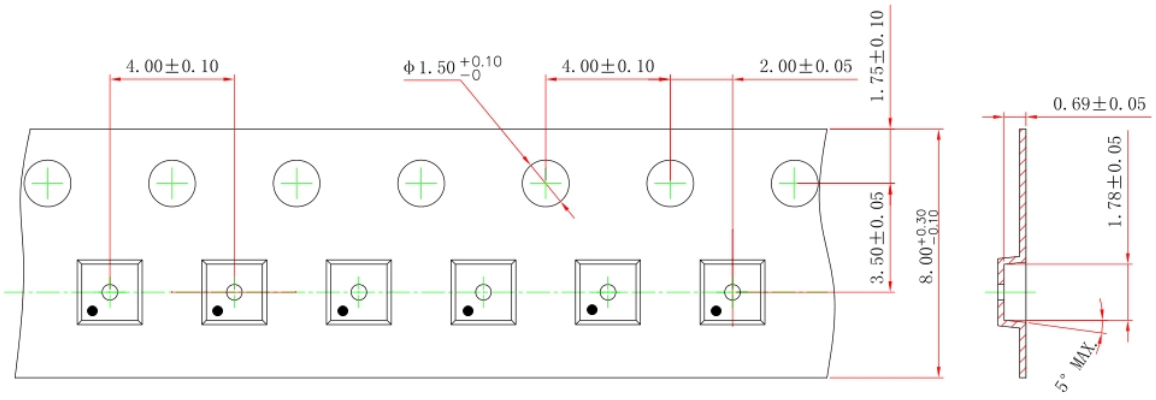
Recommended PCB layout (Reference only)

Note: *All dimensions are in millimeters and exclude mold flash and metal burr.*

Taping and Reel Specification

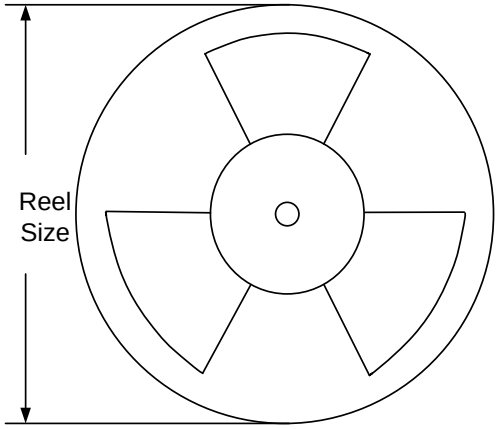
Taping Orientation

SOT563



Feeding Direction ⟶

Carrier Tape and Reel Specification for Packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel (pcs)
SOT563	8	4	7"	280	160	5000

Others: NA

Revision History

The revision history provided is for informational purposes only and is believed to be accurate; however, it is not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change
Jun. 11, 2020	Revision 0.9	Initial Release
Jun. 11, 2021	Revision 1.0	Production Release

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