SY20518

High Efficiency, 1MHz, 2A, Buck-Boost DC/DC Regulator

General Description

The SY20518 is a 2.6V to 5.5V input voltage range, high efficiency, fixed frequency Buck-Boost converter that can provide up to 2A of continuous current to a load that requires a voltage below equal or above the input voltage. The converter can provide power for system powered by either a two-cell or three-cell alkaline, Ni-Cd or Ni-MH batteries, or a single cell Li-Ion or Li-polymer battery.

The SY20518 is based on a fixed frequency, pulse-width-modulation (PWM) controller using synchronous rectification to obtain maximum efficiency. The output voltage and compensation circuit can be programmed using an external RC network.

The part automatically transitions to PFM mode under light load conditions, to maintain high efficiency across the entire load range.

During shutdown, the load is disconnected from the battery and the part only consumes 0.1μA of current (typ.).

The device is available in a 2 mm ×3 mm QFN package.

Features

- 2.6V to 5.5V Input Voltage Range
- 2A Continuous Output Current Capability
- Adjustable Output Voltage between 2.6V and 3.8V Independent of the Input Voltage
- 1 MHz (typ.) Fixed Frequency Operation
- Four low R_{DSON} Internal Power Switches
- Seamless Buck-Boost Transition
- Output Disconnect During Shutdown
- Power Good Indicator
- Built In Thermal Shut Down Protection, Hard Short Protection

Applications

- Handheld Instruments
- MP3/MP4 Players
- Digital Cameras/Camcorders
- Personal Medical Products
- High Power LED's
- Two-cell and three-cell alkaline, Ni-Cd or Ni-MH or single cell Li battery powered products

Typical Applications

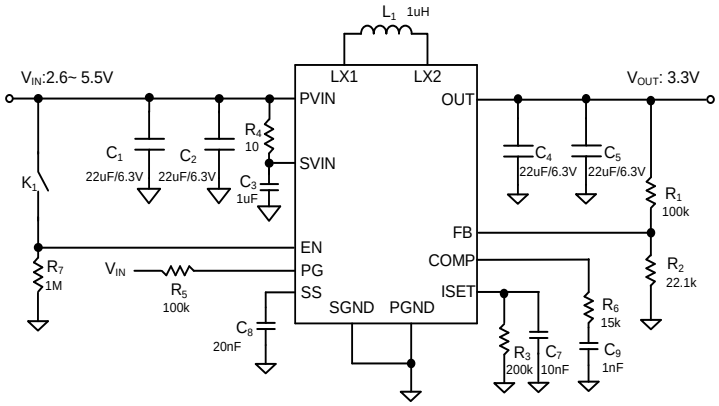


Figure 1. Schematic diagram

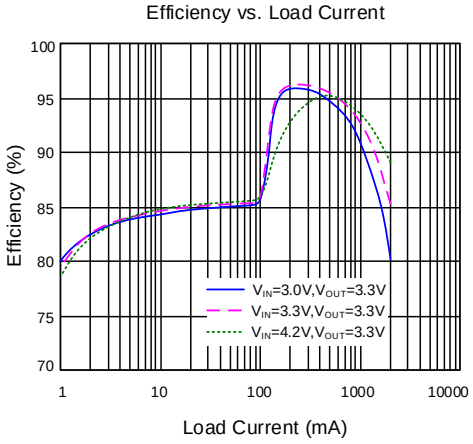


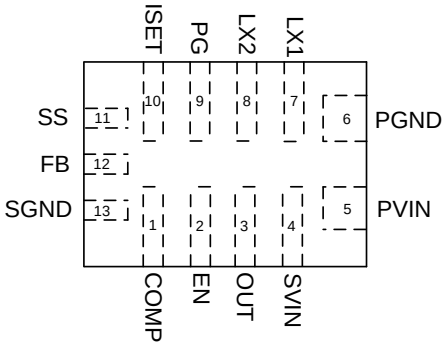
Figure2. Efficiency vs. Output Current

Ordering Information

Ordering Part Number	Package Type	Top Mark
SY20518QOC	QFN2×3-13 RoHS Compliant and Halogen Free	**ZN*xyz***

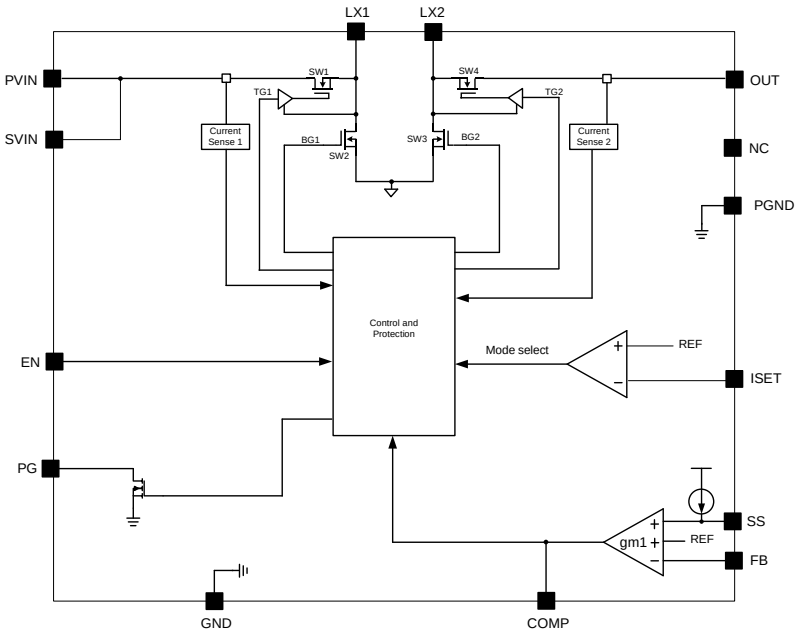
x=year code, y=week code, z= lot number code

Pinout (top view)



Pin Name	Pin Number	Function description
COMP	1	External compensation for voltage loop.
EN	2	Enable control. Pull high to turn on. Internal 1MΩ pull-down resistor.
OUT	3	Output of the synchronous rectifier. Decouple this pin to GND with at least a 22µF ceramic capacitor. Minimize the loop area formed by output capacitor, the OUT pin and GND pins.
SVIN	4	Signal power input pin. Decouple this pin to GND with at least a 1µF ceramic capacitor.
PVIN	5	Power input pin. Decouple this pin to GND with at least a 22µF ceramic capacitor. Minimize the loop area formed by input capacitor, the PVIN pin and GND paddles.
PGND	6	Power ground pin.
LX1	7	Inductor connection 1 Connect this node to the switching node of the inductor.
LX2	8	Inductor connection 2. Connect this node to the switching node of the inductor.
PG	9	Power good open-drain output.
ISET	10	Use a resistor and capacitor parallel network to sense the output average current. When V_{ISET} is lower than 0.2V, the converter will go into PFM mode. Do not let it float. Tie to ground for forced PWM operation.
SS	11	Connect this pin to a soft-start capacitor to program the soft-start time.
FB	12	Output feedback pin. Connect this pin to the center point of the output resistor divider to program the output voltage.
SGND	13	Signal ground pin.

Block Diagram



Absolute Maximum Ratings

Parameter (1)	Min	Max	Unit
OUT	-0.3	4	V
COMP, EN, PVIN, SVIN, FB, SS, ISET, PG, LX1, LX2	-0.3	6	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering, 10sec.)		260	
Storage Temperature	-65	150	

Thermal Information

Parameter (2)	Typ	Unit
θ_{JA} Junction-to-ambient Thermal Resistance	40	°C/W
θ_{JC} Junction-to-case Thermal Resistance	18	
P_D Power Dissipation T_A=25°C	3	W

Recommended Operating Conditions

Parameter (3)	Min	Max	Unit
PVIN, SVIN	2.6	5.5	V
OUT	2.6	3.8	
Junction Temperature, Operating	-40	125	°C
Ambient Temperature	-40	85	

Electrical Characteristics

(V_{IN} = 4.2V, V_{OUT} = 3.3V, L =1μH, C_{OUT} = 22uFx2, T_A = 25°C, I_{OUT} = 1A unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.6		5.5	V
Output Voltage Range	V_{OUT}		2.6		3.8	V
Quiescent Current	I_Q	I_{OUT}=0, EN=1, ISET=250kΩ, FB=105%×V_{REF}		60	100	μA
Shutdown Current	I_{SHDN}	EN=0		0.1	1	μA
Feedback Reference Voltage	V_{REF}		0.591	0.6	0.609	V
NFET $R_{DS(ON)}$	$R_{DS(ON)1}$			50		mΩ
PFET $R_{DS(ON)}$	$R_{DS(ON)2}$			50		mΩ
Input Peak Current Limit	I_{LIM}		4.5	5		A
Output Negative Current Limit	I_{NEG}			-1		A
Soft-start Current	I_{SS}	Soft-start time: $t_{ss} = \frac{0.7V}{I_{ss}} \times C_{ss}$		5		μA
EN Rising Threshold	V_{ENH}		1.5			V
EN Falling Threshold	V_{ENL}				0.4	V
Input UVLO Rising Threshold	V_{UVLO}			2.45	2.55	V
UVLO Hysteresis	V_{HYS}			0.2		V
PG Rising Threshold	$V_{FB,HV}$			0.48		V
PG Under-voltage Threshold	$V_{FB,LV}$			0.48		V
PG Over Voltage Threshold	$V_{FB,OV}$			0.72		V
Output Current Sense	I_{SET}	I_{OUT}=1A		5		μA
Output Voltage Over Protection	V_{OVP}			125		%
OVP Protection Delay Time	t_{OVP_delay}			16		μs
ISET Pin Threshold for PFM Mode	V_{PFM}			0.2		V
Oscillator Frequency	f_{OSC}	I_{OUT}=1.0A	0.8	1.0	1.2	MHz
Min Duty Cycle		Boost & Buck		10		%
Max Duty Cycle		Boost & Buck		90		%
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			15		°C

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

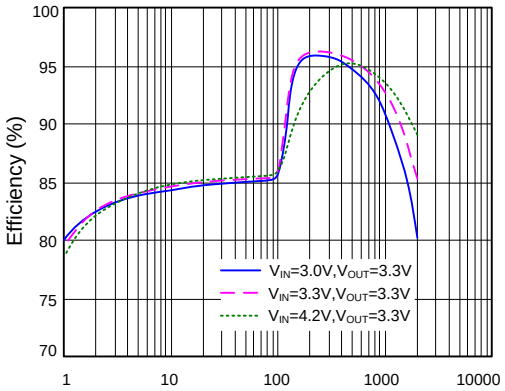
Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Paddle of QFN2×3-13 package is the case position for θ_{JC} measurement.

Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

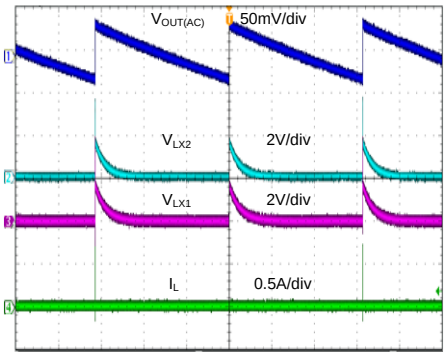
(T_A= 25℃, V_{OUT} = 3.3V, L = 1.0μH, C_{OUT}= 44μF, unless otherwise specified)

Efficiency vs. Load Current



Output Ripple

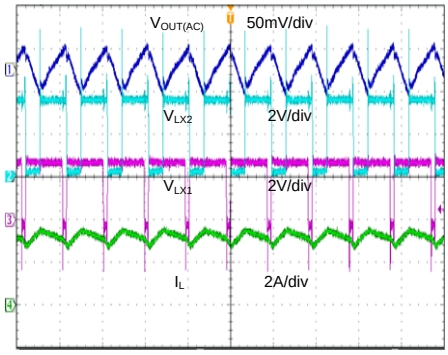
(V_{IN}=3.0V, V_{OUT}=3.3V, I_{OUT}=0A)



Time (10ms/div)

Output Ripple

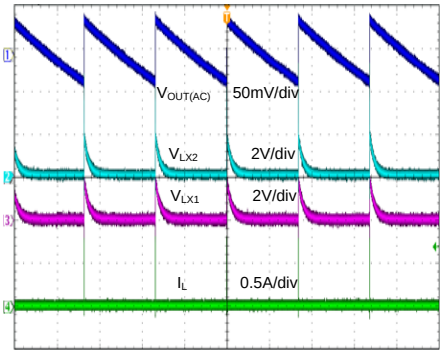
(V_{IN}=3.0V, V_{OUT}=3.3V, I_{OUT}=2A)



Time (1μs/div)

Output Ripple

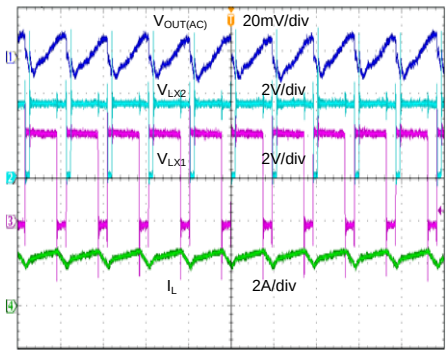
(V_{IN}=4.2V, V_{OUT}=3.3V, I_{OUT}=0A)



Time (20ms/div)

Output Ripple

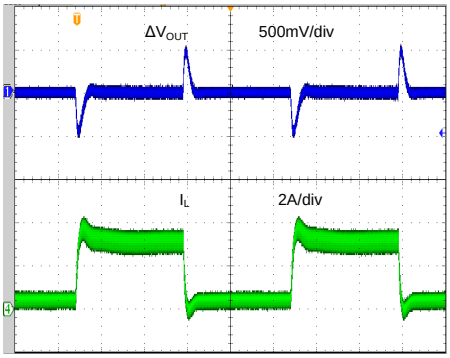
(V_{IN}=4.2V, V_{OUT}=3.3V, I_{OUT}=2A)



Time (1μs/div)

Load Transient

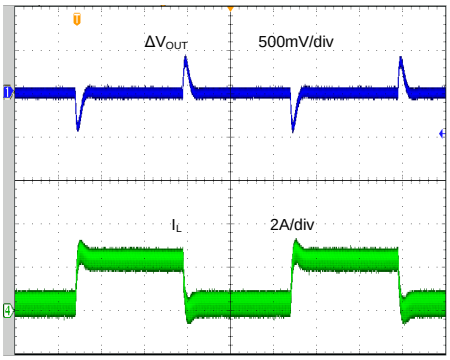
(V_{IN}=3.0V, V_{OUT}=3.3V, I_{OUT}=0.2~2A)



Time (200μs/div)

Load Transient

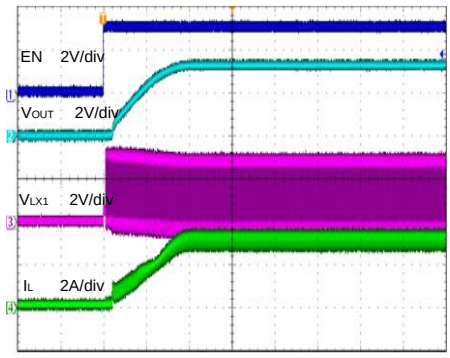
(V_{IN}=4.2V, V_{OUT}=3.3V, I_{OUT}=0.2~2A)



Time (200μs/div)

Startup From Enable

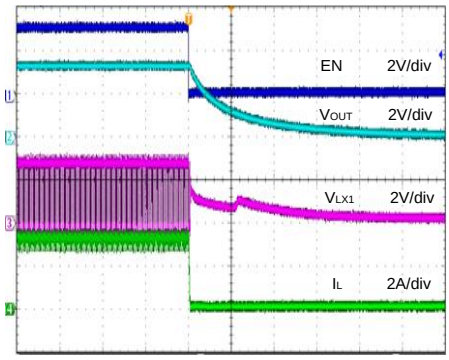
(V_{IN}=3.0V, V_{OUT}=3.3V, I_{OUT}=2A)



Time (800μs/div)

Shutdown From Enable

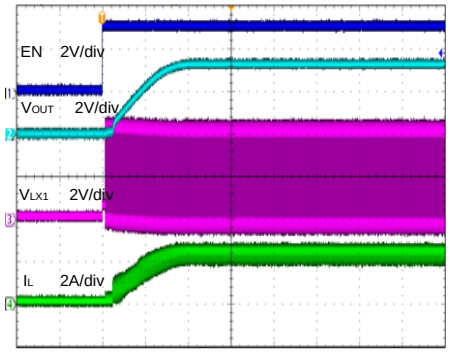
(V_{IN}=3.0V, V_{OUT}=3.3V, I_{OUT}=2A)



Time (40μs/div)

Startup From Enable

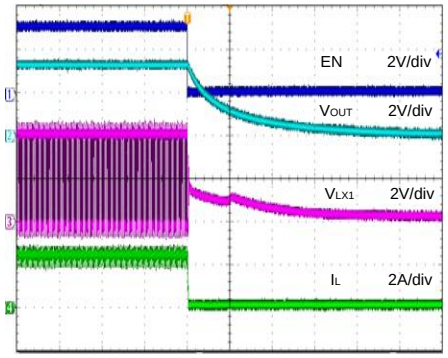
(V_{IN}=4.2V, V_{OUT}=3.3V, I_{OUT}=2A)



Time (800μs/div)

Shutdown From Enable

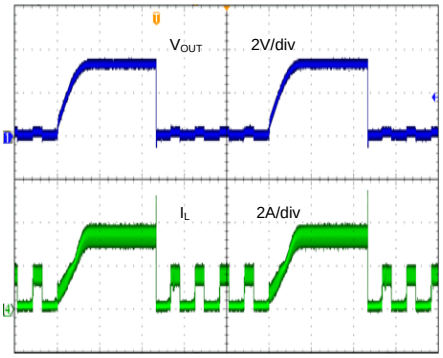
(V_{IN}=4.2V, V_{OUT}=3.3V, I_{OUT}=2A)



Time (40μs/div)

Short Circuit Protection

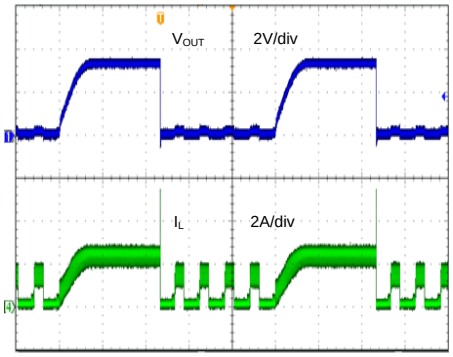
(V_{IN}=3.0V, V_{OUT}=3.3V, 2A to Short)



Time (2ms/div)

Short Circuit Protection

(V_{IN}=4.2V, V_{OUT}=3.3V, 2A to Short)



Time (2ms/div)

Operation

The SY20518 is a wide input voltage range, high efficiency, fixed frequency Buck-Boost converter that operates from input voltage above, below or equal to the output voltage. It provides a power supply for system powered by either a two-cell or three-cell alkaline, Ni-Cd or Ni-MH battery, or a one-cell Li-Ion or Li-polymer battery.

The SY20518 can support up to 2A of load current. It is based on a fixed frequency, pulse-width-modulation (PWM) controller using synchronous rectification to obtain maximum efficiency. The output voltage and compensation circuit can be programmed using an external RC.

Application Information

The following paragraphs provide the information needed for selecting the input capacitor C_{IN}, the output capacitor C_{OUT}, the inductor L and the feedback resistors (R_1 and R_2) need to meet the target specifications.

Input Under-voltage Lock-out

To prevent operation before all internal circuitry is ready and to ensure that the power and synchronous rectifier switches may be sufficiently enhanced, the device incorporates an input under-voltage lock-out (UVLO) protection. The device remains in a low current state and all switching is inhibited until V_{IN} exceeds V_{UVLO}, the input UVLO (rising) threshold. At that time, if EN is enabled, the device will start-up by initiating a soft-start ramp. If V_{IN} falls below V_{UVLO} less the UVLO hysteresis, switching will be suppressed again.

Enable Operation

Pulling the EN pin low (<0.4V) will shut down the device. During shutdown, the SY20516A shutdown current drops to lower than 0.1μA, Driving the EN pin high (>1.5V) will turn on the IC again.

SVIN

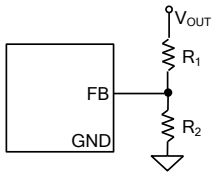
The SVIN is a signal power input pin which is used to supply power for the voltage reference. Decouple this pin to GND with at least a 1μF ceramic capacitor. Place this ceramic capacitor close to the SVIN and GND pins. Adding a 10Ω resistor in series between PVIN and SVIN is recommended.

Feedback Resistor Divider R1 and R2

Choose R_1 and R_2 to program the target output voltage. To minimize the power consumption under light load, it is desirable to choose large resistance values for both R_1 and R_2.

A value between 10k and 1M is recommended for both resistors. After selecting R1, R_2 can be calculated using the following formula:

$$R_2 = \frac{0.6R_1}{V_{OUT} - 0.6} (\Omega)$$



Input Capacitor C_{IN}

With the maximum load current at 2A, a typical X5R or better grade ceramic capacitor with 6.3V rating and greater than 22μF capacitors can handle this ripple current well. To minimize the switching noise, place this ceramic capacitor really close to the V_{IN} and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and the VIN/GND pins.

Output Capacitor C_{OUT}

Both steady state ripple and transient requirements must be considered when selecting this capacitor.

For the best performance, it is recommended to use two X5R or better grade ceramic capacitors, with 6.3V rating and more than 22μF capacitance.

The worst condition for the output voltage ripple is when the device operates in boost mode. The minimum capacitance required for a given output voltage ripple can be calculated using the formula:

$$C_{OUT} = I_{LOAD} \times \frac{D}{(\Delta V_{OUT} \times f_{SW})}$$

Where, D is the duty-cycle approximately equal to (V_{OUT}-V_{IN})/V_{OUT}, I_{LOAD} is the maximum load current and ΔV_{OUT} is the maximum acceptable voltage ripple. The output voltage ripple contribution from the output capacitor(s) ESR can be calculated as:

$$\Delta V_{ESR} = I_{LOAD} \times R_{ESR}$$

Where R_{ESR} represents the equivalent series resistance of the output capacitors.

The total output ripple is the sum of the ripple caused by the capacitance and the ripple caused by the ESR of the capacitor.

Output Inductor L:

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum average input current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN\_MAX})}{F_{SW} \times I_{OUT\_MAX} \times 40\%} (H)$$

where F_{SW} is the switching frequency and I_{OUT_MAX} is the maximum load current.

The SY20518 is less sensitive to the ripple current variations. Consequently, the final choice of inductance

can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of an inductor must be selected to guarantee an adequate margin to the peak inductor current under full load conditions.
The maximum peak current happens under minimum input voltage condition.

$$I_{SAT,MIN} > \left(\frac{V_{OUT}}{V_{IN\_MIN}}\right) \times I_{OUT,\,MAX} + \frac{V_{IN\_MIN}}{V_{OUT}} \frac{(V_{OUT} - V_{IN\_MIN})}{2 \times F_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<15mΩ to achieve a good overall efficiency.

Soft Start Programming

The SY20518 provides an external soft-start pin that gradually raises the output voltage. The soft-start time can be programmed by the external capacitor across SS pin and GND. The soft start time is calculated as:

$$t_{ss} = \frac{0.7}{I_{ss}} \times C_{ss}$$

If a 20nF capacitor is used, the typical soft-start time will be 2.8ms. Don't leave SS pin floating.

Light Load Mode

The device provides light load mode automatic switching between PFM and forced PWM operation. Choose the resistor between ISET pin and GND to program the hysteresis voltage which configures the mode transition point. The load current threshold when the SY20518 changes from PWM to PFM operation can be calculated as:

$$I_{PFM} = \frac{V_{REF\_PFM}}{R_Z \times 12.5 \times 10^{-6}}$$

Where V_{REF_PFM} is the reference for mode switching from PWM to PFM (0.2V typ.). The internal current sensing factor is about 12.5×10^{-6}.

The minimum load current for PWM operation is 130mA (typ.). Using a small resistor will reduce the hysteresis and may cause instability if the I_{PFM} is close to 130mA. If the resistor is too large it might force the device to always operate in forced PWM mode. A resistor with a value between 150kΩ and 250kΩ is recommended for most applications.

Loop Compensation

The SY20518 incorporates an average current control scheme. The inner current loop uses internal compensation. The outer voltage loop, is compensated using external components.

The device operates in buck mode or boost mode and in both cases loop compensation is required for stable operation.

Typically for a converter designed either work in buck mode or boost mode, the boost mode compensation design is more restrictive due to presence of a right half plan zero (RHPZ).

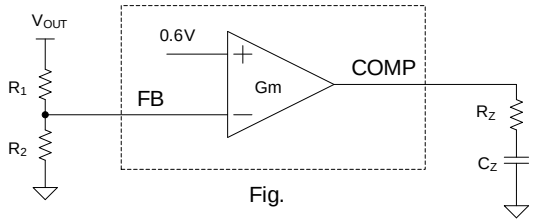


Fig.

To calculate the value of external components for the outer voltage loop, follow the following steps.

1. Select the crossover frequency fc of the closed loop. It is recommended that the crossover frequency is chosen 1/5 of the right half plane zero (f_{RHPZ}) and 1/10 of the switching frequency, in order to obtain a good tradeoff between stability and transient response of the system. The system has faster response at higher crossover frequency. For boost mode:

$$f_{RHPZ} = \frac{(1-D)^2 \times V_{OUT}}{2\pi \times L \times I_{OUT}}$$

2. Select the Rz value of the R-C series combination connected to the COMP pin.

$$R_Z = \frac{V_{OUT}}{G_m \times G_{fc} \times V_{REF}}$$

Where G_m is the error amplifier trans-conductance, which is typically 150uS; G_{fc} is gain of the power stage at the crossover frequency.

$$G_{fc} = \frac{(1-D)}{2\pi \times fc \times C_{OUT} \times R_S}$$

Where Rs is the current sense gain, which is typically 100mΩ.

3. Select the Cz value of the R-C series combination connected to the COMP pin. The compensation zero determines the phase margin at the crossover frequency. Place a compensation zero at or before the dominant pole of R_L and C_{OUT}.

$$C_Z = \frac{R_L \times C_{OUT}}{R_Z}$$

Where R_L is the load resistance.

Power Good Indicator

The PG pin is an open-drain output. The pin is actively driven low when the voltage measured at the FB pin is below 0.48V or above 0.72V. This translates to the output voltage being 20% below or above the target voltage set by the resistor divider.

The PG pin is also driven low during the start-up sequence, as soon as the voltage at the P_{VIN} pin reaches

the V_{UVLO} level, and until the output voltage raises to 80% of the configured value.

For proper operation, the pin requires a pull-up resistor to a voltage rail within the operating voltage range.

During normal operation, when the output is within +/-20% of the target, the output is Hi-Z and the pull-up resistor ensures a high level for interfacing to the rest of the system.

Thermal protection

The SY20518 includes over temperature protection circuitry to prevent overheating due to excessive power dissipation. This will shut down the device when the junction temperature exceeds 150°C. Once the junction temperature cools down by approximately 15°C, the device will resume normal operation after a complete soft-start cycle. For continuous operation, provide adequate cooling so that the junction temperature does not exceed the thermal protection threshold.

Short circuit protection

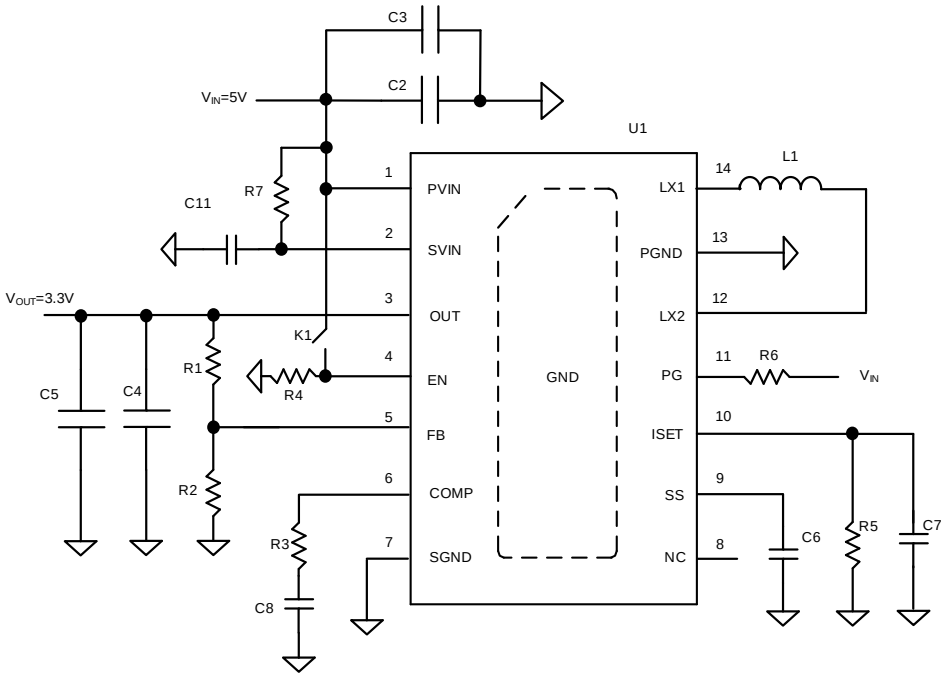
The SY20518 includes short circuit protection. If VOUT < ~50% of the target voltage and the device is in current limit, the short circuit protection mode will be initiated and the device will enter hic-cup protection mode. During hic-cup protection mode, the device will try to restart, and the cycle of hic-cup is approximately 4ms. If the output fault conditions are removed, the device will go back to normal operation on the nearest hic-cup on time with a complete soft start cycle.

Over Voltage Protection

The SY20518 includes output over voltage protection. If the feedback voltage rises above 125% of the feedback reference voltage the protection will be triggered after a 16µs delay. The device resumes operation once the overvoltage condition is removed.

Typical Design

Typical Schematic



Design Specifications

Input Voltage (V)	Output Voltage (V)	Maximum Output Current (A)
2.6~5.5	3.3	2

BOM List

Reference Designator	Description	Part Number	Manufacturer
L_1	1.0μH/14.1A inductor	SPM6530T-1R0M120	TDK
C_e	470μF/25V (Electrolytic Cap)		
C_1, C_2	22μF/6.3V, 0805, X5R	C2012X5R0J226M	TDK
C_4, C_5	22μF/6.3V, 0805, X5R	C2012X5R0J226M	TDK
C_3	1μF/25V, 0603		
C_7	10nF, 0603		
C_8	20nF, 0603		
C_9	1nF, 0603		
R_1	100kΩ, 1%, 0603		
R_2	22.1kΩ, 1%, 0603		
R_3	250kΩ, 0603		
R_4	10Ω, 0603		
R_5	100kΩ, 0603		
R_6	15kΩ, 0603		
R_7	1MΩ, 0603		

Layout Design suggestion

To achieve high efficiency and better noise immunity, following components should be placed close to the IC: C_{IN}, C_{OUT}, L, R_1 and R_2.

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and reduce the switching noise. Reasonable vias are suggested to be placed underneath the ground pad the thermal performance.

2) SVIN is the power supply pin for the internal control circuit. Don't connect SVIN pin to PVIN pin directly. A separate 1uF ceramic cap is strongly recommended to decouple SVIN pin to GND.

3) The decoupling capacitor of VIN must be placed close enough to the VIN pin and GND pins. The loop area formed by the input capacitors, VIN pin and GND pins must be minimized.

4) The PCB copper area associated with LX pin must be minimized to reduce switching noise and EMI.

5) The components R_1, R_2 and the trace connecting to the FB/OUT pin must NOT be adjacent to the LX node on the PCB layout to minimize the noise coupling to FB/OUT pin.

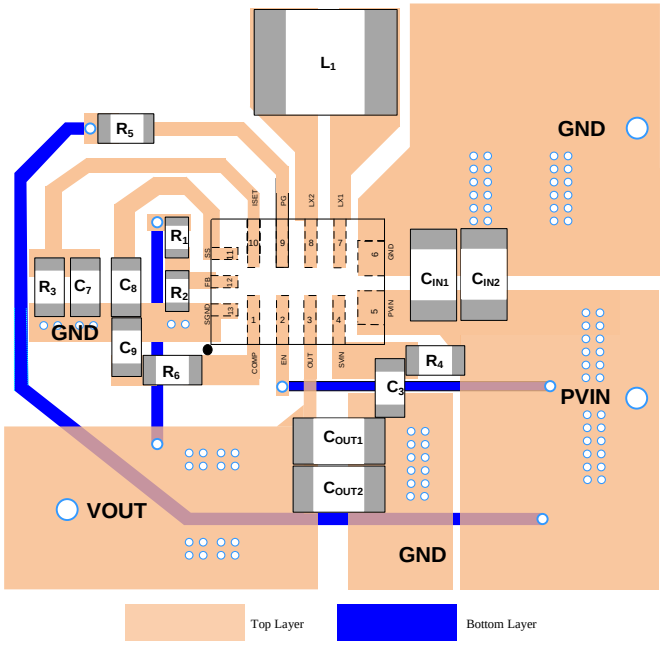
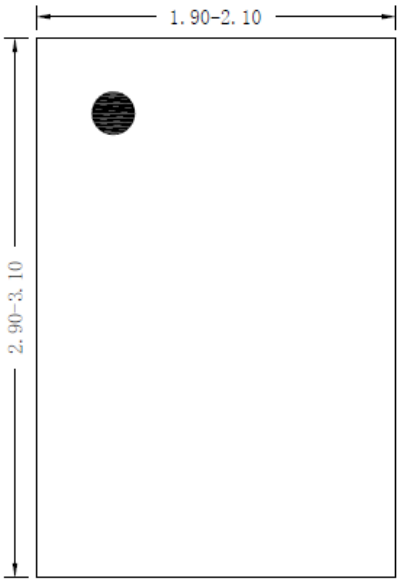
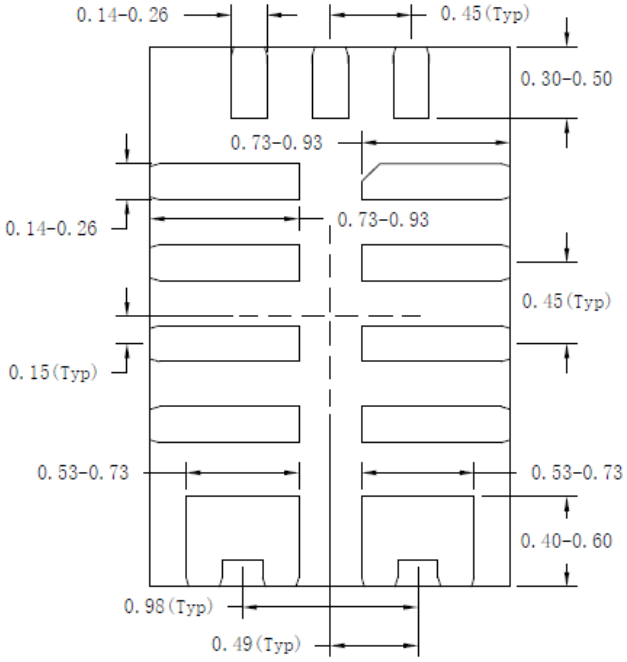


Figure3. PCB Layout Suggestion

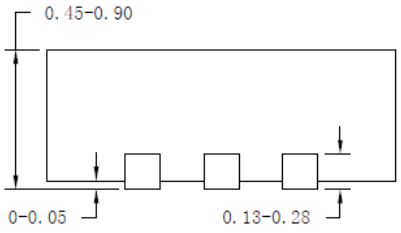
QFN2×3-13 Package Outline Drawing



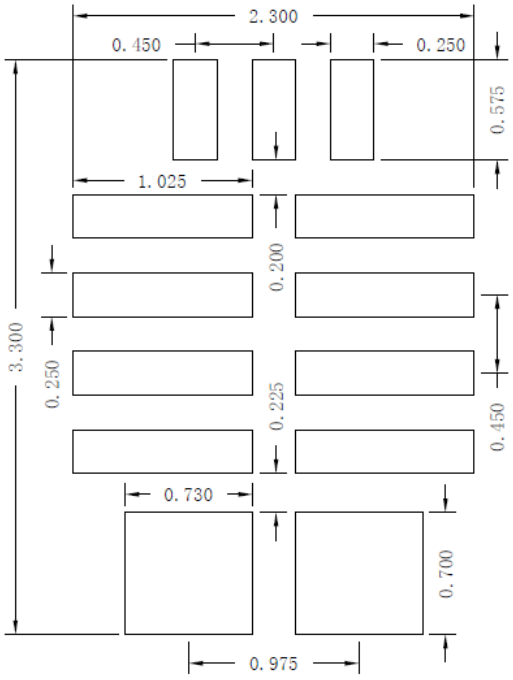
Top View



Bottom View



Side View

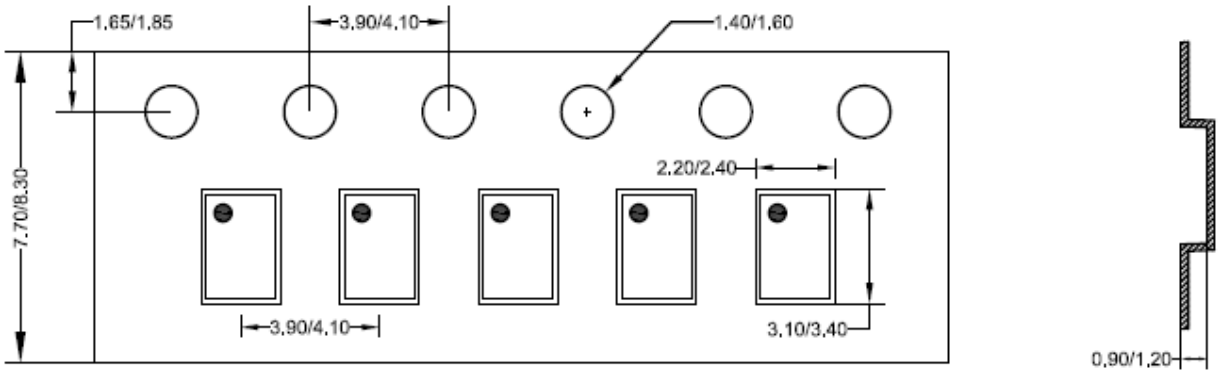


Recommended PCB layout
(Reference Only)

Notes: All dimension in millimeter and exclude mold flash & metal burr.

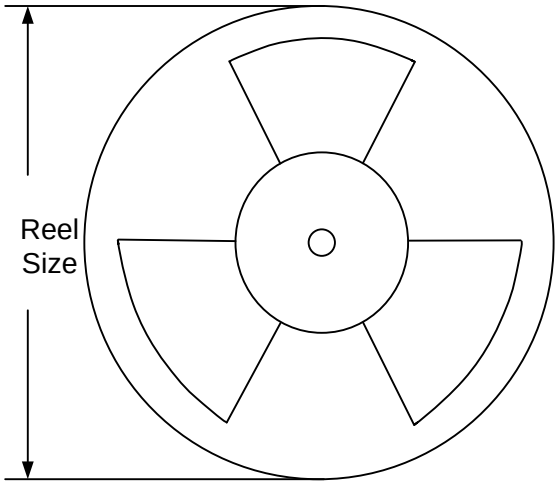
Taping & Reel Specification

1. QFN2×3-13 taping orientation



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN2x3	8	4	7"	400	160	3000

3. Others: NA

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