SY20725

40V, 300mA LDO Regulator

General Description

The SY20725 is an efficient, precise low-dropout (LDO) regulator designed for high input voltage and ultra-low quiescent current applications.

The SY20725 provides adjustable output voltage with ±2% accuracy and very low dropout (300mV at 300mA). It also features optimized internal compensation, overcurrent protection, and thermal shutdown for stable operation when using low-ESR ceramic or tantalum capacitors.

The device can be enabled by driving the EN pin above the V_{EN_H} threshold (1.5V) and disabled by driving EN below V_{EN_L} (0.4V).

Only the divider resistors, input capacitor, and output capacitor need to be selected for the targeted application.

SY20725 is available in a compact SOT23-5 package.

Features

- Wide Input Voltage Range: 4V to 40V
- Low Dropout Voltage (300mV at 300mA)
- Low Quiescent Current (10μA max)
- Very Low Shutdown Current (1.25μA max)
- Stable with Tantalum or Ceramic Capacitors
- Excellent Load and Line Regulation
- ±2% 0.6V Reference Accuracy
- 300mA Maximum Load Current
- Enable Control Input
- Overcurrent Protection
- Thermal Shutdown
- Compact SOT23-5 Package

Applications

- Battery-Powered Applications
- Automotive Applications
- Gateway Applications
- Remote Keyless Entry Systems
- SMPS Post-Regulator/ DC-DC Modules

Typical Application

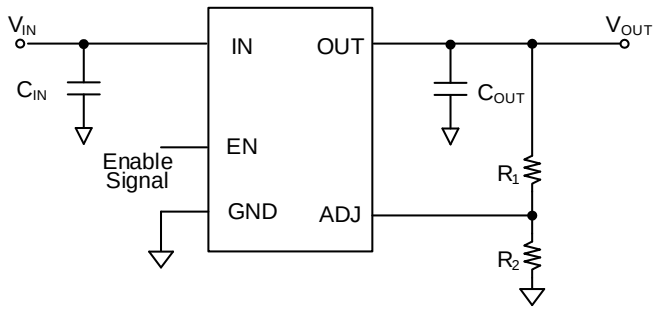


Figure 1. Schematic diagram

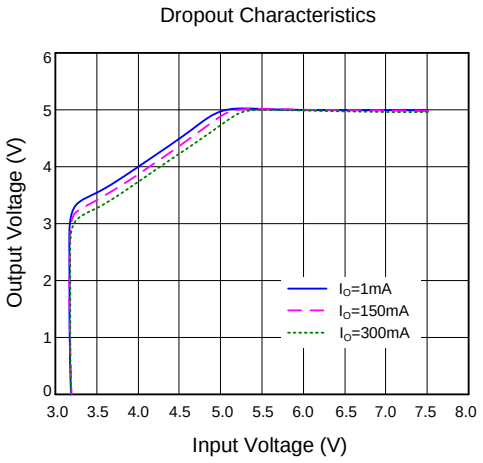


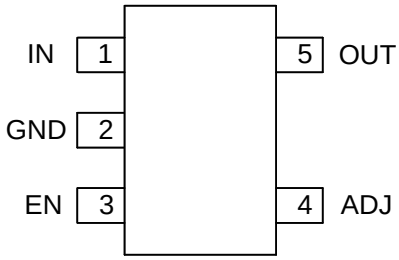
Figure 2. Dropout characteristics

Ordering Information

Ordering Part Number	Package Type	Details
SY20725AAC	SOT23-5 RoHS-Compliant and Halogen-Free	**YS*xyz***

x = year code, y = week code, z = lot number code

Pinout (top view)



Pin Description

Pin No.	Pin Name	Pin Description
1	IN	IC power supply input. Bypass this pin to the Ground pin with a capacitor.
2	GND	Ground pin
3	EN	Enable pin. Pull low to shut down or pull high to enable; do not leave floating.
4	ADJ	Output voltage adjust pin. Feed the output voltage back through the resistor voltage divider network. V_{OUT} = 0.6 × (1 + R1 / R2)
5	OUT	Output pin. Bypass this pin to the Ground pin with a low-ESR ceramic capacitor.

Block Diagram

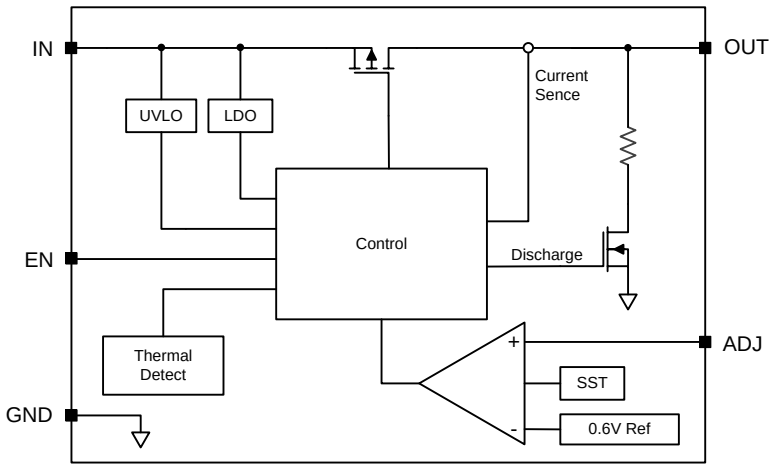


Figure 3. Block diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
IN to GND	-0.3	40	V
OUT, EN, ADJ to GND	-0.3	0.3+V_{IN}	
Lead Temperature (Soldering, 10 sec.)		260	°C
Junction Temperature, Operating	-40	150	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	45	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	22.5	

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
IN	0	72	V
Output Voltage	0	72	
Output Current	0	18	
Junction Temperature	-40	125	°C

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Note 2: I_{RTN} = 0 for V_{RTN} > 80V.
Note 3: Do not apply voltage to this pin.
Note 4: JESD 51-2，-5，-7，-8，-14 standard.

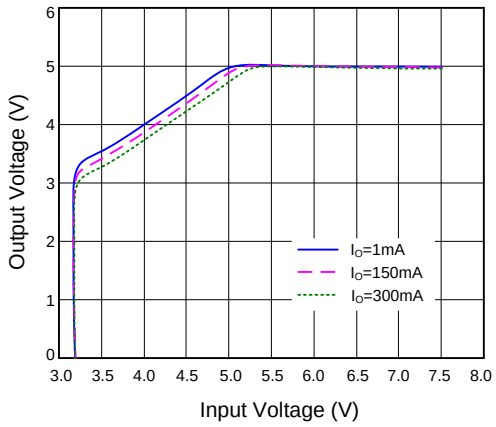
Electrical Characteristics

(V_{IN} = 12V, V_{EN} = V_{IN}, T_A = 25°C unless otherwise specified)

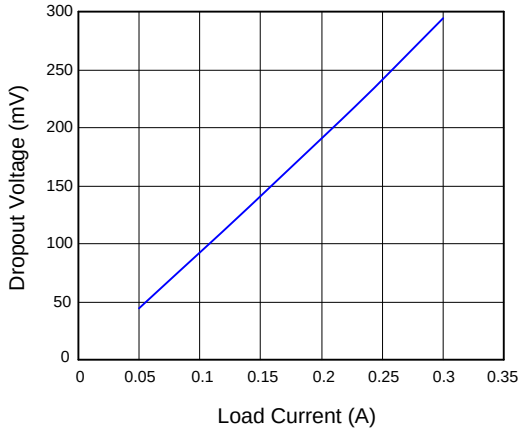
Parameter	Symbol	Test Conditions	Min	Typical	Max	Unit
Input Voltage	V_{IN}	I_{OUT} = 10mA	4		40	V
Reference Voltage	V_{REF}	V_{IN} = 12V, Io = 10mA	588	600	612	mV
Line Regulation	ΔV_{LNR}	V_{IN} = (V_{OUT} + 0.3V) to 40V, I_O = 10mA		1		mV/V
Load Regulation	ΔV_{LDR}	I_O = 10mA to 300mA		0.25	1	%
Dropout Voltage	V_{IN}-V_{OUT}	I_O = 10mA		10		mV
		I_O = 150mA		150		mV
		I_O = 300mA		300		mV
Quiescent Current	I_Q	No Load		7	10	μA
Shutdown Current	I_{SHDN}	V_{EN} = 0V, V_{IN} = 24V			1.25	μA
Output Current	I_O	V_{IN} = V_{OUT}+0.6V	0		300	mA
Output Current limit	I_{LIM}	V_{IN} = 6V, V_{OUT} = 0.9 x V_{OUT} (normal)	350		750	mA
Power-Supply Rejection Ratio	PSRR	f = 1kHz, C_{OUT} = 10uF		60		dB
		f = 150kHz, C_{OUT} = 10uF		30		dB
Input UVLO Threshold	V_{UVLO}	V_{IN} rising			3.8	V
UVLO Hysteresis	V_{UVLO_th}			0.2		V
Shutdown Discharge Resistance	R_{DIS}			600		Ω
Enable Input Logic-High Voltage	V_{EN_H}	V_{IN} = 5V to 40V	1.5			V
Enable Input Logic-Low Voltage	V_{EN_L}	V_{IN} = 5V to 40V			0.4	V
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown hysteresis	T_{HYS}			20		°C

Typical Performance Characteristics

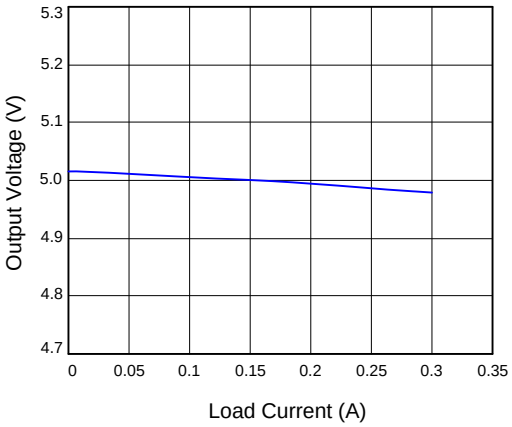
Dropout Characteristics



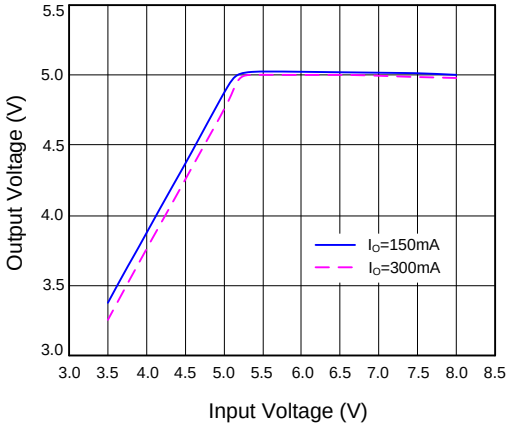
Dropout Voltage vs. Load Current



Load Regulation

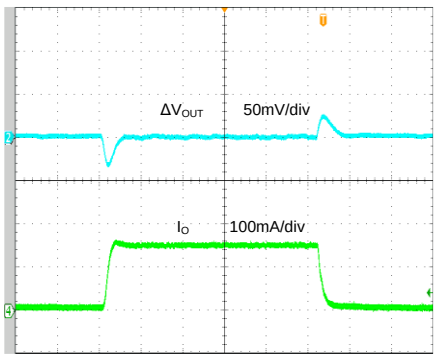


Line Regulation



Load Transient

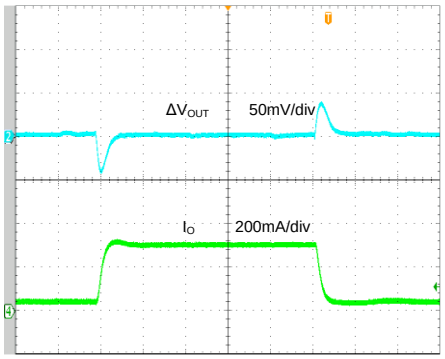
(V_{IN}=7.4V, V_{OUT}=5V, I_{OUT}=0~150mA)



Time (100μs/div)

Load Transient

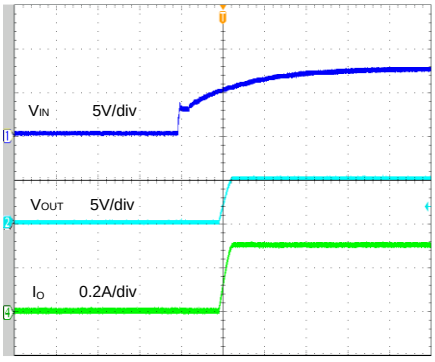
(V_{IN}=7.4V, V_{OUT}=5V, I_{OUT}=30~300mA)



Time (100μs/div)

Startup from V_{IN}

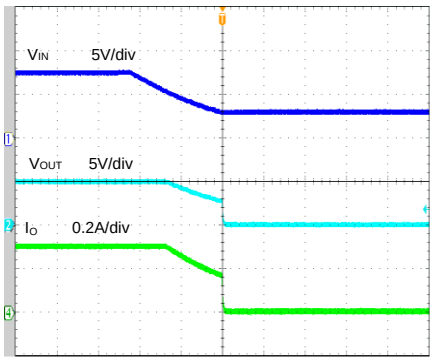
(V_{IN}=7.4V, V_{OUT}=5V, I_{OUT}=300mA)



Time (2ms/div)

Shutdown from V_{IN}

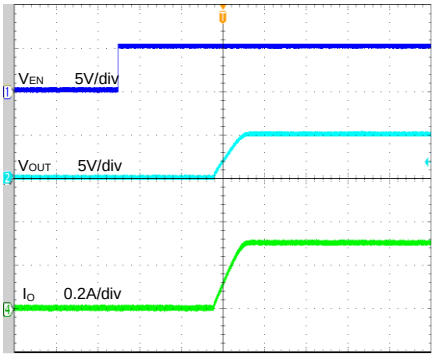
(V_{IN}=7.4V, V_{OUT}=5V, I_{OUT}=300mA)



Time (2ms/div)

Startup from Enable

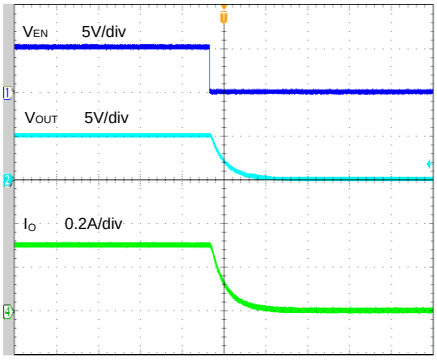
(V_{IN}=7.4V, V_{OUT}=5V, I_{OUT}=300mA)



Time (800μs/div)

Shutdown from Enable

(V_{IN}=7.4V, V_{OUT}=5V, I_{OUT}=300mA)



Time (100μs/div)

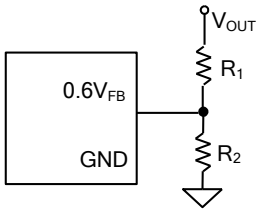
Application Information

The SY20725 is a 300mA linear regulator with a low dropout voltage. The SY20275 is highly integrated, so only the divider resistors, input capacitor, and output capacitor need to be selected for the targeted application specifications.

Feedback Resistor-Divider R1 and R2

Select R1 and R2 to program the proper output voltage. To minimize power consumption under light loads, select large resistance values (between 10kΩ and 1MΩ) for both R1 and R2. Given V_{OUT} = 3.3V and R1 = 100kΩ, then R2 can be calculated as 22.2kΩ using the following equation:

$$R2 = \frac{0.6V}{V_{OUT} - 0.6V} \times R1$$



With a calculated value of 22.2kΩ for R2, a standard 1% 22.1kΩ resistor is selected.

Input Capacitor C_{IN}

For the best performance, select a typical X5R or better grade ceramic capacitor with a 10V rating, and greater than 2.2μF capacitance. The capacitor should be placed as close as possible to the device, while also minimizing the loop area formed by C_{IN} and the IN/GND pins. When selecting an input capacitor, ensure that its voltage rating is at least 20% greater than the maximum voltage of the input supply. X5R or X7R dielectric types are the most often selected due to their small size, low cost, surge current capability, and high RMS current rating over a wide temperature and voltage range.

In situations where the input rail is supplied through long wires, it is recommended to add some bulk capacitance like electrolytic, tantalum or polymer type capacitors to reduce the overshoot and ringing caused by the added parasitic inductance.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

Output Capacitor C_{OUT}

For transient stability, the SY20725 is designed specifically to work with small ceramic capacitors. A 2.2μF output capacitor can be used in this application, but higher capacitance values help to improve transient stability. Using a low ESR capacitor is important because it forms a zero to provide phase lead, which is required for loop stability.

Dropout Voltage

The SY20725 has a very low dropout voltage due to the low $R_{DS(ON)}$ of the main PMOS, which determines the lowest usable supply.

$$V_{DROPOUT} = V_{IN} - V_{OUT} = R_{DS(ON)} \times I_{OUT}$$

Overcurrent and Short-Circuit Protection

The SY20725 includes overcurrent and short-circuit protection. The current limitation circuit regulates the output current to its limit threshold to protect the IC from damage. Under an overcurrent or short-circuit condition, the power loss of the IC is relatively high, which may also trigger thermal protection.

Thermal Considerations

The SY20725 can deliver a current of up to 300mA over the full operating junction temperature range. However, the maximum output current must be derated at higher ambient temperatures to ensure the junction temperature does not exceed 125℃. For all possible conditions, the junction temperature must be within the range specified under operating conditions. Power dissipation can be calculated based on the output current and the voltage drop across the regulator, as follows:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND}$$

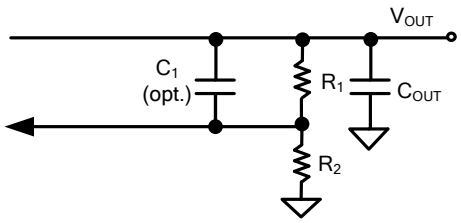
The final operating junction temperature for any set of conditions can be estimated by the following thermal equation:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA}$$

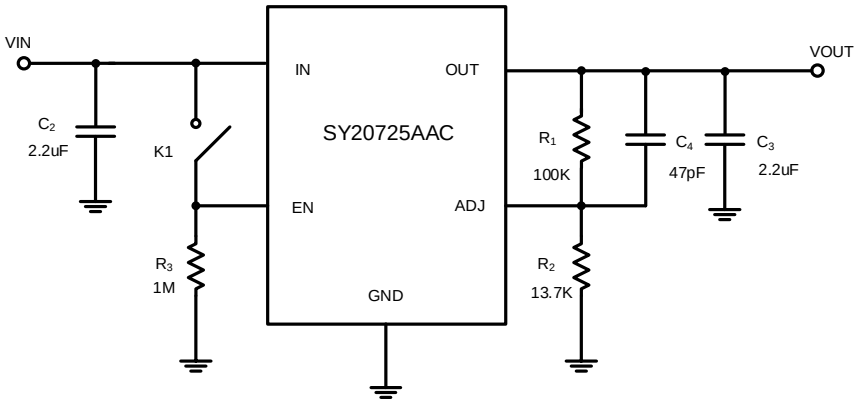
Where $T_{J(MAX)}$ is the maximum junction temperature of the die (125℃), and T_A is the maximum ambient temperature. The junction-to-ambient thermal resistance (θ_{JA}) footprint is 170℃/W for the SOT23-5 package.

Load-Transient Considerations

The SY20725 integrates the compensation components to achieve good stability and fast transient responses. In some applications, adding a small ceramic capacitor in parallel with R1 may further speed up the load-transient responses, and is thus recommended for applications with large load-transient step requirements.



Application Schematic (V_{OUT} = 5V)



BOM List

Reference Designator	Description	Part Number	Manufacturer
C2, C3	CHIP CAP X7R 2.2µF ±10% 50V 1206	C3216X7R1H225K	TDK
C4	CHIP CAP C0G 47pF ±5% 50V 0603	C1608C0G1H680J	TDK
R1	100kΩ ±1% 0.1W 0603	RC0603FR-07100KL	YAGEO
R2	13.7kΩ ±1% 0.1W 0603	RC0603FR-0713K7L	YAGEO
R3	1MΩ ±1% 0.1W 0603	RC0603FR-071ML	YAGEO

Layout Design

Good PCB layout practices must be followed to prevent ground loops and voltage drops from inducing instability. Additionally, increased PCB copper area can improve thermal performance.

The input and output capacitors MUST be directly connected to the input, output, and ground pins of the device using traces that have no other currents flowing through them. The best way to do this is to place C_{IN} and C_{OUT} near the device with short traces to the V_{IN}, V_{OUT}, and ground pins. The regulator ground pin should be connected to the external circuit ground so that the regulator and its capacitors have a single-point ground.

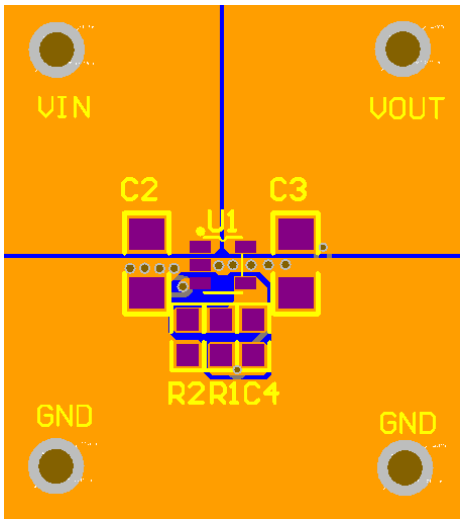
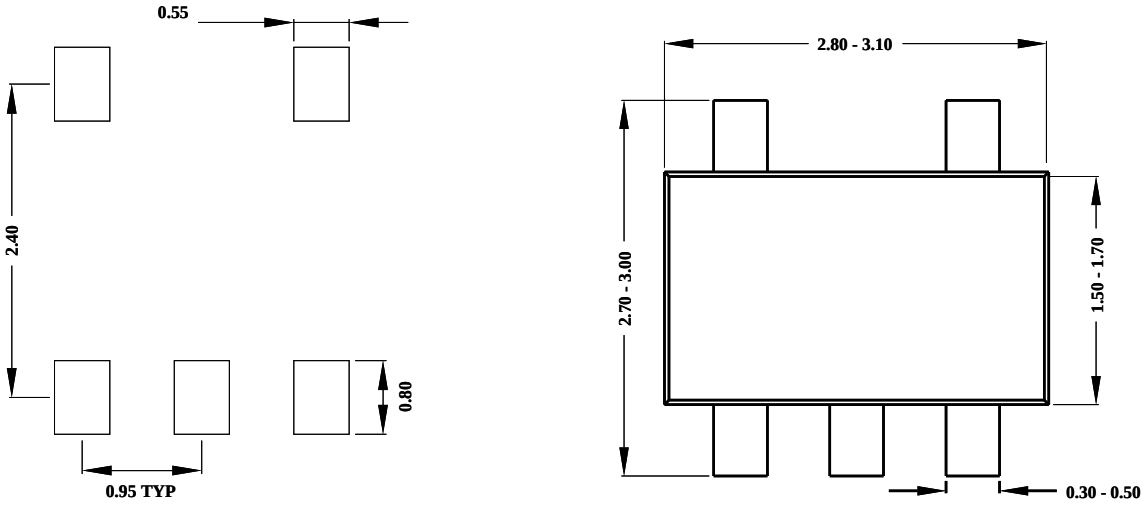
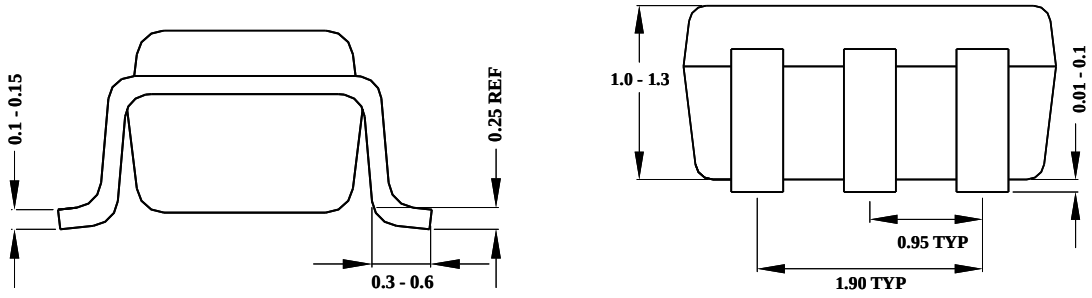


Figure 4. Recommended PCB layout

SOT23-5 package outline



Recommended Pad Layout

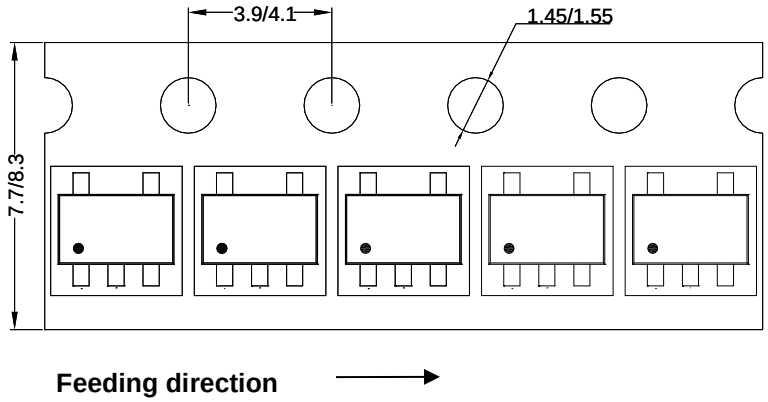


Note: *All dimensions are in millimeters and exclude mold flash and metal burr.*

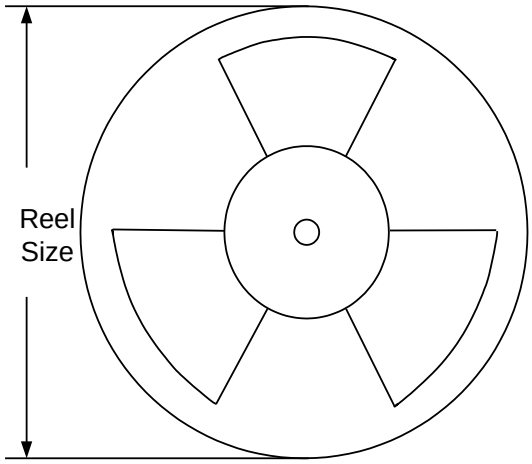
Taping and Reel Specification

Taping orientation

SOT23-5



Carrier tape and reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SOT23-5	8	4	7"	280	160	3000

Others: NA

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change
Apr .22, 2023	Revision 1.0	Upgrade the version code to Rev1.0 for Production Release. (No change in Specification.)
Mar.21, 2016	Revision 0.9	Initial Release

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