SY21113I

High-Efficiency, 3A, 18V Input Synchronous Step-Down Regulator

General Description

The SY21113I high-efficiency 500kHz synchronous step-down DC/DC regulator operates over a wide input voltage range of 4.2V to 18V, and can deliver an output current up to 3A. It integrates a main switch and a synchronous switch with very low $R_{DS(ON)}$ to minimize conduction loss. The 500kHz pseudoconstant switching frequency enables using small external inductor and capacitor values.

The SY21113I uses constant-on-time and ripple-based control to provide high efficiency at light loads, and to achieve fast transient responses for applications with high step-down ratios. It also provides cycle-by-cycle current limiting and overtemperature protection.

The SY21113I is available in a compact TSOT23-6 package.

Features

- 4.2V to 18V Input Voltage Range
- Up to 3A Output Current
- Low $R_{DS(ON)}$ for Internal Switches: 80mΩ Top, 40mΩ Bottom
- 500kHz Switching Frequency Minimizes External Components
- Constant-On-Time and Ripple-Based Control to Achieve Fast Transient Responses
- Stable with 10µF C_{OUT} and 2.2µH Inductor
- Cycle-by-Cycle Top/Bottom Current Limits
- Internal Soft-Start Limits Inrush Current
- Hiccup Mode Output Short-Circuit Protection
- Overtemperature Protection with Auto-Recovery
- Output Auto-Discharge Function
- RoHS-Compliant and Halogen-Free
- Compact Package: TSOT23-6

Applications

- Set-Top Box
- Portable TV
- DSL Modem
- LCD TV
- IP Camera
- Networking

Typical Application

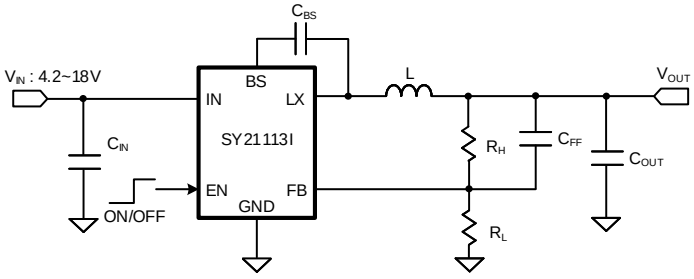


Figure 1. Schematic Diagram

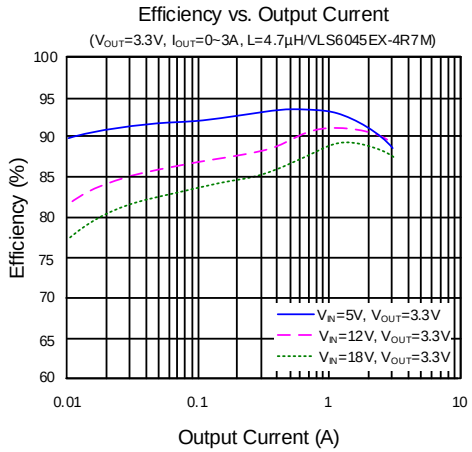


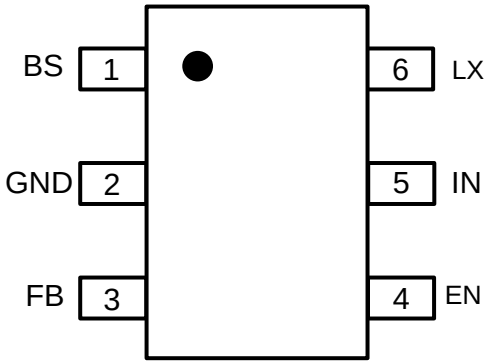
Figure 2. Efficiency vs. Output Current

Ordering Information

Ordering Part Number	Package type	Top Mark
SY21113IADC	TSOT23-6 RoHS-Compliant and Halogen-Free	dK*xyz*

x = year code, y = week code, z = lot number code

Pinout (top view)



Pin Description

Pin No	Pin Name	Pin Description
1	BS	Bootstrap pin. Supply for the high-side gate driver. Connect a 0.1μF ceramic capacitor between the BS and LX pins.
2	GND	Ground pin.
3	FB	Output feedback pin. Connect this pin to the center point of the output resistor-divider as shown in Figure 1. $V_{OUT} = 0.6 \times (1 + R_H/R_L)$.
4	EN	Enable pin. Pull low to disable the device, pull high to enable. Do not leave this pin floating.
5	IN	Power input. Decouple this pin from the GND pin with at least a 10μF ceramic capacitor.
6	LX	Inductor pin. Connect this pin to the switching node of inductor.

Block Diagram

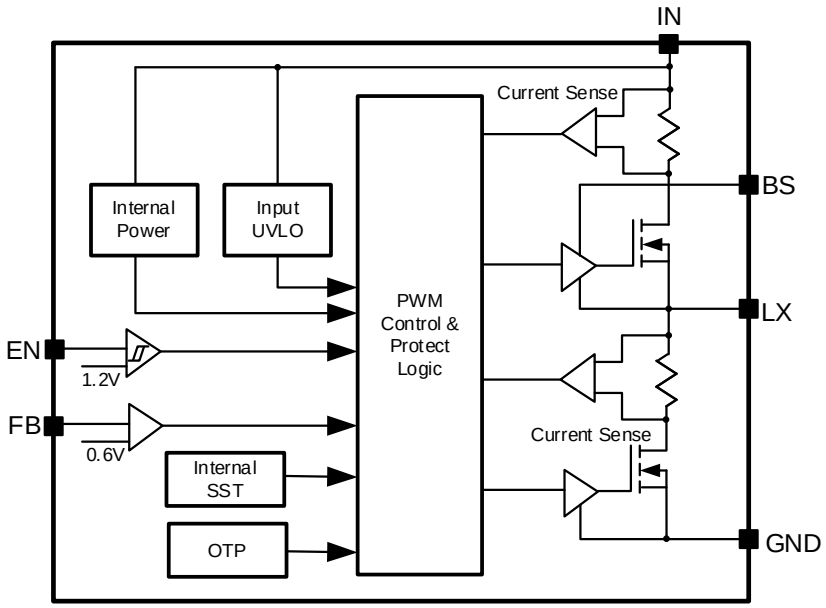


Figure 3. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
IN	-0.3	19	V
EN, LX	-0.3	IN + 0.3	
LX, 10ns duration	-5	IN + 3	
BS	LX - 0.3	LX + 4	
FB	-0.3	4	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering,10s)		260	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	66	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	15	
P_D Power Dissipation T_A = 25°C	1.5	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
IN	4.2	18	V
Output Current		3	A
Ambient Temperature	-40	85	°C
Junction Temperature	-40	125	

Electrical Characteristics

(V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7μH, C_{OUT} = 10μF, T_A = 25°C, I_{OUT} = 1A unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input	Voltage Range	V_{IN}		4.2		18	V
	UVLO Rising Threshold	V_{UVLO}				4.15	V
	UVLO Hysteresis	V_{HYS}			0.3		V
	Quiescent Current	I_Q	I_{OUT} = 0A, V_{FB} = V_{REF} × 105%		200	280	μA
	Shutdown Current	I_{SHDN}	V_{EN} = 0V		5	10	μA
Output	FB Reference Voltage	V_{REF}		591	600	609	mV
	FB Input Current	I_{FB}	V_{FB} = 3.3V	-50		50	nA
	Turn-On Delay	$t_{ON,DLY}$	from EN high to LX start switching		300		μs
	Soft-Start Time	t_{SS}	V_{OUT} from 0 to 100%	0.5	1	1.5	ms
	Discharge FET Resistance	R_{DIS}			40		Ω
	UVP Threshold	V_{UVP}			33		%V_{REF}
	UVP Delay	$t_{UVP,DLY}$			100		μs
	UVP Hiccup On-Time	$t_{HICCUP,ON}$			2		ms
	UVP Hiccup Off-Time	$t_{HICCUP,OFF}$			6		ms
Enable (EN)	Rising Threshold	$V_{EN,R}$		1.08	1.2	1.32	V
	Falling Threshold	$V_{EN,F}$		0.9	1.0	1.1	V
MOSFET	Top FET On-Resistance	$R_{DS(ON),TOP}$			80	120	mΩ
	Bottom FET On-Resistance	$R_{DS(ON),BOT}$			40	60	mΩ
	Top FET Current Limit	$I_{LMT,TOP}$		4.5			A
	Bottom FET Current Limit	$I_{LMT,BOT}$		3			A
Frequency	Switching Frequency	f_{SW}	V_{OUT} = 3.3V, CCM		500		kHz
	Min On-Time	$t_{ON,MIN}$			50		ns
	Min Off-Time	$t_{OFF,MIN}$			200		ns
OTP	Temperature	T_{OTP}	(Note 4)		150		℃
	Temperature Hysteresis	T_{HYS}	(Note 4)		15		℃

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} of SY21113I is measured in the natural convection at T_A = 25℃ on a 2oz two-layer Silergy evaluation board. Paddle of TSOT23-6 package is the case position for SY21113I θ_{JC} measurement.

Note 3: The device is not guaranteed to function outside its operating conditions.

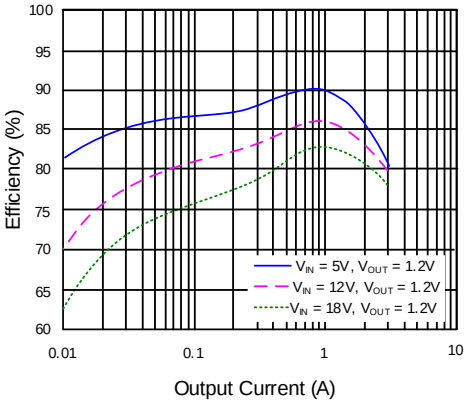
Note 4: Guaranteed by design.

Typical Performance Characteristics

(SY21113I, T_A = 25°C, V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, C_{OUT} = 10µF, unless otherwise noted)

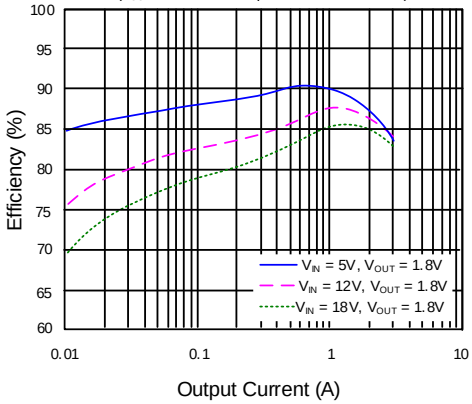
Efficiency vs. Output Current

(I_{OUT} = 0~3A, L = 2.2µH/VLS6045EX-2R2N)



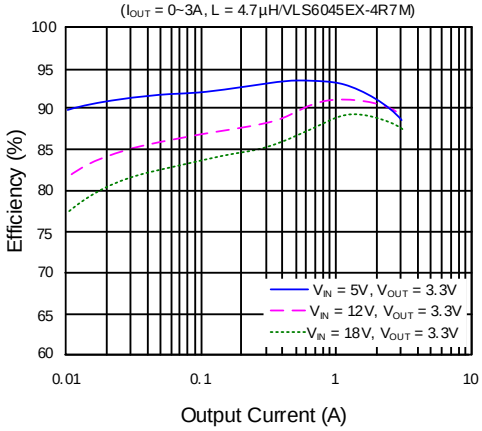
Efficiency vs. Output Current

(I_{OUT} = 0~3A, L = 3.3µH/VLS6045EX-3R3N)



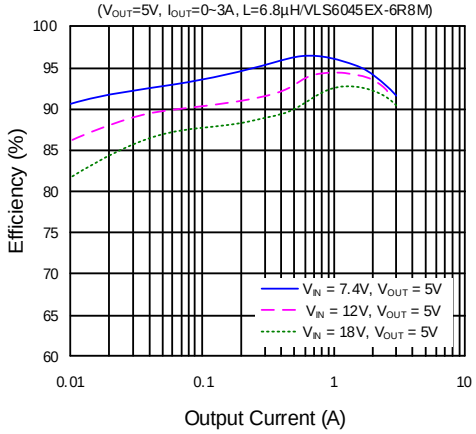
Efficiency vs. Output Current

(I_{OUT} = 0~3A, L = 4.7µH/VLS6045EX-4R7M)



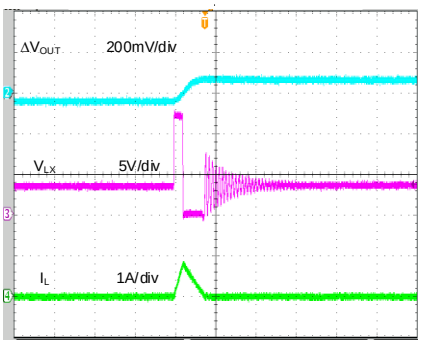
Efficiency vs. Output Current

(V_{OUT}=5V, I_{OUT}=0~3A, L=6.8µH/VLS6045EX-6R8M)



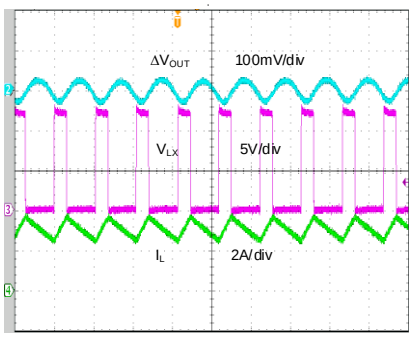
Output Ripple

(V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A)



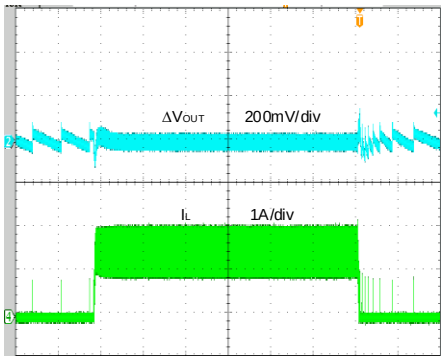
Output Ripple

(V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 3A)



Load Transient

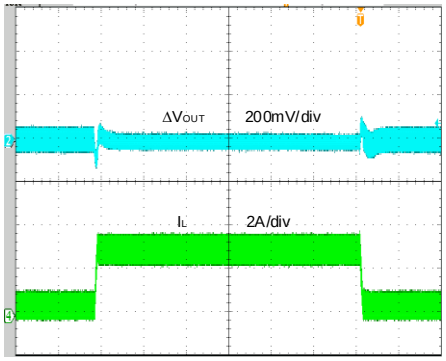
(V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A ~ 1.5A)



Time (400μs/div)

Load Transient

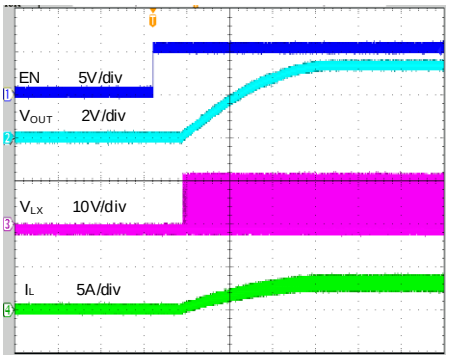
(V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0.3A ~ 3A)



Time (400μs/div)

Startup from Enable

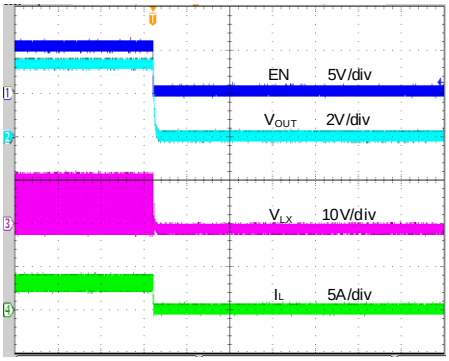
(V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 3A)



Time (400μs/div)

Shutdown from Enable

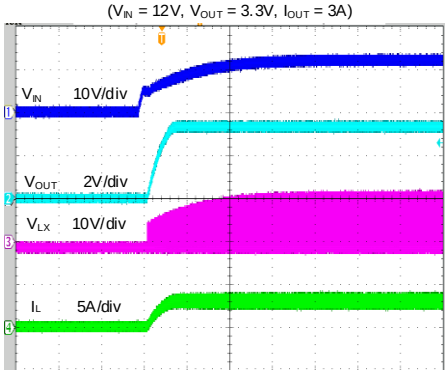
(V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 3A)



Time (400μs/div)

Startup from V_{IN}

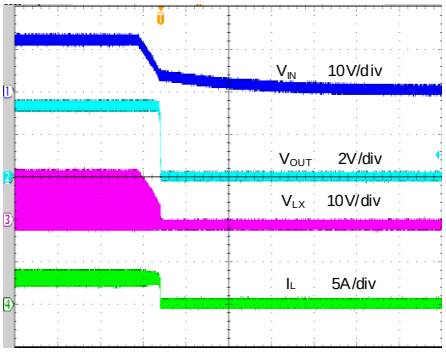
(V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 3A)



Time (2ms/div)

Shutdown from V_{IN}

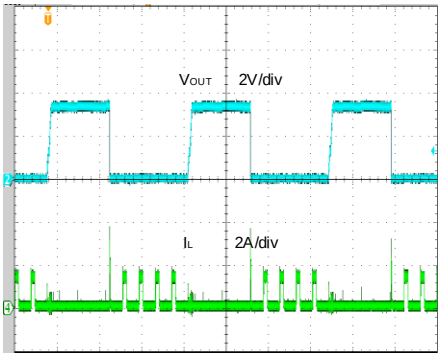
(V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 3A)



Time (2ms/div)

Short Circuit Protection

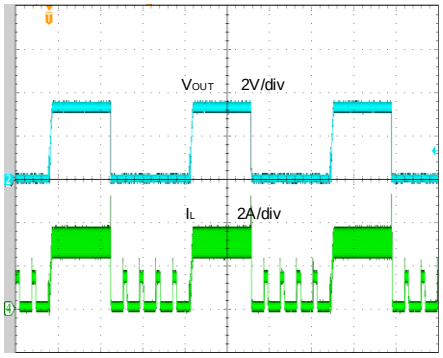
(V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A ~ short)



Time (20ms/div)

Short Circuit Protection

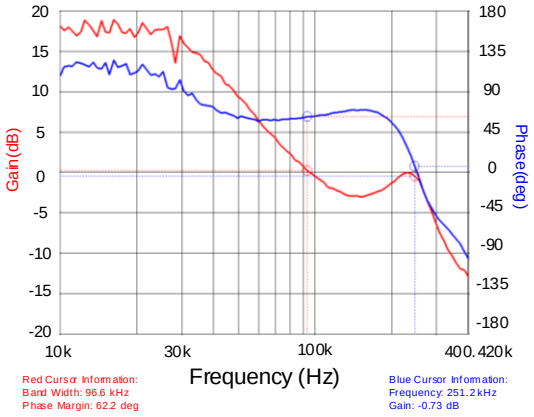
(V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 3A ~ short)



Time (20ms/div)

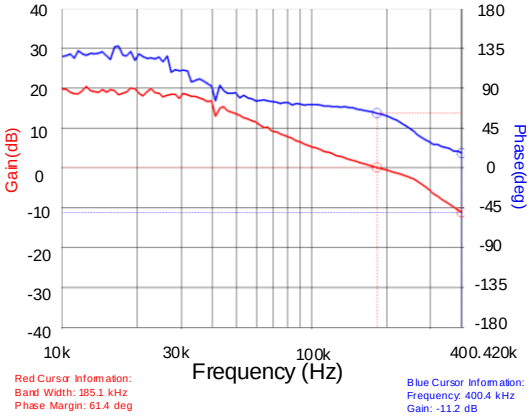
Bode Plot

(V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 3A)



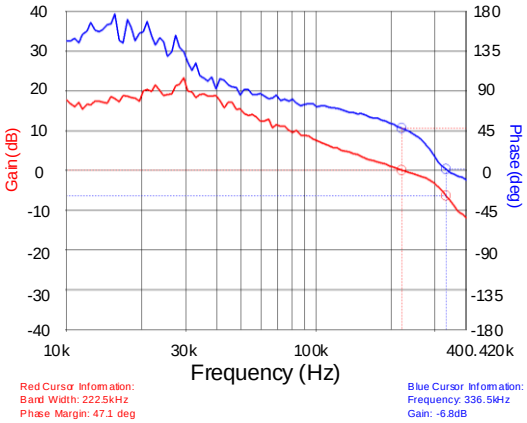
Bode Plot

(V_{IN} = 12V, V_{OUT} = 1.8V, I_{OUT} = 3A)



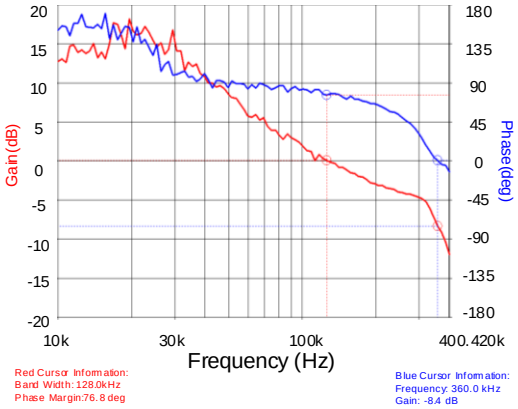
Bode Plot

(V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 3A)



Bode Plot

(V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 3A)



Operation

The SY21113I high-efficiency 500kHz synchronous step-down DC/DC regulator operates over a wide input voltage range of 4.2V to 18V, and can deliver an output current up to 3A. It integrates a top FET and a bottom FET with very low $R_{DS(ON)}$ to minimize conduction loss. The 500kHz pseudo-constant switching frequency allows small external inductor and capacitor values.

The SY21113I also provides cycle-by-cycle current limiting and thermal shutdown protection.

Constant-On-Time and Ripple-Based Control

The SY21113I uses Instant-PWM™ architecture to achieve high efficiency at light loads and fast transient response for applications with high step-down ratios. It uses a constant-on-time and ripple-based control strategy in which a virtual replica of the inductor current signal is synthesized internally and combined with the feedback voltage. When the sum of the above voltages is lower than the reference voltage, the bottom FET turns off and the top FET turns on for a fixed period of time (constant t_{ON}). t_{ON} is internally calculated according to the input voltage, output voltage, and desired switching frequency (f_{SW}):

$$t_{ON} = \frac{V_{OUT}/V_{IN}}{f_{SW}}$$

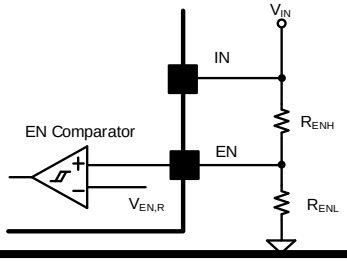
The top FET turns off after a period of t_{ON}.

Input Undervoltage Lockout (UVLO)

The SY21113I incorporates input undervoltage lockout (UVLO) protection to prevent operation before all internal circuitry is ready, and to ensure that the top FET and bottom FET are properly biased. The SY21113I remains in a low-current state and all switching actions are inhibited until V_{IN} exceeds its rising threshold. At that time, if EN is enabled, the device will start up. If V_{IN} falls below $V_{IN,UVLO}$ by more than the input UVLO hysteresis, switching actions are again suppressed.

Enable and Adjusting Input Undervoltage Lockout

The EN pin provides programmable ON/OFF control using an external resistor-divider and has accurate rising and falling thresholds. The SY21113I will operate while the EN pin voltage exceeds the rising threshold. If the EN pin voltage is pulled below the falling threshold, the regulator will stop switching and enter shutdown state.



It is not recommended to connect EN to the IN node directly. A resistor with a value between 1kΩ and 1MΩ is recommended if the EN pin is pulled high to the IN node.

Soft-Start

The SY21113I has a built-in soft-start to control the rise rate of the output voltage and limit the input current surge during IC startup. The typical soft-start time is 1ms.

Output Auto-Discharge Function

The SY21113I discharges the output voltage when the regulator shuts down from V_{IN} UVLO, EN, or overtemperature protection, so that the output voltage can be discharged in a minimal time, even when the output load current is zero.

Fault-Protection Modes

Overcurrent and Short-Circuit Protection

If the top FET current exceeds the top current-limit threshold, the top FET will turn off and the bottom FET will turn on. If the bottom FET current exceeds the bottom current-limit threshold, the bottom FET will remain on until the bottom FET current decreases below the bottom current-limit threshold. As a result, both inductor peak and valley currents are limited. If the output current continues to increase, the output voltage will drop. If the output voltage falls below 33% of the regulation level, an output-short condition is detected and the SY21113I will operate in hiccup mode. The hiccup on-time is 2ms and the hiccup off-time is 6ms. If the hard short is removed, the SY21113I will return to normal operation.

Overtemperature Protection (OTP)

The device includes overtemperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. This will shut down the device when the junction temperature exceeds 150°C. Once the junction temperature cools by approximately 15°C, the device will resume normal operation after a complete soft-start cycle. For continuous operation, provide adequate cooling so that the junction temperature will not exceed the OTP threshold.

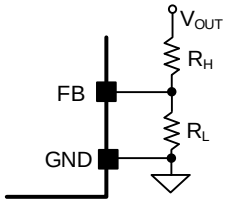
Application Information

The selection process for the input capacitor C_{IN}, output capacitor C_{OUT}, output inductor L, and feedback resistors R_H and R_L is described in the following sections.

Feedback Resistor-Divider R_H and R_L

Choose R_H and R_L to program the proper output voltage. A value between 1kΩ and 1MΩ is recommended for both resistors to minimize power consumption under light loads. If V_{OUT} = 3.3V and R_H is chosen as 100kΩ, for example, then R_L can be calculated as follows:

$$R_L = \frac{0.6}{V_{OUT} - 0.6V} \times R_H$$



With a calculated value of 22.2kΩ for R_L, a standard 1% 22.1kΩ resistor is selected.

Input Capacitor C_{IN}

For the best performance, select a typical X5R or better grade ceramic capacitor with a 10V rating, and at least 10μF capacitance. The capacitor should be placed as close as possible to the device, while also minimizing the loop area formed by C_{IN} and the IN/GND pins.

When selecting an input capacitor, ensure that its voltage rating is at least 20% greater than the maximum voltage of the input supply. X5R or X7R dielectric types are the most often selected due to their small size, low cost, surge current capability, and high RMS current rating over a wide temperature and voltage range.

In situations where the input rail is supplied through long wires, it is recommended to add some bulk capacitance like electrolytic-, tantalum-, or polymer-type capacitors to reduce the overshoot and ringing caused by the added parasitic inductance.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

The worst-case condition occurs at D = 0.5, then

$$I_{CIN\_RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplicity, use an input capacitor with an RMS current rating greater than 50% of the maximum load current.

The input capacitor value determines the input voltage ripple of the converter. If there is a voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification.

Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated using the formula:

$$V_{CIN\_RIPPLE,CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1 - D)$$

The worst-case condition occurs at D = 0.5, then

$$V_{CIN\_RIPPLE,CAP,MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. A single 10μF X5R capacitor is sufficient in most applications.

Output Inductor L

Consider the following when choosing this inductor:

1) Choose the inductance to provide a ripple current that is approximately 40% of the maximum output current. The recommended inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT} / V_{IN,MAX})}{f_{sw} \times I_{OUT,MAX} \times 0.4}$$

where f_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY21113I has tolerance for ripple current amplitude variation. As a result, the final choice of inductance can vary slightly from the calculated value with no significant performance impact.

2) The inductor's saturation current rating must be greater than the peak inductor current under full load:

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{2 \times f_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. Use an inductor with DCR less than 20mΩ to achieve good overall efficiency.

Output Capacitor C_{OUT}

Select the output capacitor C_{OUT} to handle the output ripple requirements. Both steady-state ripple and transient requirements must be taken into consideration when selecting C_{OUT}. For the best performance, use an X5R or better grade ceramic capacitor with a 16V rating, and capacitance of at least 22μF.

For applications where the design must meet stringent ripple requirements, the following considerations must be followed.

The output voltage ripple at the switching frequency is caused by the inductor-current ripple (ΔI_L) on the output capacitor's ESR (ESR ripple), as well as the stored charge (capacitive ripple). When calculating total ripple, consider both.

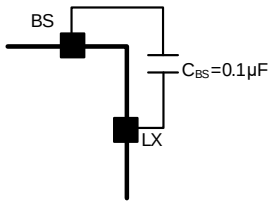
$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

The capacitive ripple might be higher because the effective capacitance for ceramic capacitors decreases with the voltage across the terminals. The voltage derating is usually included as a chart in the capacitor datasheet, and the ripple can be recalculated after taking the target output voltage into account.

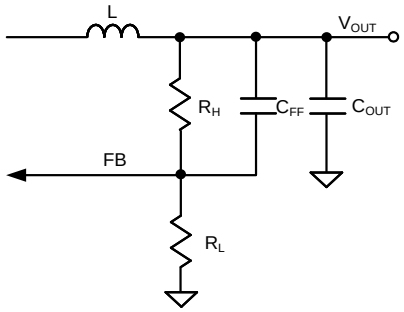
External Bootstrap Capacitor

The external bootstrap capacitor provides the gate driver voltage for the N-channel top FET. A 0.1μF low-ESR ceramic capacitor connected between the BS pin and the LX pin is recommended.

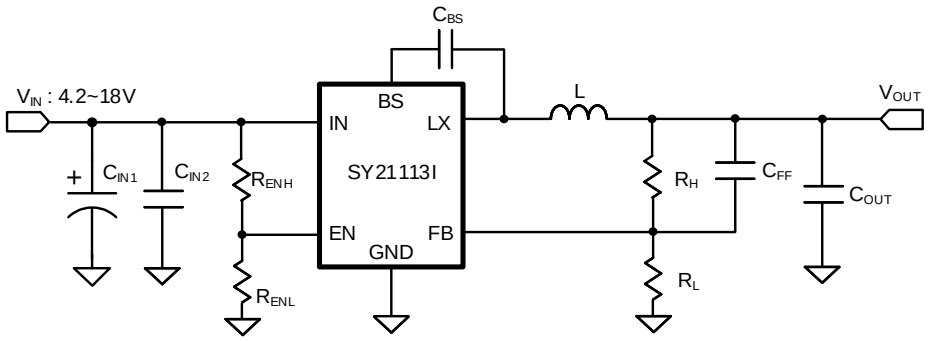


Load-Transient Considerations

The SY21113I integrates compensation components to achieve fast transient response and improved stability. In some applications, adding a ceramic capacitor (feed-forward capacitor C_{FF}) in parallel with R_H may further speed up the load-transient response, and is therefore recommended for applications with large load-transient step requirements.



Application Schematic (V_{OUT} = 3.3V)



BOM List

Reference Designator	Description	Part Number	Manufacturer
C_{IN1}	47μF/50V Electrolytic Capacitor		
C_{IN2}	10μF/25V/X7R, 1206	C3216X7R1E106K	TDK
C_{OUT}	10μF/16V/X5R, 1206	C3225X5R1C106K	TDK
C_{BS}	0.1μF/50V/X7R, 0603	C1608X7R1H104K	TDK
C_{FF}	100pF/50V/C0G, 0603	C1608C0G1H101J	TDK
L	4.7μH/inductor, 3.8A	VLS6045EX-4R7M	TDK
R_H	100kΩ, 1%, 0603		
R_L	22.1kΩ, 1%, 0603		
R_{ENH}	10kΩ, 1%, 0603		
R_{ENL}	1MΩ, 1%, 0603		

Recommended Component Values for Typical Applications

V_{OUT}(V)	R_H(kΩ)	R_L(kΩ)	C_{FF}(pF)	L/Part Number	C_{OUT}
1.2	100	100	22	2.2μH/VLS6045EX-2R2N	22μF/16V, 1206, X5R
1.8	100	49.9	22	3.3μH/VLS6045EX-3R3N	10μF/16V, 1206, X5R
3.3	100	22.1	100	4.7μH/VLS6045EX-4R7M	10μF/16V, 1206, X5R
5	100	13.7	100	6.8μH/VLS6045EX-6R8M	10μF/16V, 1206, X5R

Layout Design

Follow these PCB layout guidelines for optimal performance and thermal dissipation:

- **Input Capacitors:** Place the input capacitors as close as possible to the IN and GND pins, minimizing the loop formed by these connections. The input capacitor should be connected to IN and GND by wide copper areas.
- **Output Capacitors:** Connect the C_{OUT} negative terminal to the GND pin using wide copper traces instead of vias, in order to achieve better accuracy and stability of output voltage.
- **Feedback Network:** Place the feedback components (R_H, R_L, and C_{FF}) as close to the FB pin as possible. Avoid routing the feedback line near LX or other high-frequency signals, as it is noise-sensitive. Use a Kelvin connection to connect with C_{OUT} rather than the inductor output terminal.
- **LX Connection:** Keep the LX area small to prevent excessive EMI, while providing a wide copper area to minimize parasitic resistance and inductance.
- **EN Signal:** It is not recommended to connect the EN signal directly to V_{IN}. A resistor in the range of 1kΩ to 1MΩ should be used if the lines are pulled high to V_{IN}.
- **GND Vias:** Place an adequate number of vias on the GND layer around the device for better thermal performance. The exposed GND pad should be connected to a copper area larger than its size. Place multiple GND vias on it for heat dissipation.
- **PCB Board:** To achieve the best thermal performance and reduce switching noise, maximize the PCB copper area connecting to the GND pin. A ground plane is highly recommended if board space allows. Connect the ground pad to a large copper area to enhance thermal performance.

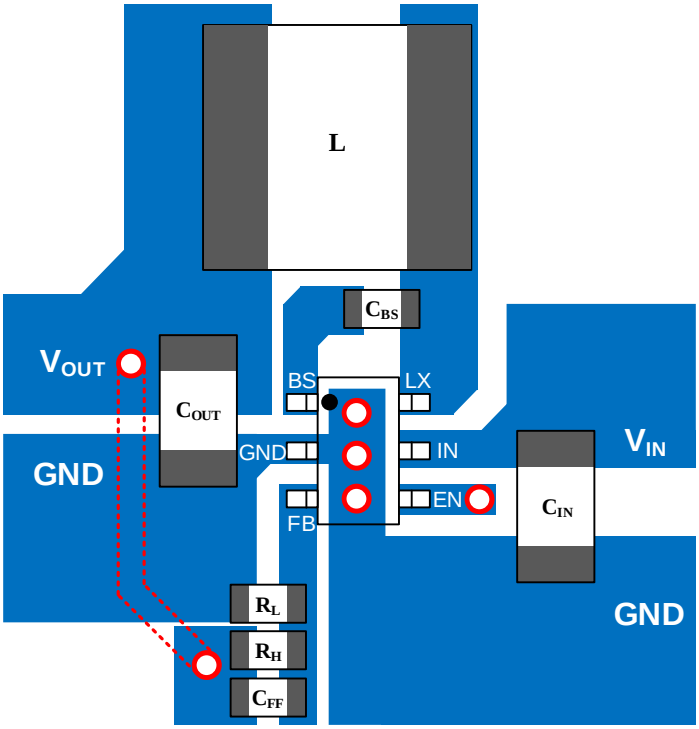
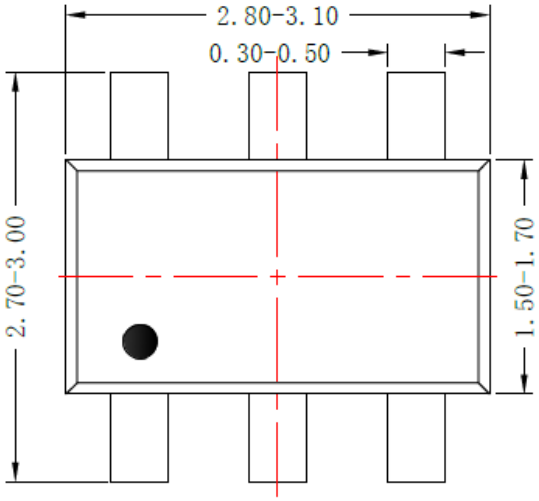
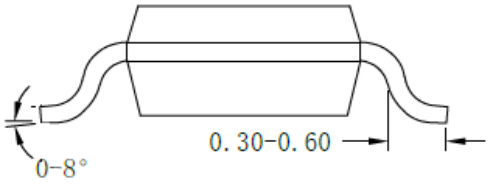


Figure3. Suggested PCB Layout

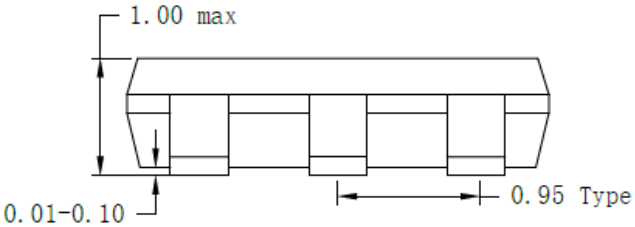
TSOT23-6 Package Outline and PCB Layout



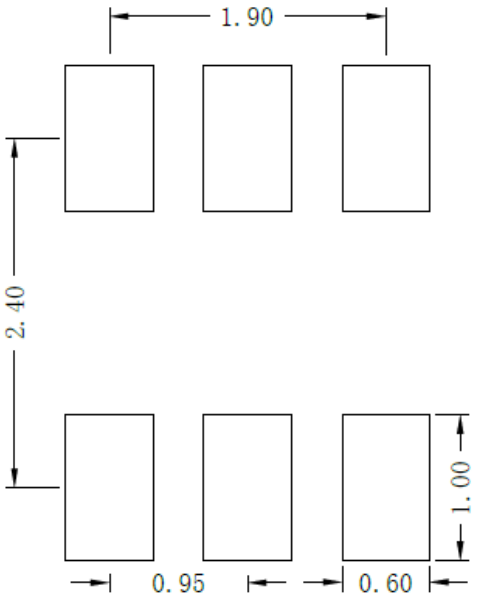
Top view



Side view



Front view

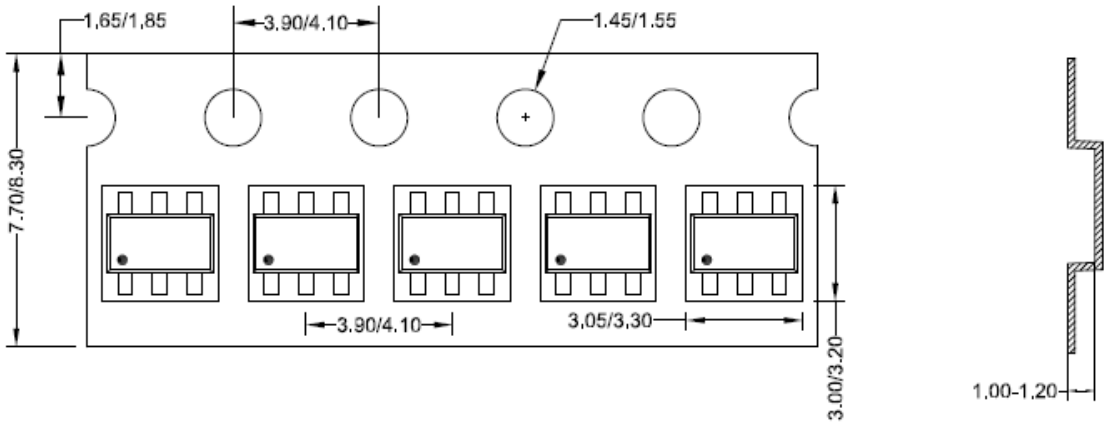


Recommended Pad Layout

Note: *All dimensions are in millimeters and exclude mold flash and metal burr.*

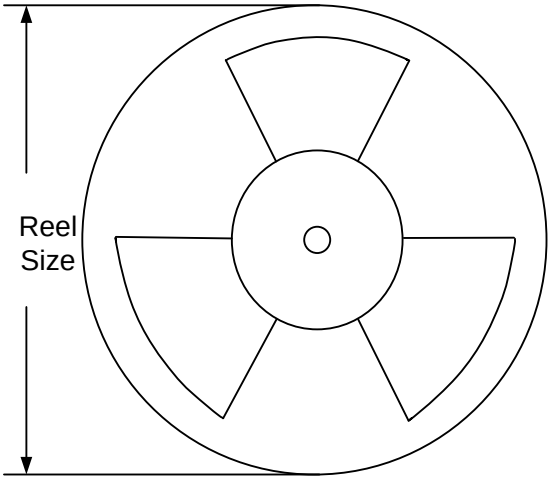
Taping and Reel Specification

TSOT23-6 taping orientation



Feeding direction →

Carrier tape and reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
TSOT23-6	**8**	**4**	**7**	**400**	**160**	**3000**

Others: NA

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Nov.14, 2022	Revision 0.9C	Updated the lead width of package (Page 11)
Jan.14, 2021	Revision 0.9B	Add “RoHS Compliant and Halogen Free “ in Features
Oct. 30, 2018	Revision 0.9A	Update in EC table (Page 4): 1. Add max value of Quiescent Current (280μA); 2: Add max value of Top FET Ron (120mΩ); 3: Add max value of Bottom FET Ron (60mΩ); 4: Add min value of Soft-start Time (0.5ms); 5: Add max value of Soft-start Time (1.5ms)
Sep.21, 2018	Revision 0.9	Initial Release

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