SY20114

High-Efficiency, 1.5MHz 2A Synchronous Step-Down Regulator

General Description

The SY20114 high-efficiency 1.5MHz synchronous step-down DC/DC regulator operates over a wide input voltage range of 2.5V to 5.5V and can deliver an output current up to 2A with a low quiescent current of 55 µA. To minimize conduction loss, it integrates a main switch and a synchronous switch with very low $R_{DS(ON)}$.

The SY20114 is highly integrated, so only the input and output capacitors, inductor, and resistor-divider components need to be selected for the targeted application specifications.

The SY20114 is available in a space-saving, low-profile SOT563 package.

Features

- 2.5V–5.5V Input Voltage Range
- Up to 2A Output Current
- Low $R_{DS(ON)}$ for Internal Switches: 125mΩ Top, 75mΩ Bottom
- Low 55µA Quiescent Current
- High 1.5MHz Switching Frequency Minimizes Required External Components
- Internal Soft-Start Limits Inrush Current
- 100% Dropout Operation
- Power-Good Indicator
- Hiccup Mode for Short-Circuit Protection
- Output Auto-Discharge Function
- RoHS-Compliant and Halogen-Free
- Compact SOT563 Package

Applications

- Set-Top Box
- USB Dongle
- Media Player
- Smartphone

Typical Application

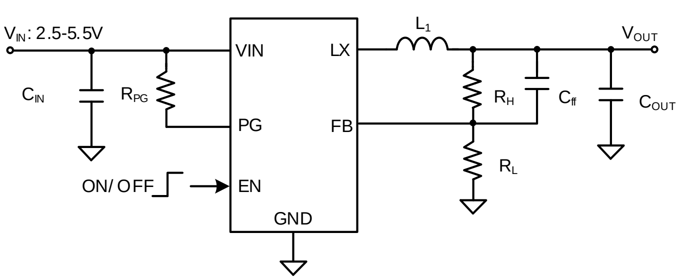


Figure 1. Schematic Diagram

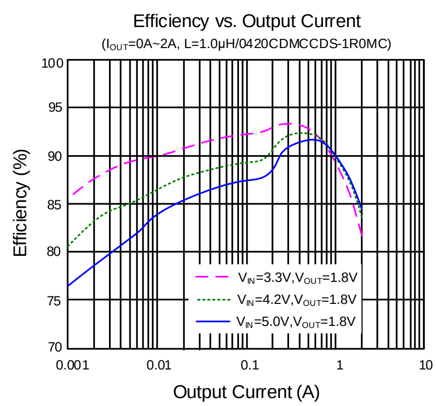
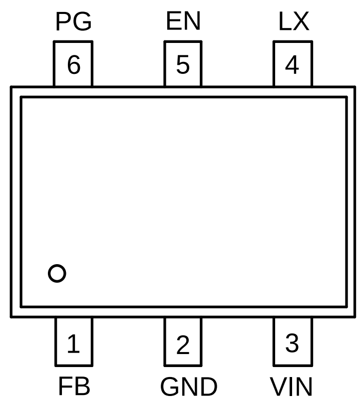


Figure 2. Efficiency vs. Output Current

Ordering Information

Ordering Part Number	Details
SY20114**ARC**	PFM Operation Pin 6 Power-Good (PG)
SY20114**BARC**	PFM Operation Pin 6 NC (No PG)
SY20114**EARC**	Forced PWM Operation Pin 6 Power-Good (PG)
SY20114**FARC**	Forced PWM Operation Pin 6 NC (No PG)

Pinout (top view)*



*Pin 6 is NC for SY20114BARC and SY20114FARC

Package Information

Part Number	Top Mark	Package type
SY20114**ARC**	**M4*xyz***	SOT-563 RoHS-Compliant, Halogen-Free
SY20114**BARC**	**M5*xyz***	
SY20114**EARC**	**E3*xyz***	
SY20114**FARC**	**M6*xyz***	

***x* = year code, *y* = week code, *z* = lot number code**

Pin Description

Pin No	Pin Name	Pin Description
1	FB	Output feedback pin. Connect this pin to the center point of the output resistor-divider (as shown in Figure 1) to program the output voltage: $V_{OUT} = 0.6 \times (1 + R_H/R_L)$.
2	GND	Ground pin
3	V_{IN}	Input pin. Decouple this pin from the GND pin with a minimum 10µF ceramic capacitor.
4	LX	Inductor pin. Connect this pin to the switching node of the inductor.
5	EN	Enable control pin. Pull high to turn on. Do not leave floating.
6	PG	SY20114ARC/SY20114EARC: Power-good indicator (open-drain output). The PG pin is high-impedance if the output is between 90% and 120% of the regulation voltage; otherwise, it is driven low. Connect a pullup resistor to the input.
	NC	SY20114BARC/SY20114FARC: NC, leave it floating or connected to GND.

Block Diagram

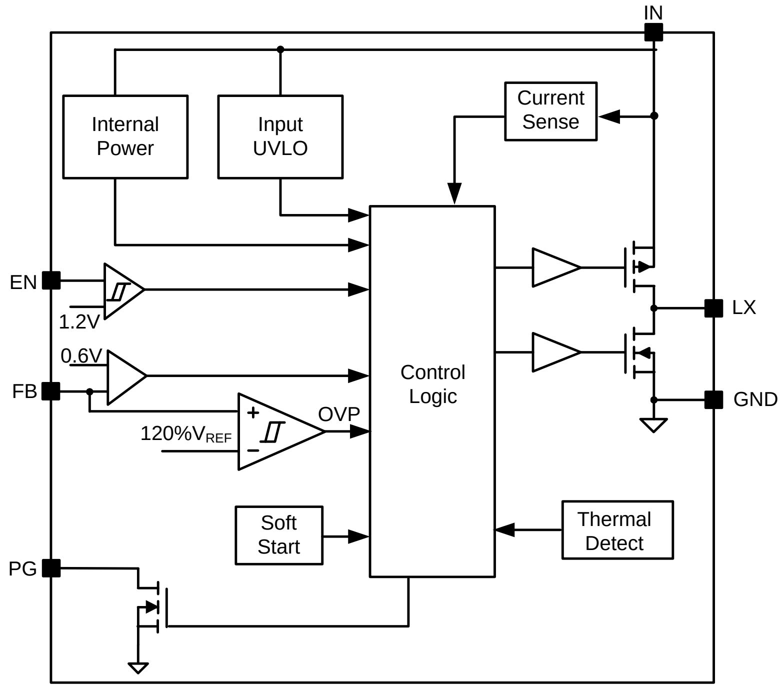


Figure 3. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
IN	-0.3	6	V
EN, FB, PG	-0.3	IN + 0.6	
LX	-0.3	6	
LX, 20ns duration	-3	7	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering,10s)		260	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 2)	Min	Max	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance		90	°C/W
θ_{JC} Junction-to-Case Thermal Resistance		20	
P_D Power Dissipation $T_A = 25°C$		1.11	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
IN	2.5	5.5	V
Output Voltage	0.6	5.5	
Output Current		2	A
Junction Temperature	-40	125	°C

Electrical Characteristics

(V_{IN} = 5V, V_{OUT} = 1.8V, L = 1.0μH, C_{OUT} = 22μF, T_J = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input	Voltage	V_{IN}		2.5		5.5	V
	UVLO, rising	$V_{IN,UVLO}$			2.45	2.5	V
	UVLO, hysteresis	$V_{IN,HYS}$			150		mV
	Quiescent current	I_Q	V_{FB} = 105% × V_{REF} (For SY20114ARC and SY20114BARC Only)		55		μA
	Shutdown current	I_{SHDN}	V_{EN} = 0V		0.1	1	μA
FB	Reference voltage	V_{REF}	I_{OUT} = 1A, CCM	0.591	0.6	0.609	V
	Input current	I_{FB}	V_{EN} = 2V, V_{FB} = 1V	-50	0	50	nA
Power Switch	On-resistance	$R_{DS(ON),HS}$			125		mΩ
	Current limit	$I_{LMT,HS}$		3			A
Synchronous Rectifier	On-resistance	$R_{DS(ON),LS}$			75		mΩ
Discharge FET Resistance		R_{DIS}			50		Ω
Enable (EN)	Input voltage high	$V_{EN,H}$		1.2			V
	Input voltage low	$V_{EN,L}$				0.4	V
	Input current	I_{EN}	V_{EN} = 2V			2	μA
Soft-Start (SS)	Turn-on delay time	$t_{ON,DLY}$	From EN high to LX start switching		0.25		ms
	Soft-start time	t_{SS}	V_{OUT} from 0% to 100%		0.75		ms
Undervoltage Protection	Threshold	V_{UVP}			50		%V_{REF}
	Delay	$t_{UVP,DLY}$			10		μs
UVP/OCP Hiccup ON Time		$t_{HICCUP,ON}$			1.45		ms
UVP/OCP Hiccup OFF Time		$t_{HICCUP,OFF}$			1.45		ms
Power-Good (SY20114ARC and SY20114EARC only)	Thresholds	V_{PG}	V_{FB} falling, fault		88		%
			V_{FB} rising, good		90		%
			V_{FB} rising, fault		120		%
			V_{FB} falling, good		114		%
	Delay	$t_{PG,R}$	V_{FB} rising, good		2		μs
		$t_{PG,F}$	V_{FB} falling, fault		20		μs
Switching Frequency		f_{SW}	I_{OUT} = 1A, CCM		1.5		MHz
Minimum ON Time		$t_{ON,MIN}$			50		ns
Maximum Duty Cycle		D_{MAX}		100			%
Thermal Shutdown Temperature		T_{SD}			160		°C
Thermal Shutdown Hysteresis		T_{HYS}			20		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} of SY20114ARC is measured in the natural convection at T_A = 25°C on a 2OZ two-layer Silergy evaluation board. Pin 4 is the case position for SY20114ARC θ_{JC} measurement.

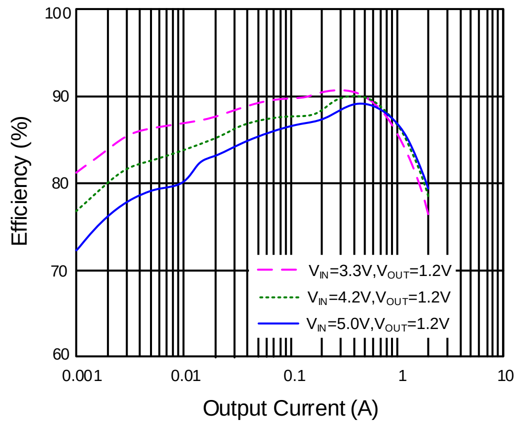
Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

(SY20114ARC, T_A = 25°C, V_{IN} = 5V, V_{OUT} = 1.8V, L = 1.0μH, C_{OUT} = 22μF, unless otherwise noted)

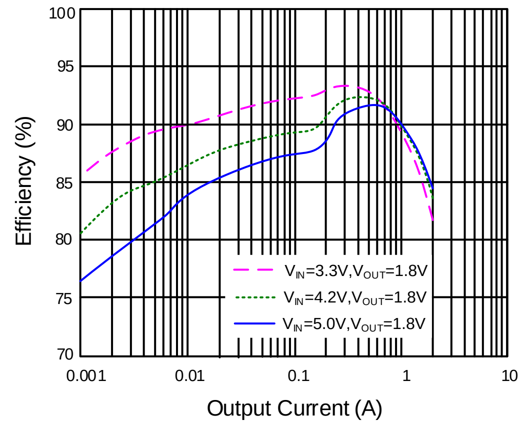
Efficiency vs. Output Current

(I_{OUT}=0A~2A, L=1.0μH/0420CDMCCDS-1R0MC)



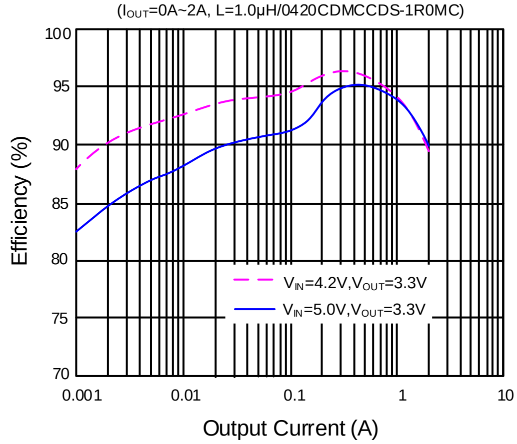
Efficiency vs. Output Current

(I_{OUT}=0A~2A, L=1.0μH/0420CDMCCDS-1R0MC)



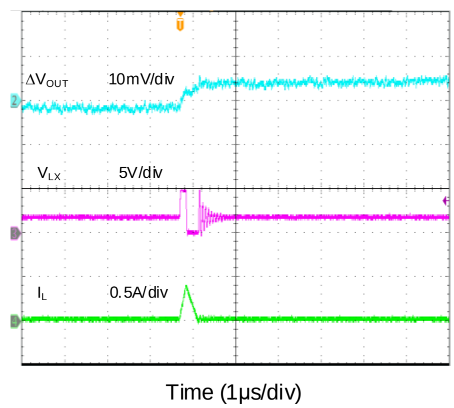
Efficiency vs. Output Current

(I_{OUT}=0A~2A, L=1.0μH/0420CDMCCDS-1R0MC)



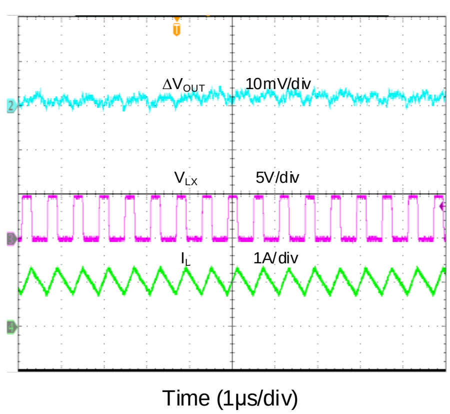
Output Ripple

(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=0A)



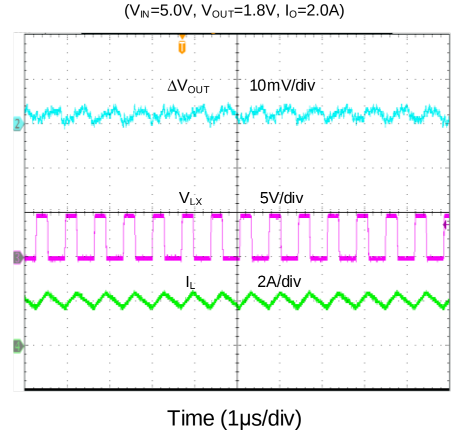
Output Ripple

(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=1.0A)



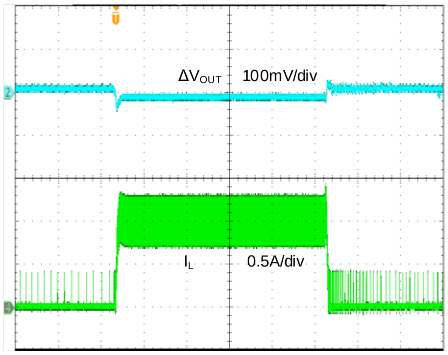
Output Ripple

(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=2.0A)



Load Transient

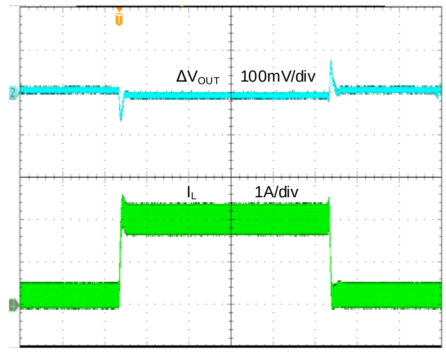
(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=0A ~ 1A)



Time (100μs/div)

Load Transient

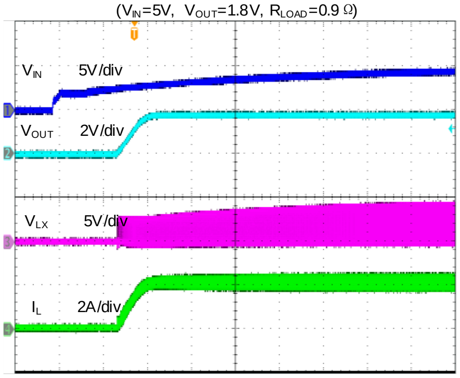
(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=0.2A ~ 2A)



Time (100μs/div)

Startup from V_{IN}

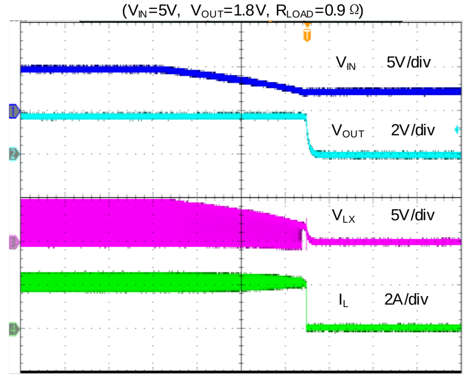
(V_{IN}=5V, V_{OUT}=1.8V, R_{LOAD}=0.9 Ω)



Time (800 μs/div)

Shutdown from V_{IN}

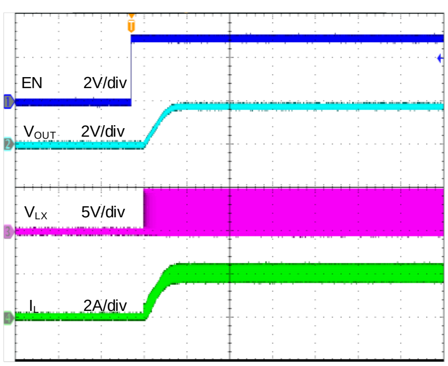
(V_{IN}=5V, V_{OUT}=1.8V, R_{LOAD}=0.9 Ω)



Time (400 μs/div)

Startup from Enable

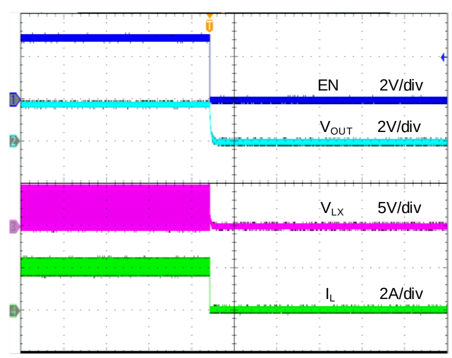
(V_{IN}=5.0V, V_{OUT}=1.8V, R_{LOAD}=0.9Ω)



Time (800μs/div)

Shutdown from Enable

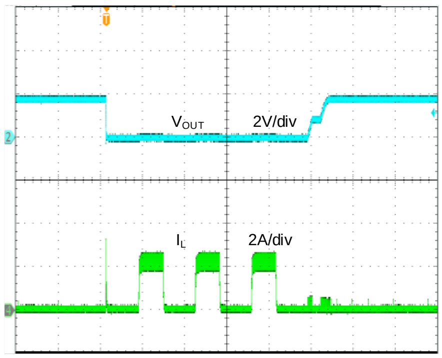
(V_{IN}=5.0V, V_{OUT}=1.8V, R_{LOAD}=0.9Ω)



Time (800μs/div)

Short Circuit Protection

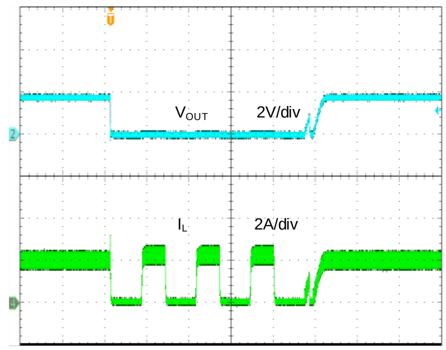
(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=0A ~ Short)



Time (2ms/div)

Short Circuit Protection

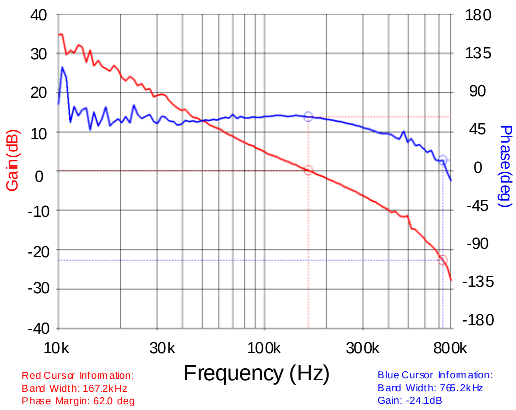
(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=2A ~ Short)



Time (2ms/div)

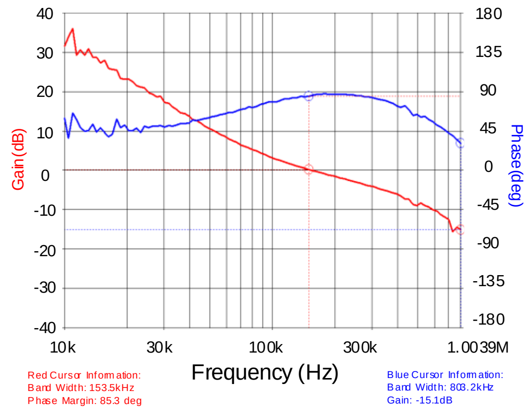
Bode Plot

(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=2A)



Bode Plot

(V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=2A)



Operation

The SY20114 high-efficiency 1.5MHz synchronous step-down DC/DC regulator operates over a wide input-voltage range of 2.5V to 5.5V and can deliver an output current up to 2A with a low quiescent current of 55 µA. To minimize conduction loss, it integrates a main switch and a synchronous switch with very low $R_{DS(ON)}$.

The SY20114 employs a constant-off-time and peak-current-mode control strategy. When the top FET's current-sense signal reaches internal V_{COMP}, the top FET turns off and the bottom FET turns on for a fixed period of time (constant t_{OFF}). t_{OFF} is internally calculated according to the input voltage, output voltage, and desired switching frequency (f_{SW}):

$$t_{OFF} = \frac{1 - V_{OUT}/V_{IN}}{f_{SW}}$$

The bottom FET turns off after a period of t_{OFF}.

The SY20114 is available in a space-saving, low-profile SOT563 package.

Application Information

The SY20114 is highly integrated, so only the following components need to be selected for the targeted application specifications: input capacitor C_{IN}, output capacitor C_{OUT}, output inductor L, and feedback resistors R_H and R_L.

Feedback Resistor-Divider R_H and R_L

Choose R_H and R_L to program the proper output voltage. A value between 1kΩ and 1MΩ is recommended for both resistors. If R_L is chosen as 120kΩ, then R_H can be calculated as follows:

$$R_H = \frac{(V_{OUT} - 0.6\,V) \times RL}{0.6V}$$

Input Capacitor C_{IN}

For the best performance, select a typical X5R or better grade ceramic capacitor with a 10V rating, and greater than 10µF capacitance. The capacitor should be placed as close as possible to the device, while also minimizing the loop area formed by C_{IN} and the IN/GND pins. When selecting an input capacitor, ensure that its voltage rating is at least 20% greater than the maximum voltage of the input supply. X5R or X7R dielectric types are the most often selected due to their small size, low cost, surge current capability, and high RMS current rating over a wide temperature and voltage range.

In situations where the input rail is supplied through long wires, it is recommended to add some bulk capacitance like electrolytic, tantalum or polymer type capacitors to reduce the overshoot and ringing caused by the added parasitic inductance.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

The worst-case condition occurs at D = 0.5, then

$$I_{CIN\_RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor value determines the input voltage ripple of the converter. If there is a voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification.

Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated using the formula:

$$V_{CIN\_RIPPLE,CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1 - D)$$

The worst-case condition occurs at D = 0.5, then

$$V_{CIN\_RIPPLE,CAP,MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. A single 10µF X5R capacitor is sufficient in most applications.

Output Capacitor C_{OUT}

Select the output capacitor C_{OUT} to handle the output ripple requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting the component. For the best performance, use an X5R or better grade ceramic capacitor with a 6.3V rating, and capacitance greater than 22µF.

For applications where the design must meet stringent ripple requirements, the following considerations must be followed:

The output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔI_L) on the output capacitor's ESR (ESR ripple), as well as the stored charge (capacitive ripple).

When calculating total ripple, consider both.

$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

The capacitive ripple might be higher because the effective capacitance for ceramic capacitors decreases with the voltage across the terminals. The voltage derating is usually included as a chart in the capacitor datasheet, and the ripple can be recalculated after taking the target output voltage into account.

Output Inductor L

There are several considerations in choosing this inductor:

1) Choose the inductance to provide a ripple current that is approximately 40% of the maximum output current. The recommended inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT} / V_{IN,MAX})}{f_{sw} \times I_{OUT,MAX} \times 0.4}$$

where f_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

2) The saturation current rating of the inductor must be greater than the peak inductor current under full-load conditions:

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{2 \times f_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is recommended to choose an inductor with DCR less than 50mΩ to achieve good overall efficiency.

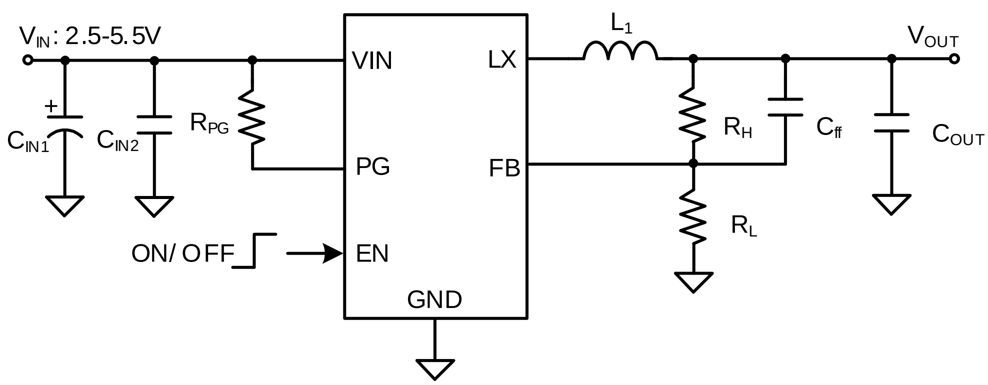
Overcurrent and Short-Circuit Protection

With load current increasing, as soon as the high-side FET current exceeds the peak current-limit threshold, the high-side FET will turn off. If the load current continues to increase, the output voltage will drop. When the output voltage falls below 50% of the regulation level, the output undervoltage protection will be activated and the SY20114 will operate in hiccup mode. The hiccup frequency is 400Hz and the hiccup duty cycle is 50%. If the hard short is removed, the SY20114 will return to normal operation.

Load-Transient Considerations

The SY20114 integrates the compensation components to achieve good stability and fast transient responses. In some applications, adding a ceramic capacitor (feed-forward capacitor C_{ff}) in parallel with R_H may further speed up the load-transient responses, and is therefore recommended for applications with large load-transient step requirements.

Application Schematic (V_{OUT} = 1.8V)



BOM List

Reference Designator	Description	Part Number	Manufacturer
L_1	1.0µH	0420CDMCCDS-1R0MC	Sumida
C_{IN1}	100µF/25V(electrolytic capacitor)		
C_{IN2}	10µF/10V, 0805, X5R	C2012X5R1A106K	TDK
C_{OUT}	22µF/6.3V, 0805, X5R	C2012X5R0J226M	TDK
C_{ff}	22pF/50V, 0603, C0G	C1608C0G1H220J	TDK
R_H	100kΩ, 1%, 0603		
R_L	49.9kΩ, 1%, 0603		
R_{PG}	100kΩ, 0603		

Recommended Component Values for Typical Applications

V_{OUT}(V)	R_H(kΩ)	R_L(kΩ)	C_{FF}(pF)	L/(Rated/Saturating Current)	C_{OUT}
1.2	49.9	49.9	22	1.0µH/(6.5A/8A)	22µF/6.3V, 0805, X5R
1.8	100	49.9	22	1.0µH/(6.5A/8A)	22µF/6.3V, 0805, X5R
3.3	100	22.1	22	1.0µH/(6.5A/8A)	22µF/6.3V, 0805, X5R

Layout Design

For optimal design, follow these PCB layout considerations:

- For maximum efficiency and minimal noise, the following components should be placed close to the IC: C_{IN}, L, R_H and R_L.
- To achieve the best thermal and noise performance, maximize the PCB copper area connecting to the GND pin. A ground plane is highly recommended if board space allows. Connect the ground pad to a large copper area to enhance thermal performance.
- C_{IN} must be close to pins IN and GND. Minimize the loop area formed by C_{IN}, V_{IN}, and GND.
- To reduce potential noise:
  - Minimize the PCB copper area connected to the LX pin.
  - R_H, R_L, and the trace connecting to the FB pin must **not** be adjacent to the LX net on the PCB layout.

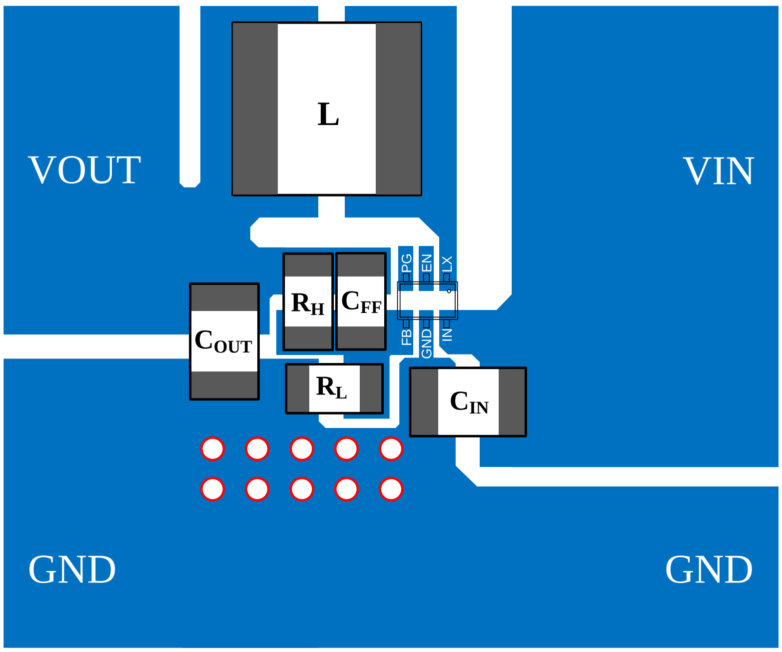
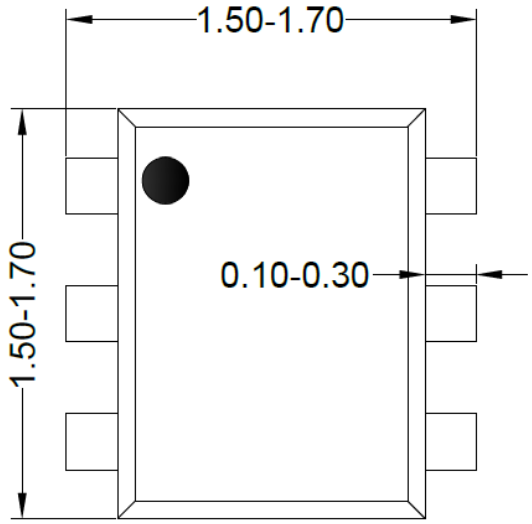
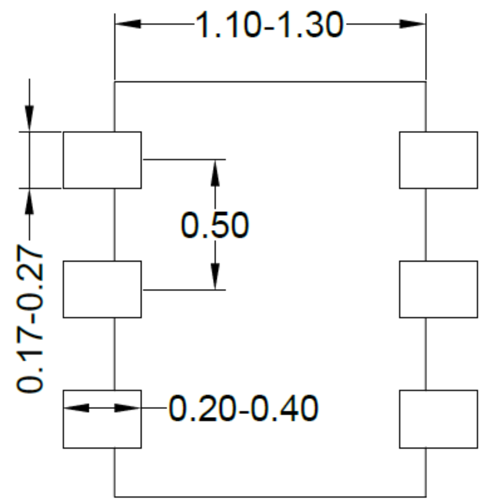


Figure 3. Suggested PCB Layout

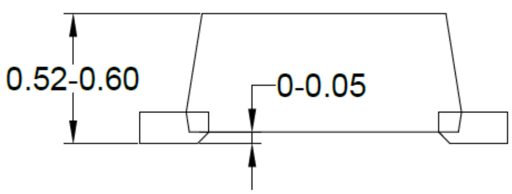
SOT563 Package Outline Drawing



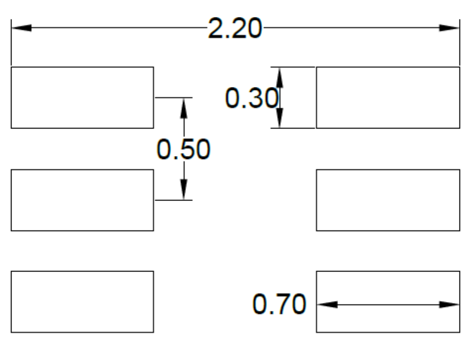
Top view



Bottom view



Side View



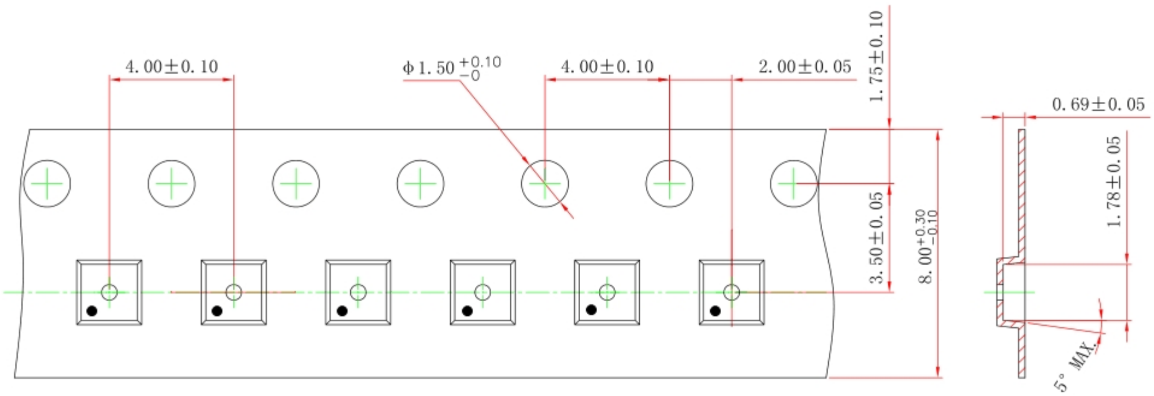
Recommended PCB layout
(Reference only)

Note: *All dimensions are in millimeters and exclude mold flash and metal burr.*

Taping and Reel Specification

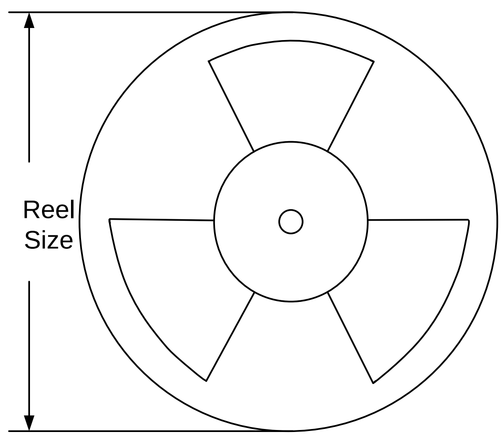
Taping Orientation

SOT563



Feeding Direction →

Carrier Tape and Reel Specification for Packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel (pcs)
SOT563	8	4	7"	280	160	5000

Others: NA

Revision History

The revision history provided is for informational purposes only and is believed to be accurate; however, it is not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change
Jun. 11, 2020	Revision 0.9	Initial Release
Jun. 11, 2021	Revision 1.0	Production Release

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