

General Description

The SY20867F is a compact supervisory circuit that monitors voltages greater than 500mV with 0.25% threshold accuracy. The output assertion delay time can be adjusted using an external capacitor. The device features a logic high enable pin to control the power on and off the internal logic.

Operating within a voltage range of 1.7V to 6.5V, the SY20867F has a typical quiescent current of 9μA and an open-drain output rated at 18V.

The device is available in an ultra-small DFN 1.45mm×1.0mm–6pin package and is fully specified for operation over a temperature range of T_J=-40°C to 125°C.

Features

- Operating Voltage Range: 1.7V to 6.5V
- Adjustable Threshold Down to 500mV
- Threshold Accuracy: 1% Over temperature
- Capacitor-adjustable Delay Time
- Low Quiescent Current: 9μA (typ.)
- External Enable Input
- Open Drain Output (Rated at 18V)
- Temperature Range: -40°C to 125°C
- RoHS Compliant and Halogen Free
- Compact Package: DFN1.45×1-6

Applications

- Notebook and Desktop Computers
- Microcontrollers, DSPs, and Microprocessors
- Portable and Battery-Powered Products
- FPGAs and ASICs

Typical Application

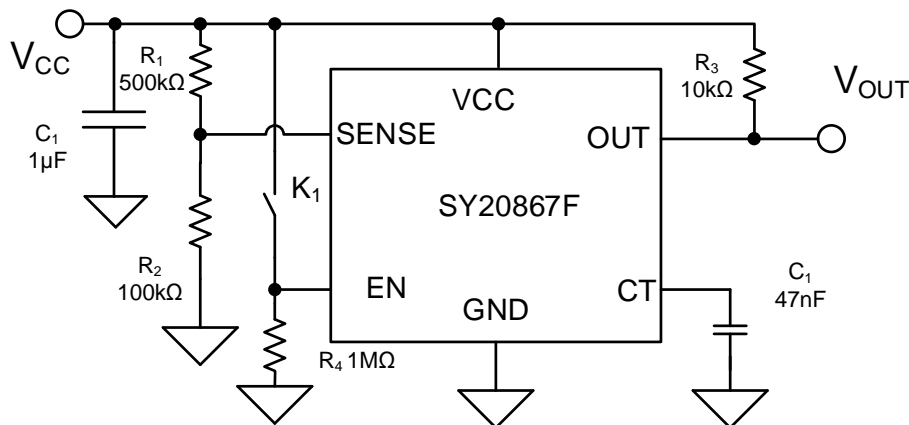


Figure1. Schematic Diagram

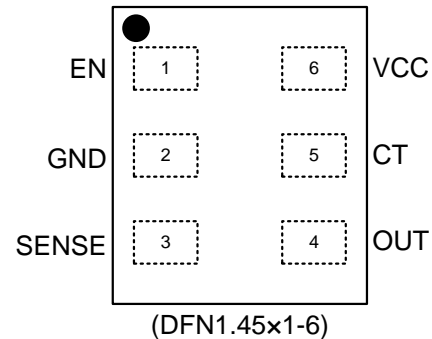
Ordering Information

Pinout (Top View)

Ordering Number	Package Type	Top Mark
SY20867FDTC	DFN1.45x1-6 RoHS Compliant and Halogen Free	Vxyz

Device code: V

x=year code, y=week code, z= lot number code



Pin Name	Pin NO.	I/O	Pin Description
EN	1	I	Active high input. Driving EN low immediately makes OUT go low, independent of V_{SENSE} . With V_{SENSE} already above V_{IT+} , drive EN high to make OUT go high after $0.2\mu s$.
GND	2		Ground pin.
SENSE	3	I	This pin is connected to the voltage that is monitored with the use of an external resistor. The output asserts after the capacitor-adjustable delay time when V_{SENSE} rises above $0.5V$ and EN is asserted. The output de-asserts after a minimal propagation delay ($16\mu s$) when V_{SENSE} falls below $V_{IT+} - V_{HYS}$.
OUT	4	O	OUT is an open drain output that is immediately driven low after V_{SENSE} falls below $(V_{IT+} - V_{HYS})$ or the EN input is low. OUT goes high after the capacitor-adjustable delay time when V_{SENSE} is greater than V_{IT+} and the EN pin is high. Open drain device can be pulled up to $18V$ independent of VCC; Pull-up resistors are required for these devices.
CT	5	I	Capacitor-adjustable delay. The CT pin offers a user-adjustable delay time. Connecting this pin to a ground referenced capacitor sets the delay time for SENSE rising above $0.5V$ to OUT asserting. $t_{pd(r)}(s) = [C_{CT}(\mu F) \times 4] + 40\mu s$
VCC	6	I	Supply Voltage Input. Connect a $1.7V$ to $6.5V$ supply to VCC to power the device. It is good analog design practice to place a $0.1\mu F$ ceramic capacitor close to this pin.

Block Diagram

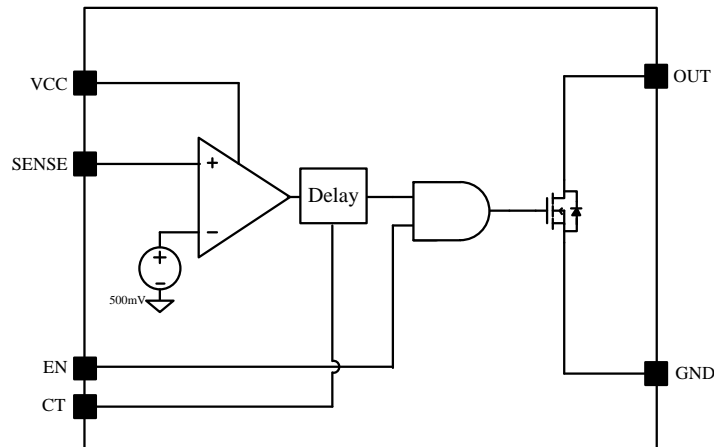


Figure2. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
VCC, EN, SENSE	-0.3	7	V
CT	-0.3	VCC + 0.3	
OUT (Open Drain)	-0.3	20	
OUT Current	-10	10	mA
Lead Temperature (Soldering, 10s)		260	°C
Junction Temperature, Operating	-40	125	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	293.8	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	165.1	
P_D Power Dissipation $T_A = 25^\circ\text{C}$	0.34	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
VCC	1.7	6.5	V
CT, EN, SENSE	0	6.5	
OUT (Open Drain)	0	18	
OUT Current	0.0003	1	mA



Electrical Characteristics

(1.7V < V_{CC} < 6.5V, typical values are at T_J = 25°C and V_{CC} = 3.3V, unless otherwise noted.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V _{CC}		1.7		6.5	V
Power on Reset Voltage	V _{POR}	V _{OL} (max) = 0.2V, I _{OUT} = 15μA (Note 4)		0.72		V
Supply Current (into VCC pin)	I _{CC}	V _{CC} =3.3V, T _A =25°C, no load		9	12	μA
		V _{CC} =6.5V, T _A =25°C, no load		11	13.5	μA
Positive-going Input Threshold Voltage	V _{IT+}	V _{SENSE} rising	0.495	0.5	0.505	V
Hysteresis Voltage	V _{HYS}	V _{SENSE} falling		5		mV
SENSE Input Current	I _{SENSE}	V _{SENSE} = 0V to V _{CC} (Note 5)	-15		15	nA
CT Pin Charge Current	I _{CT}		260	310	360	nA
CT Pin Comparator Threshold Voltage	V _{CT}		1.18	1.238	1.299	V
CT Pin Down Resistance	R _{CT}			200		Ω
Low-level Input Voltage	V _{IL}				0.4	V
High-level Input Voltage	V _{IH}		1.4			V
Under Voltage Lockout	V _{UVLO}	V _{CC} falling, (Note 6)	1.3		1.7	V
EN Leakage		EN/#EN = V _{CC} or GND	-100		100	nA
Low-level Output Voltage	V _{OL}	V _{CC} ≥ 1.2V, I _{SINK} = 90μA			0.3	V
		V _{CC} ≥ 2.25V, I _{SINK} = 0.5mA			0.3	V
		V _{CC} ≥ 4.5V, I _{SINK} = 1mA			0.4	V
Open-drain Output Leakage Current	I _{LKG(OD)}	V _{OUT} high impedance = 18V		20		nA

Timing Requirements

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SENSE (rising) to OUT Propagation Delay	t _{PD(r)}	V _{SENSE} rising, C _{CT} = open		40		μs
		V _{SENSE} rising, C _{CT} = 0.047μF		190		ms
SENSE (falling) to OUT Propagation Delay	t _{PD(f)}	V _{SENSE} falling		16		μs
Start-up Delay		(Note 7)		50		μs
EN Pin Minimum Pulse Duration	t _w		1			μs
EN Glitch Rejection	t _{EN_GLH}			100		ns
EN to OUT Delay Time (Output Disable)	t _{d_off}	EN de-asserted to output de-asserted		200		ns
EN to V _{OUT} Delay Time	t _{d_fix}	EN asserted to output asserted delay		200		ns

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Θ_{JA} is measured in the natural convection at $T_A = 25^\circ\text{C}$ on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions

Note 4: The lowest supply voltage (V_{CC}) at which output is active (OUT is low); $t_{r_VCC} > 15\mu\text{s/V}$. below V_{POR} , the output cannot be determined.

Note 5: Specified by design.

Note 6: When V_{CC} falls below the UVLO threshold, the output de-asserts (OUT goes low). Below V_{POR} , the output cannot be determined

Note 7: During power on, V_{CC} must exceed 1.7 V for at least $50\mu\text{s}$ (plus propagation delay time, $t_{PD(r)}$) before output is in the correct state.

Timing Sequence:

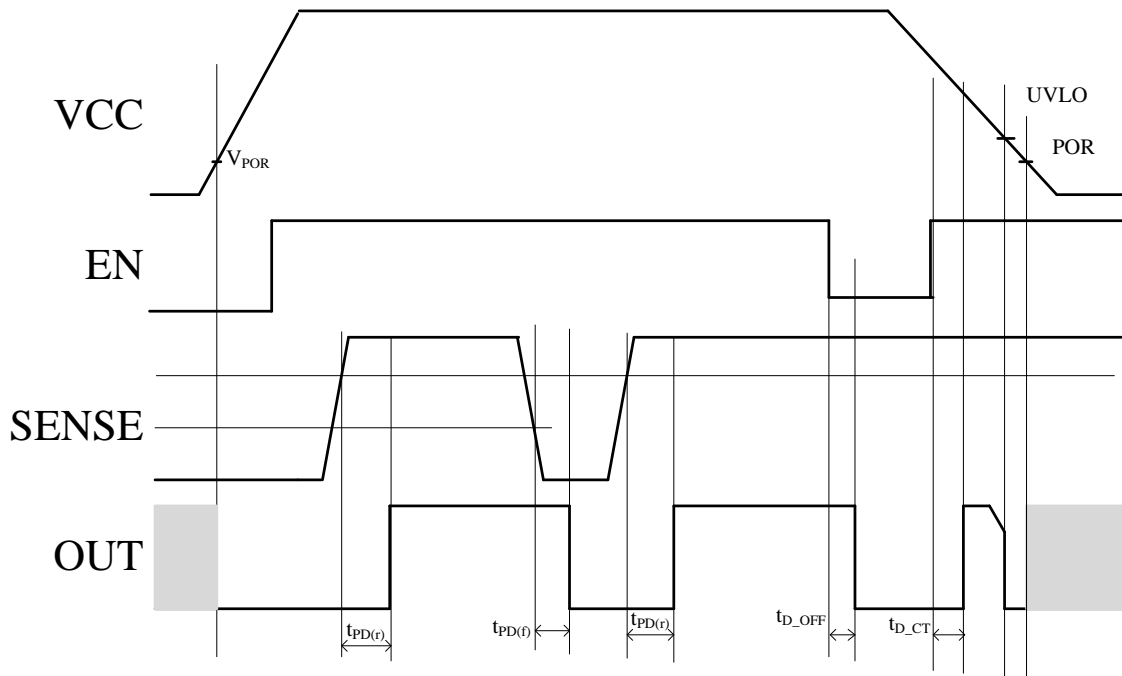
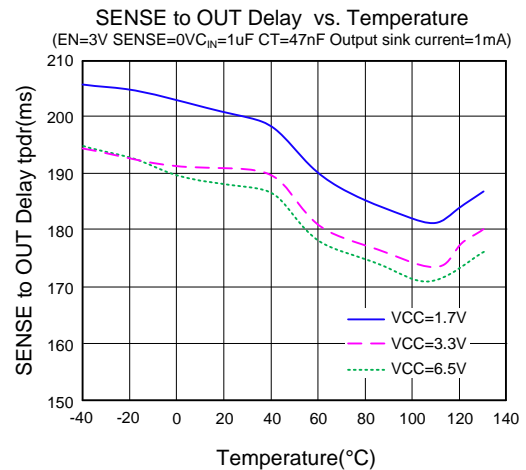
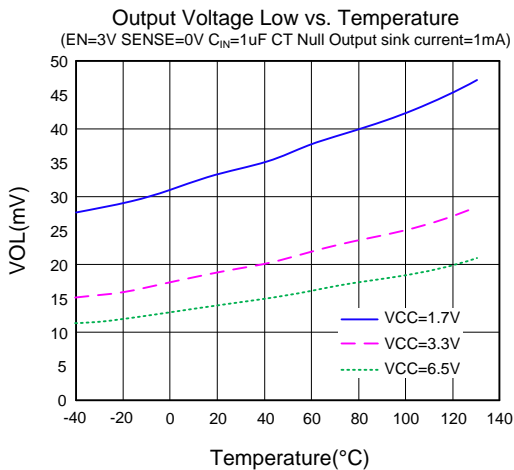
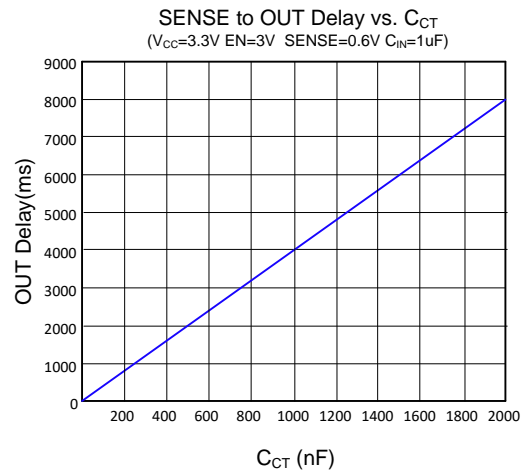
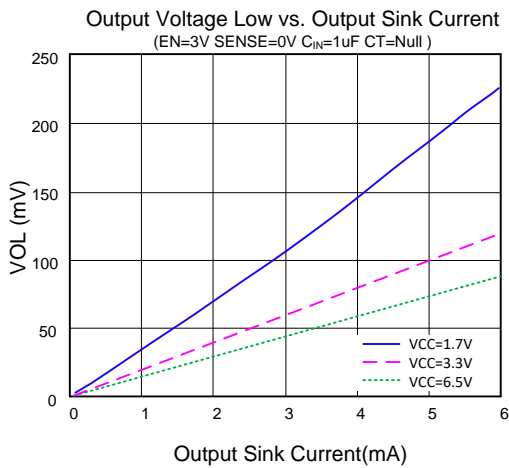
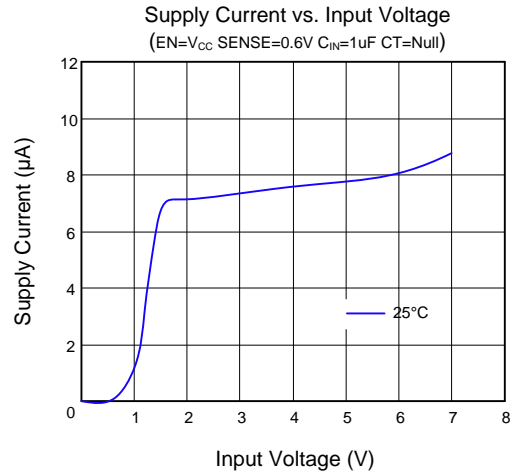
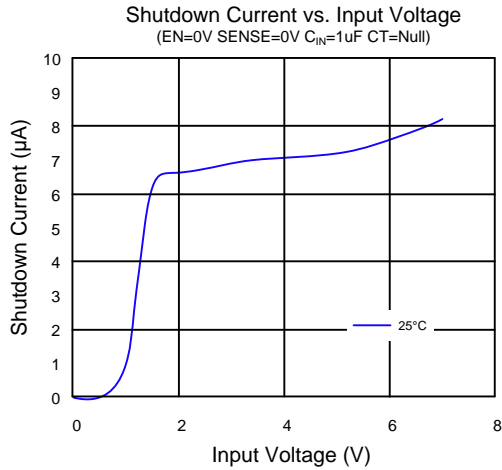
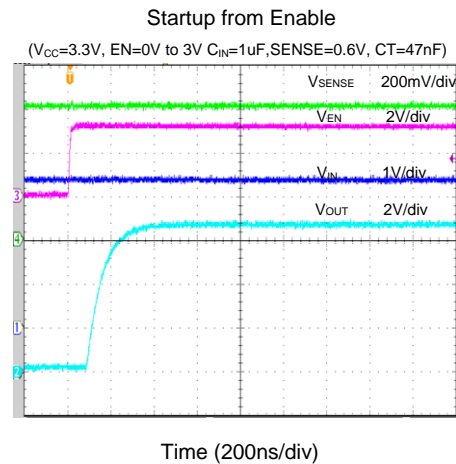
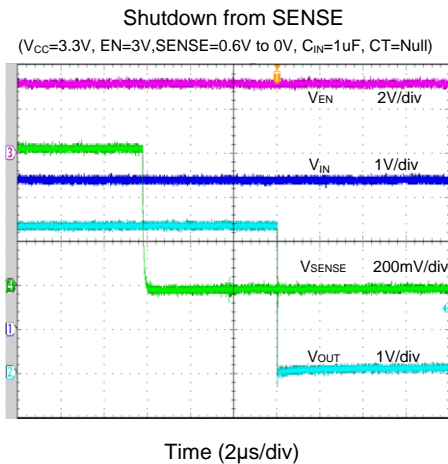
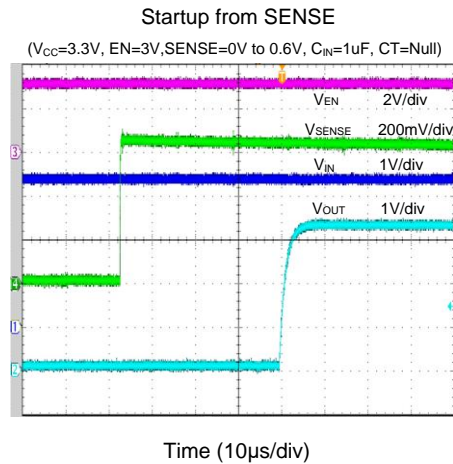
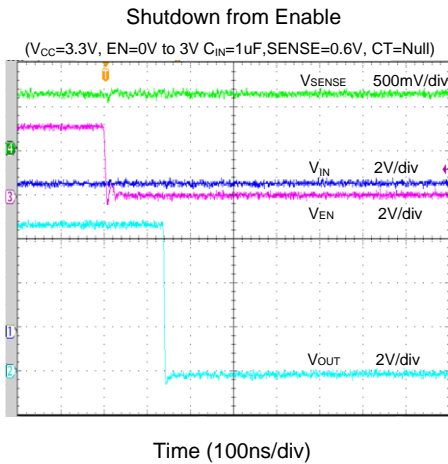
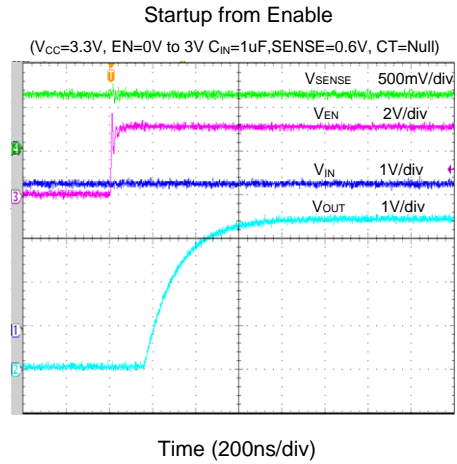
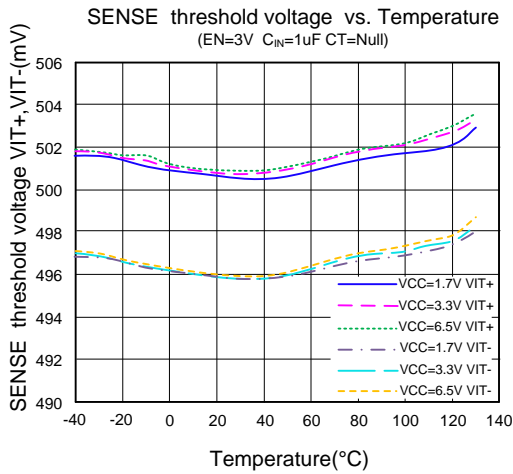


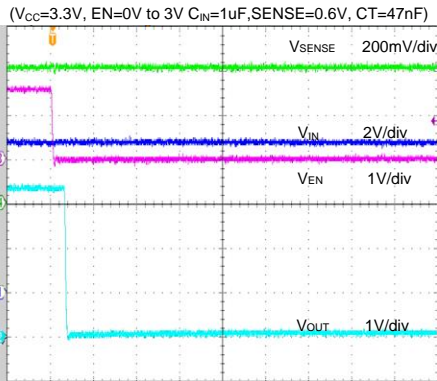
Figure3. SY20867F Timing Sequence

Typical Operating Characteristics



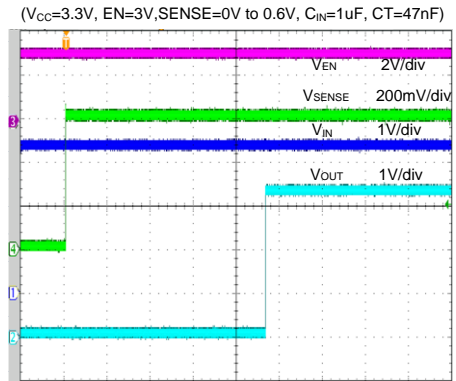


Shutdown from Enable



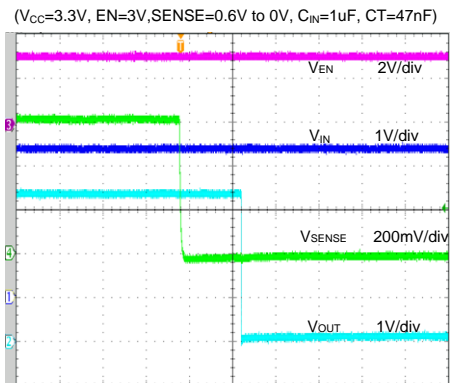
Time (400ns/div)

Startup from SENSE



Time (40ms/div)

Shutdown from SENSE



Time (4 μ s/div)

Application Information

The SY20867F is a compact supervisory circuit that monitors voltages greater than 500mV with 0.25% threshold accuracy. The output assertion delay time can be adjusted using an external capacitor. The device features a logic high enable pin to control the power on and off the internal logic.

Operating within a voltage range of 1.7V to 6.5V, the SY20867F has a typical quiescent current of 9μA and an open-drain output rated at 18V.

The device is available in an ultra-small DFN 1.45mm×1.0mm–6pin package and is fully specified for operation over a temperature range of T_J=-40°C to 125°C.

Table1. SY20867F Truth Table

Conditions		Output	Status
ENABLE = high	SENSE < VIT+	OUT = low	Output not asserted
ENABLE = low	SENSE < VIT+	OUT = low	Output not asserted
ENABLE = low	SENSE > VIT+	OUT = low	Output not asserted
ENABLE = high	SENSE > VIT+	OUT = high	Output asserted after delay

SENSE Input Pin

The SENSE input pin is designed to monitor system voltages greater than 0.5V. When the voltage on this pin reaches the threshold voltage (VIT+), and the ENABLE input is high, the output will be asserted after a delay set by a capacitor-adjustable timer. The output is de-asserted when the voltage at the SENSE pin falls below (VIT+ - Vhys). The comparator features built-in hysteresis to ensure smooth transitions between output assertions and de-assertions. While not typically necessary, a 1nF to 10nF bypass capacitor at the SENSE input is recommended for high noise environments, in order to mitigate sensitivity to transients and layout parasitics. The desired threshold voltage can be calculated using the following equation:

$$V_{TARGET} = (1 + R_1/R_2) \times 0.5(V) \quad (1)$$

CT Output Delay Time

The delay time can be programmed by adding an external capacitor between the CT pin and the ground. If the CT pin is floating, the device will use the internally set delay of 40μs. If required, the delay time can be extended to a value determined by the following equation:

$$t_{pd}(r) (s) = [C_{CT}(\mu F) \times 4] + 40 \mu s \quad (2)$$

The reset delay time is determined by the duration required for the on-chip, precision 310nA current source to charge an external capacitor to 1.24V. The internal current source is enabled when the voltage on the SENSE pin exceeds VIT+ and ENABLE is set high, initiating the charging of the external capacitor. Once the voltage across a capacitor reaches 1.24V, the OUT signal will be asserted. The use of a good dielectric ceramic capacitor is recommended for most applications. Note that stray capacitance around this pin could introduce errors when compared with the calculated reset delay time.

Output Pin (OUT)

In a typical application, the output is connected to a reset/enable input of the processor (DSP, CPU, FPGA, ASIC, etc.) or to the enable input of a voltage regulator.

The SY20867F features an open-drain output. A pull-up resistor must be used to ensure proper interfacing between the OUT pin and the circuit it controls. By connecting the pull-up resistor to an adequate voltage rail, OUT can be connected to other devices using different interface voltage levels. The outputs can be pulled up to 18V independent of the supply voltage (VCC). To ensure proper voltage levels, some thought should be given to choosing the correct pull-up resistor value. The ability to sink current is determined by the supply voltage; as an example, if VCC = 5V and the desired output pull-up rails is 18 V, then to obtain a sink current of 1 mA or less (as mentioned in the Electrical Characteristics section), the pull-up resistor value should be greater than 18 kΩ. Multiple devices can be used to monitor different voltage levels in a system and their outputs can be OR-wired, to create a single logic control signal.

Enable Function

An external logic signal from processors can control the enable input of the SY20867F, turning the output on or off. The SY20867F features an active-high enable input (ENABLE). When ENABLE is driven high, the OUT pin will be in high-impedance state. The threshold levels for ENABLE are 0.4V (maximum) when low, and 1.4V (minimum) when high, allowing it to be driven by a system supply of 1.5V or higher.

Active high input. Driving ENABLE low immediately makes OUT go low-impedance. With VSENSE greater than VIT+, driving ENABLE high causes OUT to go high-impedance after 0.2μs.

PCB Layout Guide

For best performance of the SY20867F, the following guidelines must be strictly followed:

1. Place the VCC decoupling capacitor close to the device.

2. Input and output capacitors should be placed closed to the IC and connected to ground plane to reduce noise coupling.

3. SENSE pin is a sensitive pin. Keep SENSE trace far away from the trace or plane that has large dv/dt. The divider resistor should be placed as close as possible to the SENSE pin.

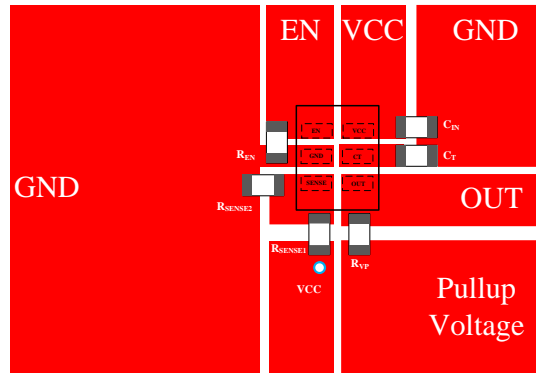
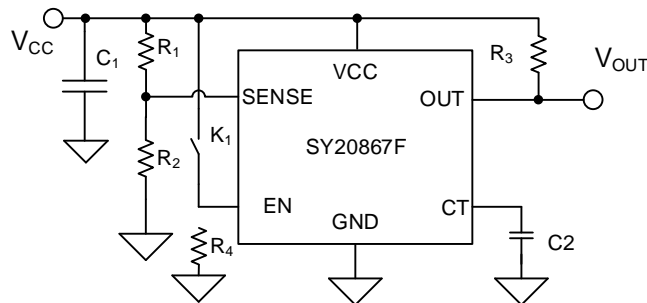


Figure4. PCB Layout Suggestion

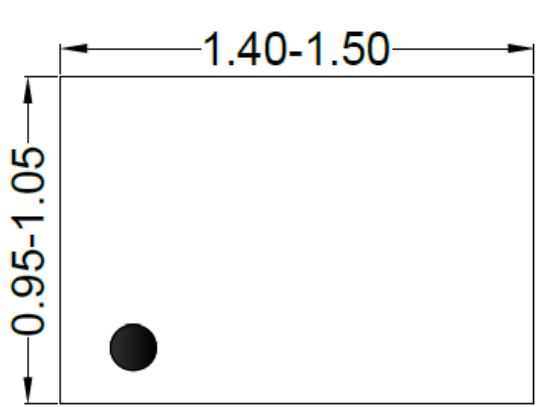
Schematic



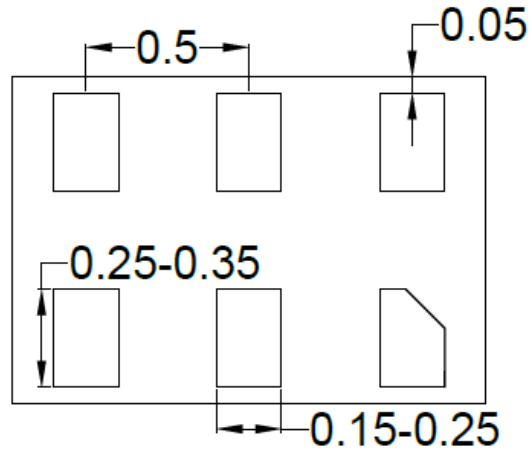
BOM List

Designator	Description	Part Number	Manufacturer
C1	1 μ F/50V, 0603, X5R	GRM188R61H105K	Murata
C2	47nF/25V,0603,X5R	GRM188R71H473K	Murata
R1	500k Ω , 0603		
R2	100k Ω , 0603		
R3	10K Ω , 0603		
R4	1M Ω , 0603		

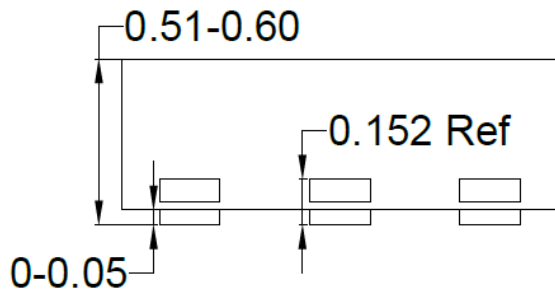
DFN1.45x1-6 Package Outline Drawing



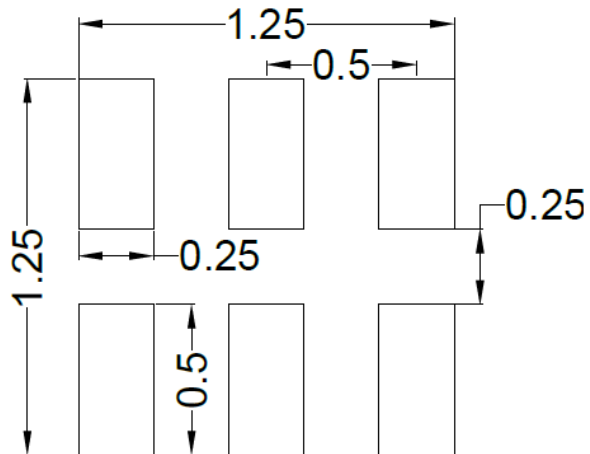
Top View



Bottom View



Side View

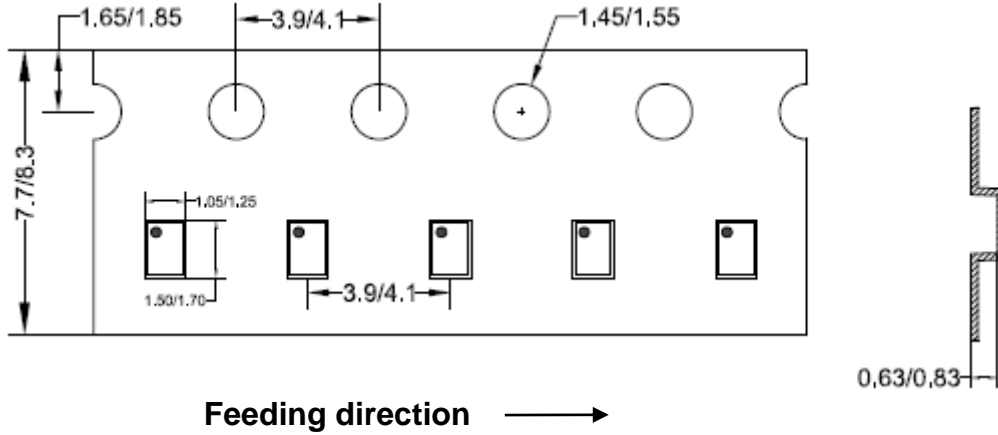


**Recommended PCB Layout
(only for reference)**

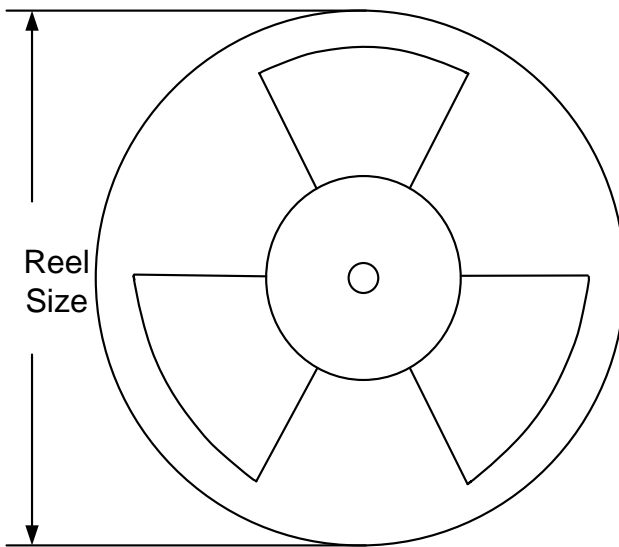
Notes: All dimension in millimeter and exclude mold flash & metal burr.

Taping & Reel Specification

1. Taping orientation



2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN1.45x1	8	4	7"	400	160	3000

3. Others: NA



Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Jan.10, 2024	Revision 1.0	Language improvements for clarity.
Nov.01, 2021	Revision 0.9A	Add "Positive-going Input Threshold Voltage" in EC table (page 4)
June 19, 2020	Revision 0.9	Initial Release



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