SY20019

High-Efficiency, 1A, 5.5V Input Synchronous Step-Down Regulator

General Description

The SY20019 high-efficiency 1.5MHz synchronous step-down DC/DC regulator operates over a wide input voltage range of 2.5V to 5.5V, and can deliver an output current up to 1A. It integrates a main switch and a synchronous switch with very low $R_{DS(ON)}$ to minimize conduction loss. The 1.5MHz pseudoconstant switching frequency allows for small external inductor and capacitor values.

The SY20019 uses constant-off-time and peak-current-mode control to achieve fast transient responses. It provides overcurrent and short-circuit protection.

The SY20019 is available in a space-saving, low-profile SOT563 package.

Features

- 2.5V to 5.5V Input Voltage Range
- Up to 1A Output Current
- 55μA Low Quiescent Current
- Low $R_{DS(ON)}$ for Internal Switches: 170mΩ Top, 100mΩ Bottom
- 1.5MHz Switching Frequency Minimizes Required External Components
- Internal Soft-Start Limits Inrush Current
- 100% Dropout Operation
- Power-Good Indicator
- Hiccup Mode for Short-Circuit Protection
- Output Auto-Discharge Function
- RoHS-Compliant and Halogen-Free
- Compact Package: SOT563

Applications

- Set-Top Boxes
- USB Dongles
- Media Players
- Smartphones

Typical Application

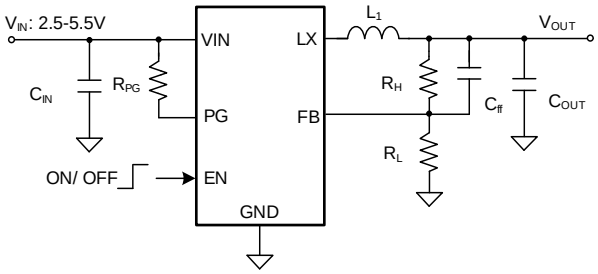


Figure 1. Schematic Diagram

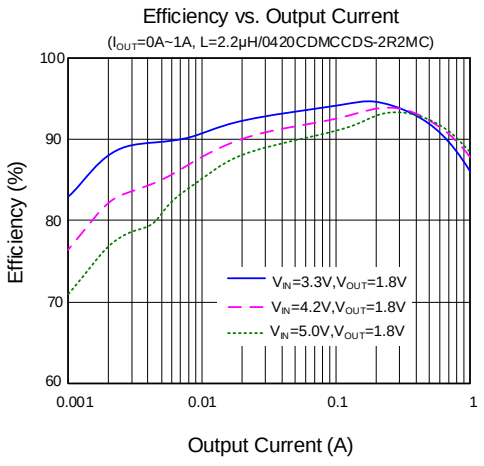


Figure 2. Efficiency vs. Output Current

Ordering Information

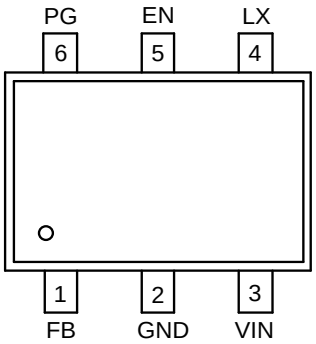
Ordering Part Number	Details
SY20019ARC	PFM Operation Pin 6 Power-Good (PG)
SY20019BARC	PFM Operation Pin 6 NC (No PG)
SY20019EARC	Forced PWM Operation Pin 6 Power-Good (PG)
SY20019FARC	Forced PWM Operation Pin 6 NC (No PG)

Package Information

Part Number	Top Mark	Package type
SY20019ARC	**L9*xyz***	SOT563 RoHS-Compliant and Halogen-Free
SY20019BARC	**M2*xyz***	
SY20019EARC	**E2*xyz***	
SY20019FARC	**M3*xyz***	

x = year code, y = week code, z = lot number code

Pinout (top view)*



*Pin 6 is NC for SY20019BARC and SY20019FARC

Pin Description

Pin No	Pin Name	Pin Description
1	FB	Output feedback pin. Connect this pin to the center point of the output resistor-divider (as shown in Figure 1) to program the output voltage: $V_{OUT} = 0.6 \times (1+R_H/R_L)$.
2	GND	Ground pin.
3	V_{IN}	Input pin. Decouple this pin to the GND pin with at least a 10µF ceramic capacitor.
4	LX	Inductor pin. Connect this pin to the switching node of the inductor.
5	EN	Enable pin. Pull low to disable the device, pull high to enable. Do not leave this pin floating.
6	PG	SY20019ARC/SY20019EARC: Power-good indicator pin. This pin is high-impedance if the output is between 90% and 120% of the regulation voltage; otherwise, it is driven low. Connect a pullup resistor to the input.
	NC	SY20019BARC/SY20019FARC: NC, leave it floating or connected to GND.

Block Diagram

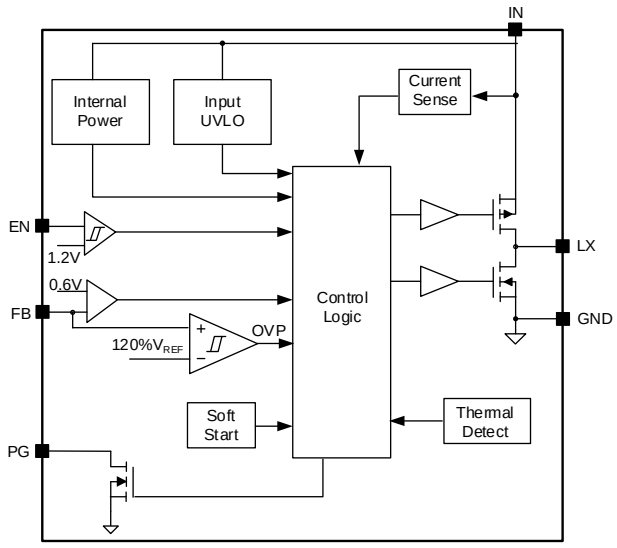


Figure 3. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
IN	-0.3	6	V
EN, FB, PG	-0.3	IN+ 0.6	
LX	-0.3	6	
LX, 20ns duration	-3	7	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering,10sec.)		260	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	105	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	30	
P_D Power Dissipation T_A = 25°C	0.95	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
IN	2.5	5.5	V
Output Voltage	0.6	5.5	
Output Current		1	A
Junction Temperature	-40	125	°C

Electrical Characteristics

(V_{IN} = 5V, V_{OUT} = 1.8V, L = 2.2μH, C_{OUT} = 10μF, T_J = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input	Voltage	V_{IN}		2.5		5.5	V
	UVLO, Rising	$V_{IN,UVLO}$			2.45	2.5	V
	UVLO, Hysteresis	$V_{IN,HYS}$			150		mV
	Quiescent Current	I_Q	V_{FB} = 105% × VREF (For SY20019ARC and SY20019BARC Only)		55		μA
	Shutdown Current	I_{SHDN}	V_{EN} = 0V		0.1	1	μA
FB	Reference Voltage	V_{REF}	I_{OUT} = 0.5A, CCM	0.591	0.6	0.609	V
	Input Current	I_{FB}	V_{EN} = 2V, V_{FB} = 1V	-50	0	50	nA
Power Switch	On-Resistance	$R_{DS(ON)HS}$			170		mΩ
	Current Limit	$I_{LMT,HS}$		1.5		2.5	A
Synchronous Rectifier	On-Resistance	$R_{DS(ON)LS}$			100		mΩ
Discharge FET Resistance		R_{DIS}			50		Ω
Enable(EN)	Input Voltage High	$V_{EN,H}$		1.2			V
	Input Voltage Low	$V_{EN,L}$				0.4	V
	Input Current	I_{EN}	V_{EN} = 2V			2	μA
Soft-Start (SS)	Turn-On Delay Time	$t_{ON,DLY}$	From EN high to LX start switching		0.25		ms
	Soft-Start Time	t_{SS}	V_{OUT} from 0% to 100%		0.75		ms
Undervoltage Protection	Threshold	V_{UVP}			50		%V_{REF}
	Delay	$t_{UVP,DLY}$			10		μs
UVP/OCP Hiccup On-Time		$t_{HICCUP,ON}$			1.45		ms
UVP/OCP Hiccup Off-Time		$t_{HICCUP,OFF}$			1.45		ms
Power-Good	Thresholds	V_{PG}	V_{FB} falling, fault		88		%
			V_{FB} rising, good		90		%
			V_{FB} rising, fault		120		%
			V_{FB} falling, good		114		%
	Delay	$t_{PG,R}$	V_{FB} rising, good		2		μs
		$t_{PG,F}$	V_{FB} falling, fault		15		μs
Switching Frequency		f_{SW}	I_{OUT} = 0.5A, CCM		1.5		MHz
Min On-Time		$t_{ON,MIN}$			50		ns
Maximum Duty Cycle		D_{MAX}		100			%
Thermal Shutdown Temperature		T_{SD}			160		°C
Thermal Shutdown Hysteresis		T_{HYS}			20		°C

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} of SY20019 is measured in the natural convection at T_A = 25°C on a 2oz two-layer Silergy evaluation board. Pin 4 is the case position for SY20019 θ_{JC} measurement.

Note 3: The device is not guaranteed to function outside its operating conditions.

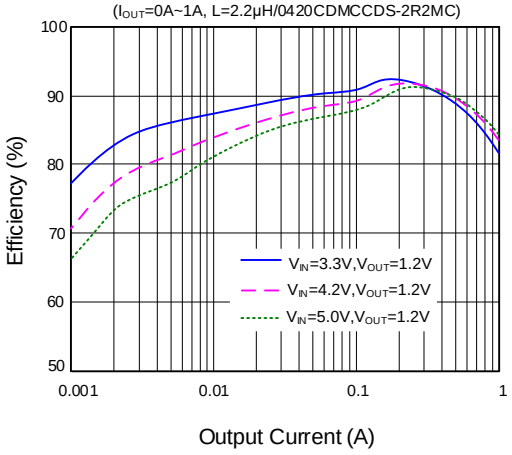
Typical Performance Characteristics

(T_A = 25°C, V_{IN} = 5V, V_{OUT} = 1.8V, L = 2.2μH, C_{OUT} = 10μF, unless otherwise noted)

SY20019ARC

Efficiency vs. Output Current

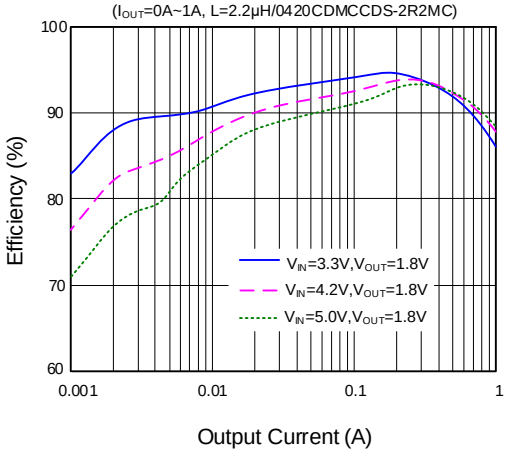
(I_{OUT}=0A~1A, L=2.2μH/0420CDMCCDS-2R2MC)



Output Current (A)

Efficiency vs. Output Current

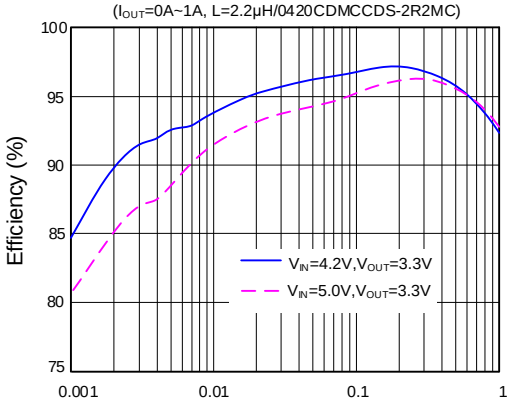
(I_{OUT}=0A~1A, L=2.2μH/0420CDMCCDS-2R2MC)



Output Current (A)

Efficiency vs. Output Current

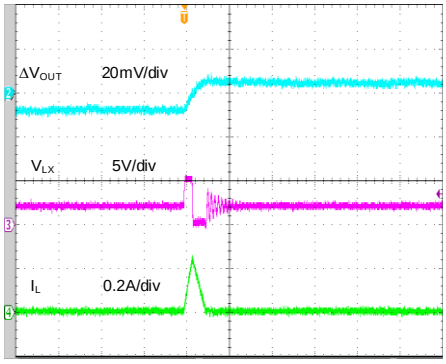
(I_{OUT}=0A~1A, L=2.2μH/0420CDMCCDS-2R2MC)



Output Current (A)

Output Ripple

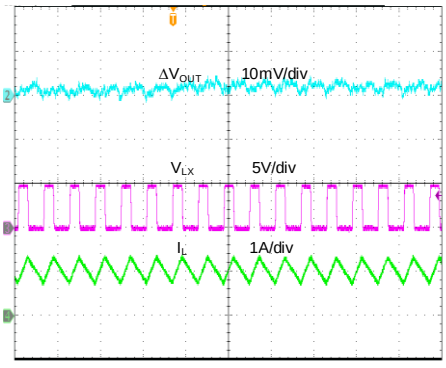
(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=0A)



Time (1μs/div)

Output Ripple

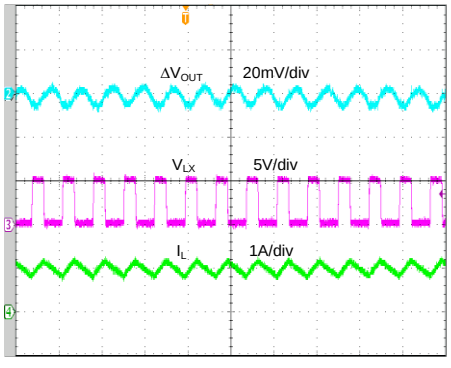
(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=0.5A)



Time (1μs/div)

Output Ripple

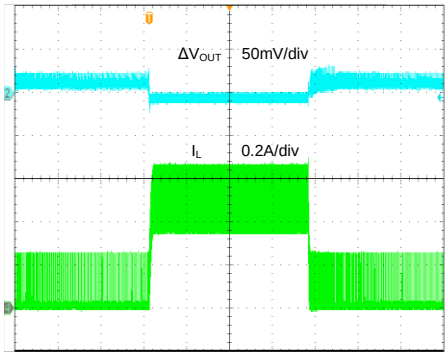
(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=1.0A)



Time (1μs/div)

Load Transient

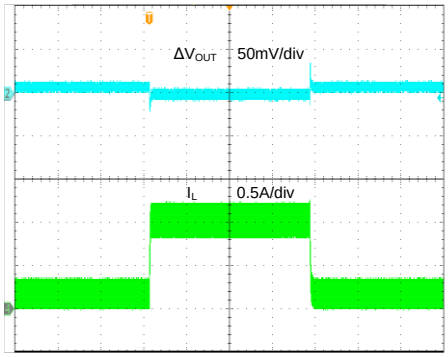
(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=0A ~ 0.5A)



Time (800μs/div)

Load Transient

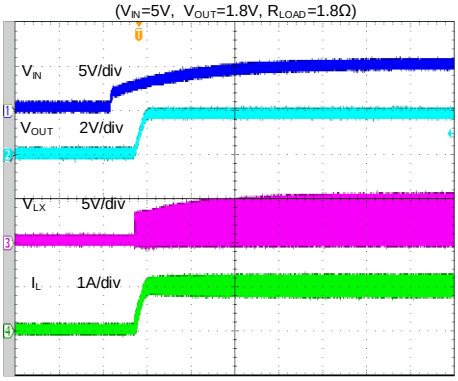
(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=0.1A ~ 1A)



Time (800μs/div)

Startup from V_{IN}

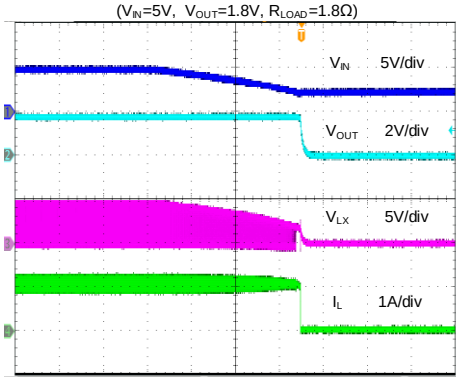
(V_{IN}=5V, V_{OUT}=1.8V, R_{LOAD}=1.8Ω)



Time (2ms/div)

Shutdown from V_{IN}

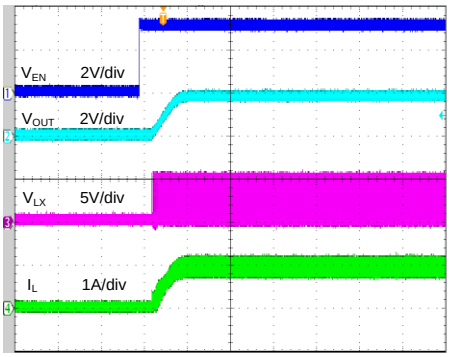
(V_{IN}=5V, V_{OUT}=1.8V, R_{LOAD}=1.8Ω)



Time (2ms/div)

Startup from Enable

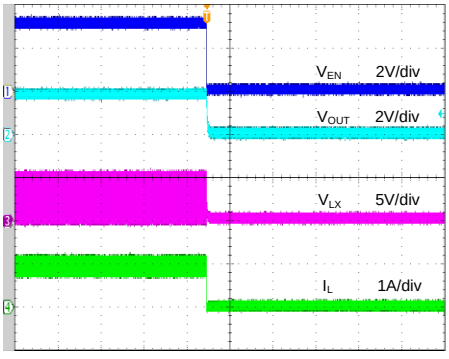
(V_{IN}=5.0V, V_{OUT}=1.8V, R_{LOAD}=1.8Ω)



Time (800μs/div)

Shutdown from Enable

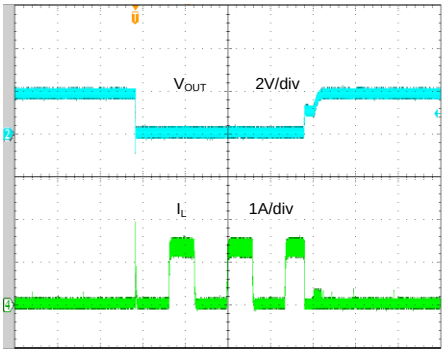
(V_{IN}=5.0V, V_{OUT}=1.8V,R_{LOAD}=1.8Ω)



Time (800μs/div)

Short Circuit Protection

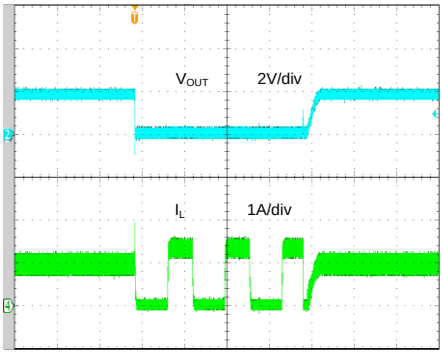
(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=0A ~ Short)



Time (2ms/div)

Short Circuit Protection

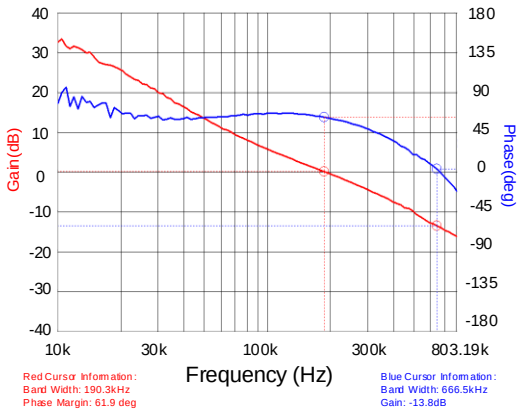
(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=1A ~ Short)



Time (2ms/div)

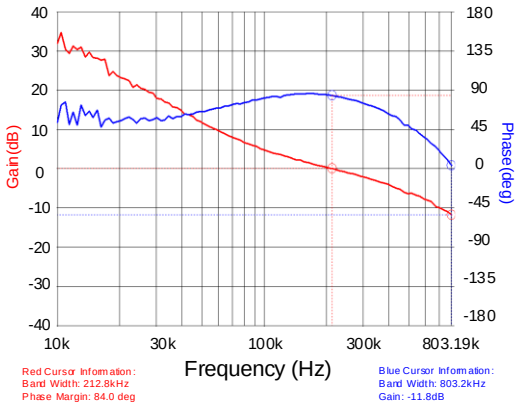
Bode Plot

(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=1A)



Bode Plot

(V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=1A)



Operation

The SY20019 high-efficiency 1.5MHz synchronous step-down DC/DC regulator operates over an input voltage range of 2.5V to 5.5V, and can deliver an output current up to 1A. It integrates a main switch and a synchronous switch with very low $R_{DS(ON)}$ to minimize conduction loss. The 1.5MHz pseudoconstant switching frequency allows for small external inductor and capacitor values.

The SY20019 uses constant-off-time and peak-current-mode control to achieve fast transient responses. When the top FET's current-sense signal reaches internal V_{COMP}, the top FET will turn off and the bottom FET will turn on for a fixed period of time (constant t_{OFF}). t_{OFF} is internally calculated according to the input voltage, output voltage, and desired switching frequency (f_{SW}):

$$t_{OFF} = \frac{1 - V_{OUT}/V_{IN}}{f_{SW}}$$

The bottom FET turns off after a period of t_{OFF}.

The SY20019 is available in a space-saving, low-profile SOT563 package.

Applications Information

The selection process for the input capacitor C_{IN}, output capacitor C_{OUT}, output inductor L, and feedback resistors (R_H and R_L) is described in the following sections.

Feedback Resistor-Divider R_H and R_L

Choose R_H and R_L to program the proper output voltage. A value between 1kΩ and 1MΩ is recommended for both resistors. If R_L = 120kΩ is chosen, then R_H can be calculated as follows:

$$R_H = \frac{(V_{OUT} - 0.6V) \times R_L}{0.6V}$$

Input Capacitor C_{IN}

For the best performance, select a typical X5R or better grade ceramic capacitor with a 6.3V rating, and at least 10µF capacitance. The capacitor should be placed as close as possible to the device, while also minimizing the loop area formed by C_{IN} and the IN/GND pins.

When selecting an input capacitor, ensure that its voltage rating is at least 20% greater than the maximum voltage of the input supply. X5R or X7R dielectric types are the most often selected due to their small size, low cost, surge current capability, and high RMS current rating over a wide temperature and voltage range.

In situations where the input rail is supplied through long wires, it is recommended to add some bulk capacitance like electrolytic-, tantalum-, or polymer-type capacitors to reduce the overshoot and ringing caused by the added parasitic inductance.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

The worst-case condition occurs at D = 0.5, then

$$I_{CIN\_RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplicity, use an input capacitor with an RMS current rating greater than 50% of the maximum load current.

The input capacitor value determines the input voltage ripple of the converter. If there is a voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification.

Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated using the formula:

$$V_{CIN\_RIPPLE,CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1 - D)$$

The worst-case condition occurs at D = 0.5, then

$$V_{CIN\_RIPPLE,CAP,MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. A single 10µF X5R capacitor is sufficient in most applications.

Output Capacitor C_{OUT}

Select the output capacitor C_{OUT} to handle the output ripple requirements. Both steady-state ripple and transient requirements must be taken into consideration when selecting C_{OUT}. For the best performance, use an X5R or better grade ceramic capacitor with a 6.3V rating, and capacitance of at least 10µF.

For applications where the design must meet stringent ripple requirements, the following considerations must be followed.

The output voltage ripple at the switching frequency is caused by the inductor-current ripple (ΔI_L) on the output capacitor's ESR (ESR ripple), as well as the stored charge (capacitive ripple). When calculating total ripple, consider both.

$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

The capacitive ripple might be higher because the effective capacitance for ceramic capacitors decreases with the voltage across the terminals. The voltage derating is usually included as a chart in the capacitor datasheet, and the ripple can be recalculated after taking the target output voltage into account.

Output Inductor L

Consider the following when choosing this inductor:

1) Choose the inductance to provide a ripple current that is approximately 40% of the maximum output current. The recommended inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT} / V_{IN,MAX})}{f_{sw} \times I_{OUT,MAX} \times 0.4}$$

where f_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY20019 has high tolerance for ripple current amplitude variation. As a result, the final choice of inductance can vary slightly from the calculated value with no significant performance impact.

2) The inductor's saturation current rating must be greater than the peak inductor current under full load:

$$I_{SAT,MIN} > \mathrm{I_{OUT,MAX}} + \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{2 \times f_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. Use an inductor with DCR less than 50mΩ to achieve good overall efficiency.

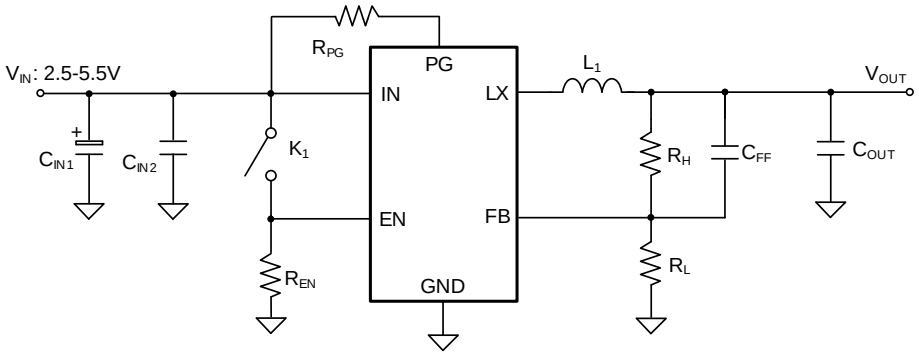
Overcurrent and Short-Circuit Protection

With load current increasing, as soon as the high-side FET current exceeds the peak current-limit threshold, the high-side FET will turn off. If the load current continues to increase, the output voltage will drop. When the output voltage falls below 50% of the regulation level, the output undervoltage protection will be activated and the SY20019 will operate in hiccup mode. The hiccup frequency is 350Hz and the hiccup duty cycle is 50%. If the hard short is removed, the SY20019 will return to normal operation.

Load-Transient Considerations

The SY20019 regulator integrates the compensation components to achieve good stability and fast transient responses. In some applications, adding a 22pF ceramic capacitor in parallel with R_H may further speed up the load-transient responses, and is therefore recommended for applications with large load-transient step requirements.

Application Schematic (V_{OUT} = 1.8V)



BOM List

Reference Designator	Description	Part Number	Manufacturer
L_1	2.2μH	0420CDMCCDS-2R2MC	Sumida
C_{IN1}	100μF/25V(electrolytic capacitor)		
C_{IN2}	10μF/6.3V, 0603, X5R	C1608X5R0J106M	TDK
C_{FF}	22pF/50V, 0603, X5R	C1608C0G1H220J	TDK
C_{OUT}	10μF/6.3V, 0603, X5R	C1608X5R0J106M	TDK
R_{EN}	1MΩ, 0603		
R_{PG}	100kΩ, 0603		
R_H	100kΩ, 0603, 1%		
R_L	49.9kΩ, 0603, 1%		

Recommended Component Values for Typical Applications

V_{OUT}(V)	R_H(kΩ)	R_L(kΩ)	C_{FF}(pF)	L/(Rated/Saturating Current)	C_{OUT}
1.2	49.9	49.9	22	2.2μH/(4.3A/6.3A)	10μF/6.3V, 0603, X5R
1.8	100	49.9	22	2.2μH/(4.3A/6.3A)	10μF/6.3V, 0603, X5R
3.3	100	22.1	22	2.2μH/(4.3A/6.3A)	10μF/6.3V, 0603, X5R

Layout Design

For optimal design, follow these PCB layout considerations:

- For minimum noise and maximum efficiency, place the following components close to the IC: C_{IN}, L1, $R_{H,}$ and R_L.
- To achieve the best thermal and noise performance, maximize the PCB copper area connecting to the GND pin. A ground plane is highly recommended if board space allows.
- C_{IN} must be close to pins IN and GND. Minimize the loop area formed by C_{IN}, V_{IN}, and GND.
- To reduce the switching noise, minimize the PCB copper area connected to the LX pin.
- R1, R2, and the trace connected to the FB pin must **not** be adjacent to the LX net on the PCB layout, in order to reduce crosstalk.

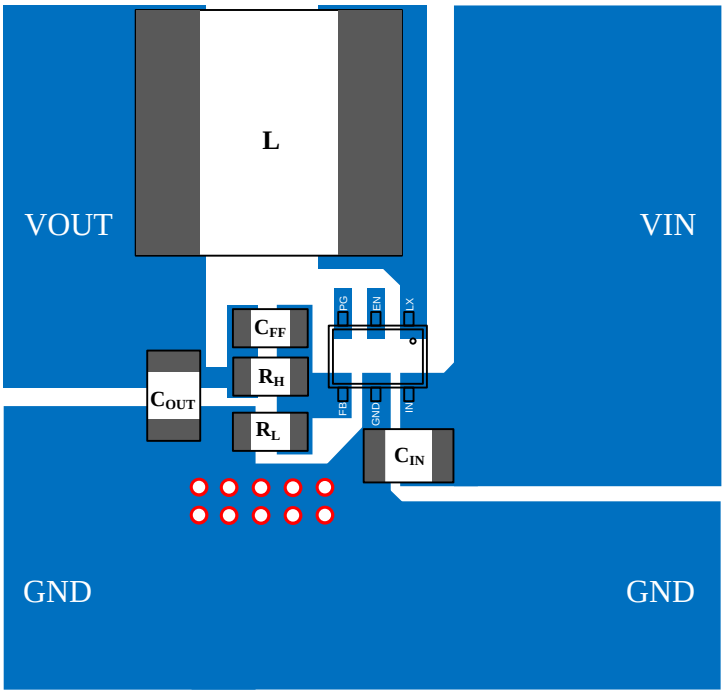
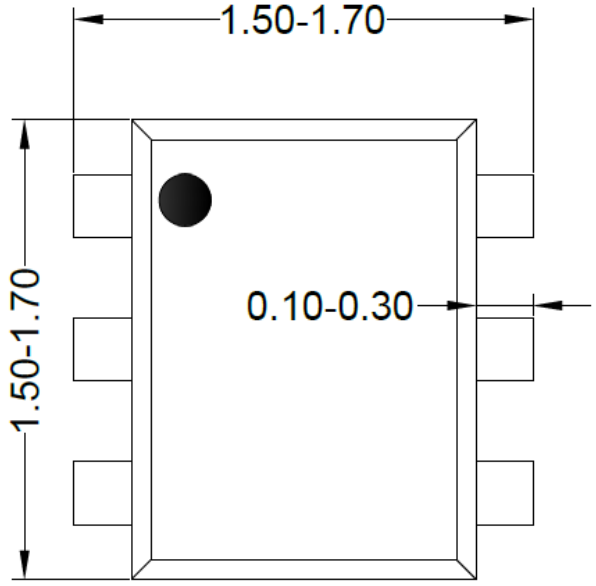
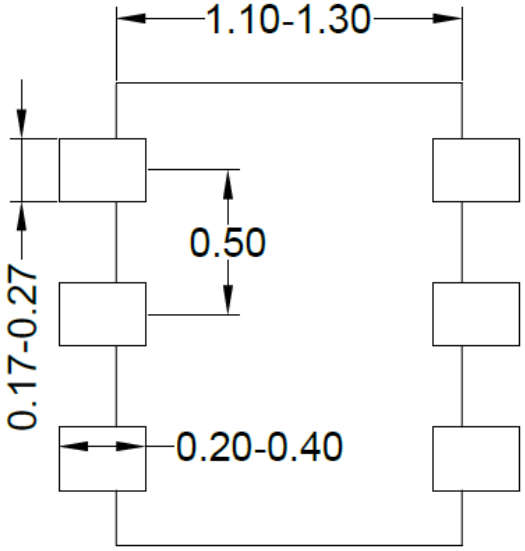


Figure 3. Suggested PCB Layout

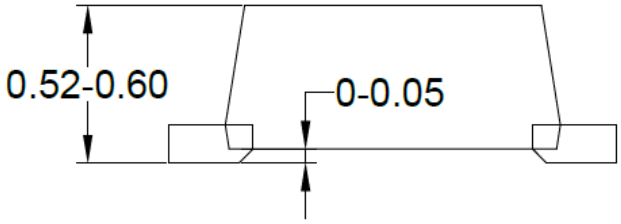
SOT563 Package Outline



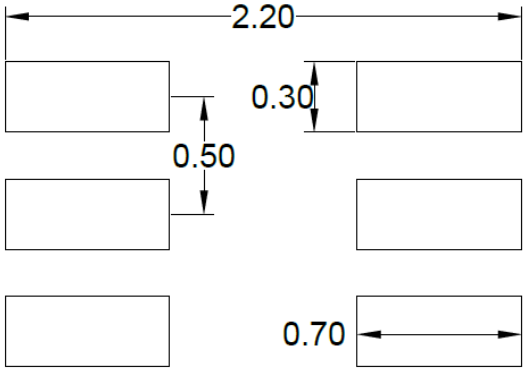
Top view



Bottom view



Side View

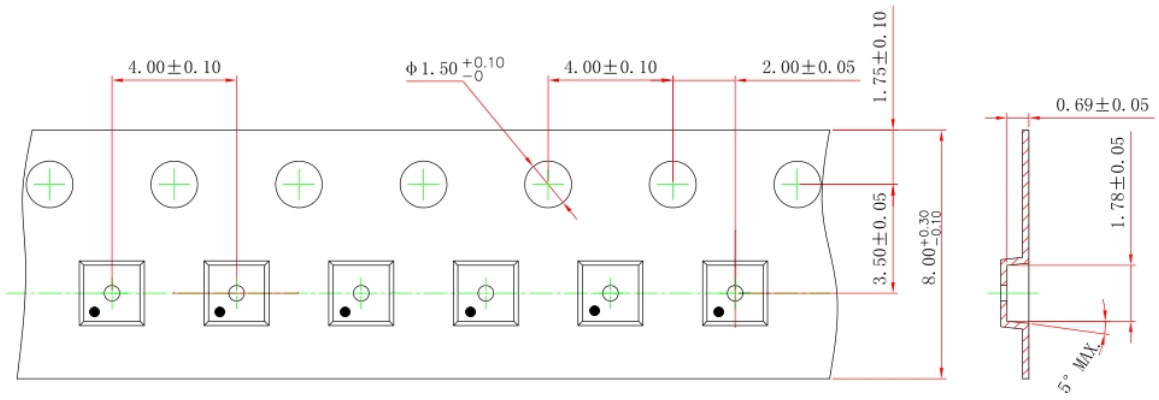


Recommended PCB layout
(Reference only)

Note: *All dimensions are in millimeters and exclude mold flash and metal burr.*

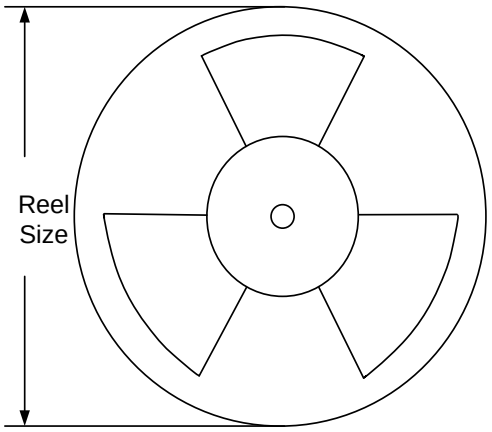
Taping & Reel Specification

SOT563 taping orientation



Feeding Direction ⟶

Carrier tape and reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SOT563	8	4	7"	280	160	5000

Others: NA

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