SY205215AOC

Low Capacitance ESD Protection

General Description

SY205215AOC is a low-capacitance transient voltage suppressor (TVS) designed to provide electrostatic discharge (ESD) protection for data, control, or power lines. With a typical capacitance of 0.6pF, SY205215AOC is designed to protect against over-voltage and over-current transient events. It complies with IEC 61000-4-2 (ESD) (±25kV air, ±25kV contact discharge), and IEC 61000-4-5 (surge) (4A, 8/20μs).

Each SY205215AOC device can protect two data lines and is available in a SOT-23 package.

Features

- Protects Two Data, Control, or Power Lines
- Low Capacitance: 0.6pF (Typical)
- Low Leakage Current: 0.01μA @ V_{RWM} (Typical)
- Low Clamping Voltage
- Transient Protection for High-Speed Data Lines
  - IEC 61000-4-2 (ESD) ±25kV (Air)±25kV (Contact)
  - IEC 61000-4-5 (Surge) 4A (8/20μs)
- Each I/O pin can withstand over 1000 ESD strikes for ±8kV contact discharge.

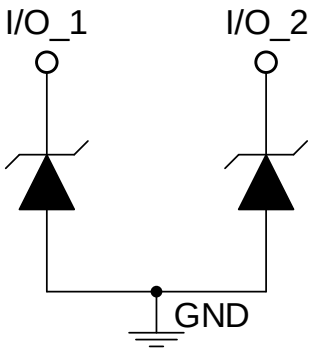
Applications

- Portable Electronics
- Desktops, Servers, and Notebooks
- Cellular Phones
- MP3 Ports
- Digital Camera Ports
- SIM Cards

Mechanical Characteristics

- SOT-23 Package
- Marking: Device Code, Date Code
- Packaging: Tape and Reel

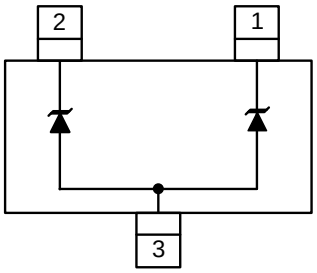
Circuit Diagram



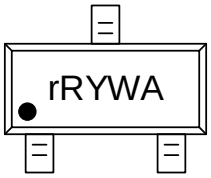
Ordering Information

Part Number	Package Type	Top Mark
SY205215AOC	SOT-23 RoHS Compliant and Halogen Free	rRYWA

Pinout (Top View)



Marking Codes



Note 1: "rR" is device code, fixed.

Note 2: "YWA" is date code.

Absolute Maximum Rating				
Parameter	**Symbol**	**Min**	**Max**	**Unit**
Maximum Peak Pulse Current (8/20μs)	I_{PP}		4	A
Maximum Peak Pulse Power (8/20μs)	P_{PK}		50	W
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	-25	25	kV
Operating Temperature	T_{OPT}	-40	+125	°C
Storage Temperature	T_{STG}	-55	+150	°C

Electrical Characteristics (T_A = 25°C)						
Parameter	**Symbol**	**Test Condition**	**Min**	**Typ**	**Max**	**Unit**
Nominal Reverse Working Voltage	V_{RWM}				5	V
Reverse Leakage Current @ V_{RWM}	I_R	V_R = 5V, T = 25°C Between I/O and GND		0.01	0.1	μA
Reverse Breakdown Voltage @ I_T	V_{BR}	I_T = 1mA Between I/O and GND	5.5		10	V
Forward Voltage @ I_F	V_F	I_F = 1mA Between I/O and GND	0.4	0.7	1.2	V
Clamping Voltage @ I_{PP}	V_C (1)	I_{PP} = 4A, t_p = 8/20μs Between I/O and GND			12	V
Clamping Voltage @ I_{PP}	V_C(1)	I_{PP} = 16A, t_p = 10/100ns Between I/O and GND		12.5		V
Dynamic Resistance	R_{DYN}(1) (2)	t_p = 10/100ns Between I/O and GND		0.2		Ω
Parasitic Capacitance	C_{ESD}(1)	V_R = 0V, f = 1MHz Between I/O and GND		0.60	0.80	pF
Parasitic Capacitance	C_{ESD}(1)	V_R = 0V, f = 1MHz Between I/O and I/O		0.30	0.40	pF

Note 1: Guaranteed by design and not subject to production test.

Note 2: R_{DYN} calculated based on I_{PP}=8A to I_{PP}=16A, t_p = 10/100ns.

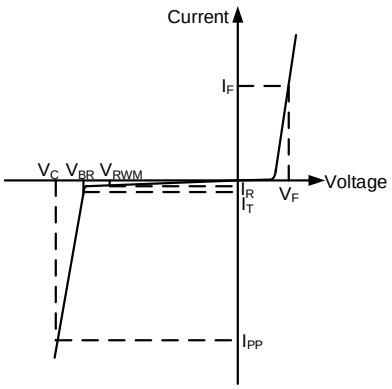
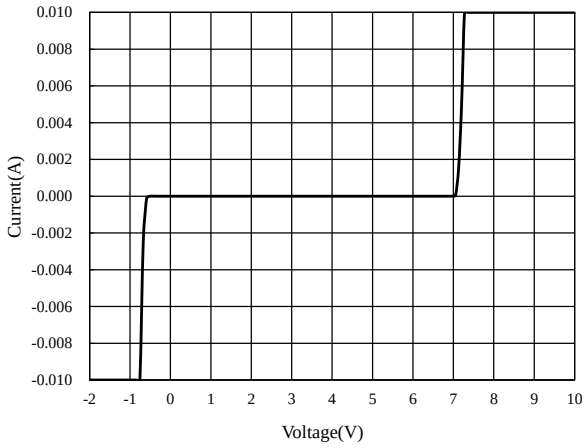


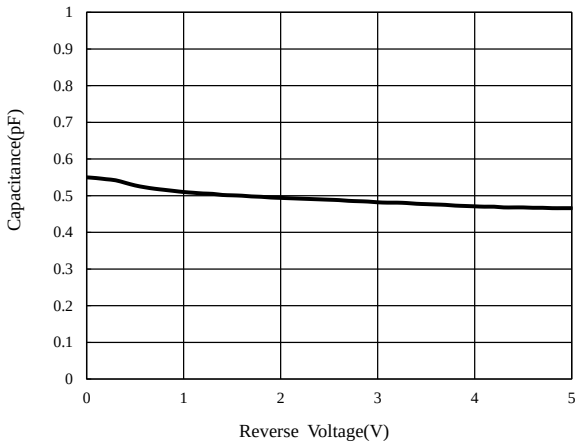
Figure 1. Uni-directional TVS

Typical Characteristics Voltage

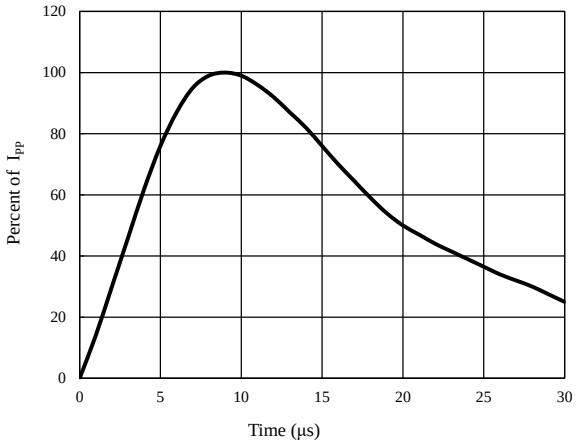
Sweeping of I/O to GND



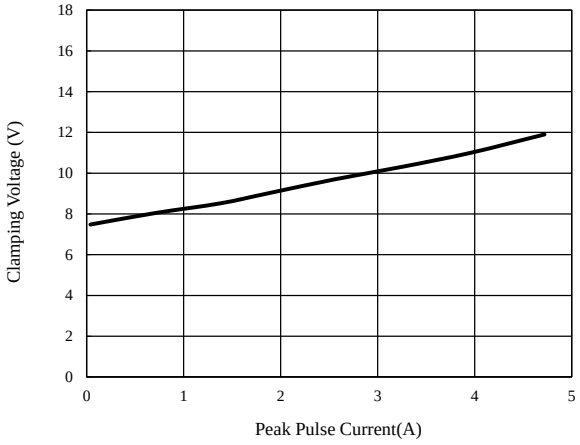
Capacitance vs. Voltage



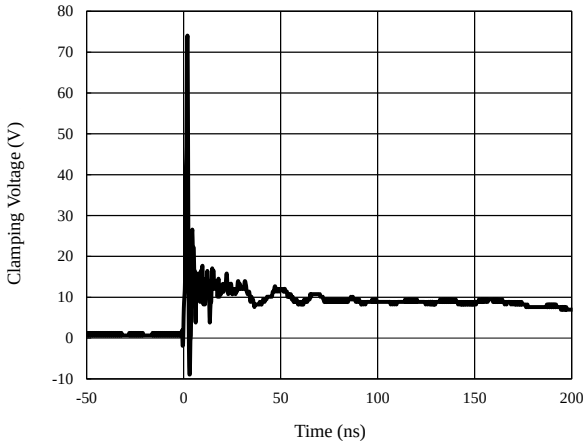
Pulse Waveform



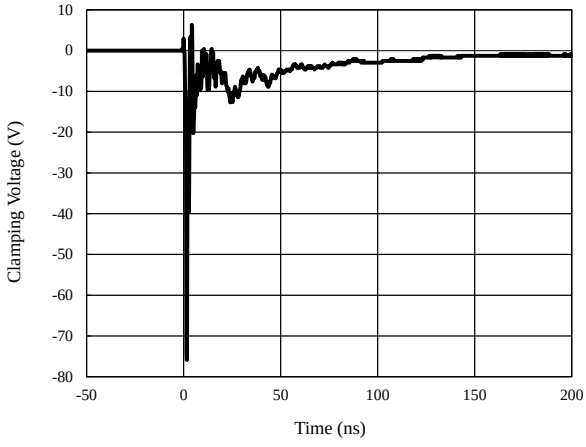
Clamping Voltage vs. Peak Pulse Current



ESD Clamping of I/O to GND (+8kV Contact per IEC 61000-4-2)



ESD Clamping of I/O to GND (-8kV Contact per IEC 61000-4-2)



Application Information

USB 2.0 Interface Application Example

Pin1 and Pin2 of SY205215AOC are connected to D+ and D- of one USB port, respectively.

SY205215AOC is designed to offer ESD protection solutions between data lines and the GND. Connecting the I/O to the data lines and attaching Pin3 to the ground can discharge any positive transient line-to-ground ESD event via the Zener diode. Negative line-to-ground transients can be directly discharged to the ground through the forward diode. Line-to-line discharges are managed through the back-to-back Zener diode.

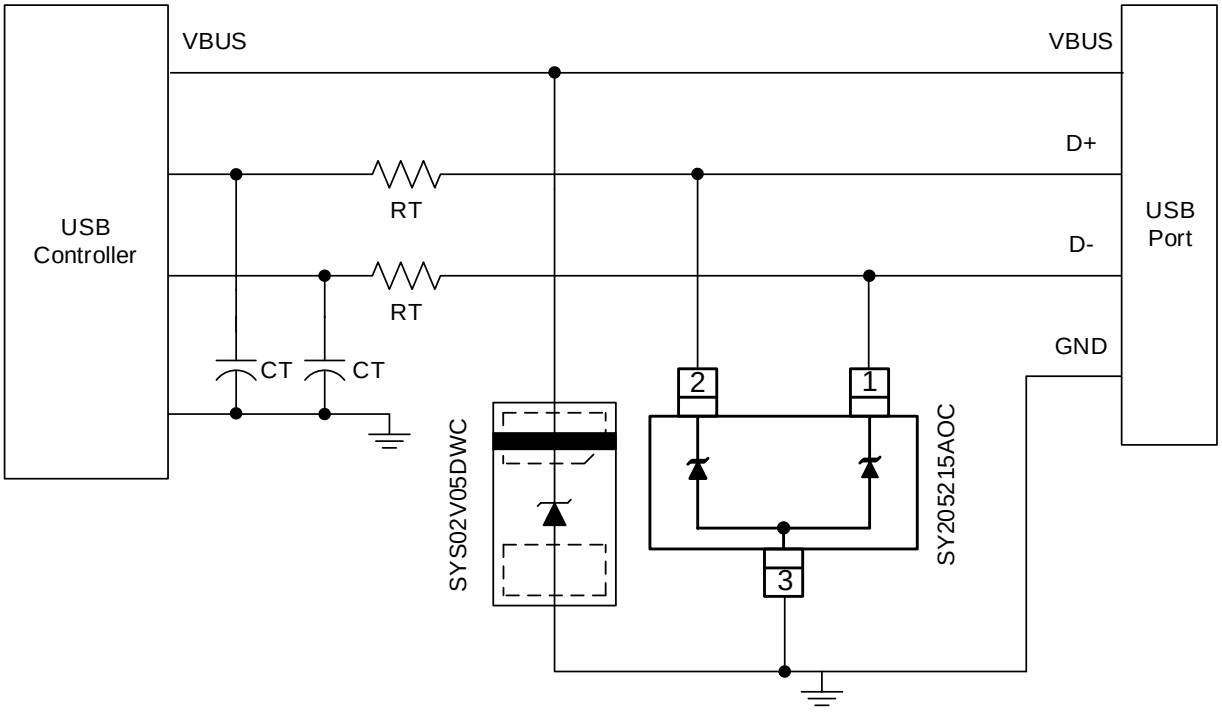


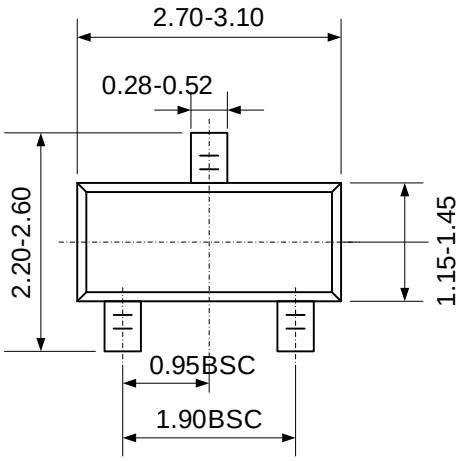
Figure 2. Typical ESD Protection for USB 2.0

PCB Layout Guidelines

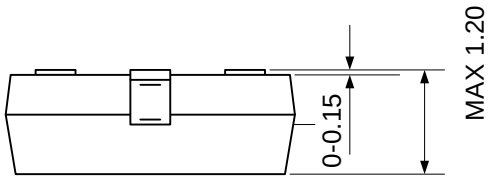
For optimum ESD protection and circuit performance, the following PCB layout guidelines are recommended:

- Place SY205215AOC as close to the connector port as possible.
- The distance between the SY205215AOC ground pin and the GND reference path should be as short as possible.
- Use a large via to connect the GND pins to the ground.
- Avoid running critical signals near board edges.

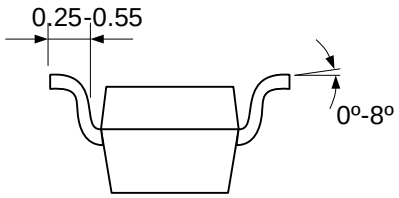
SOT-23 Package Outline



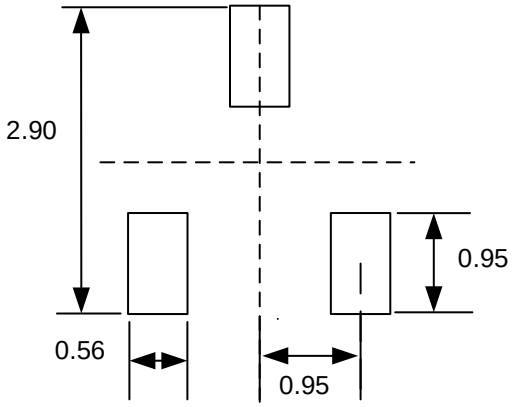
Top View



Side View



Side View

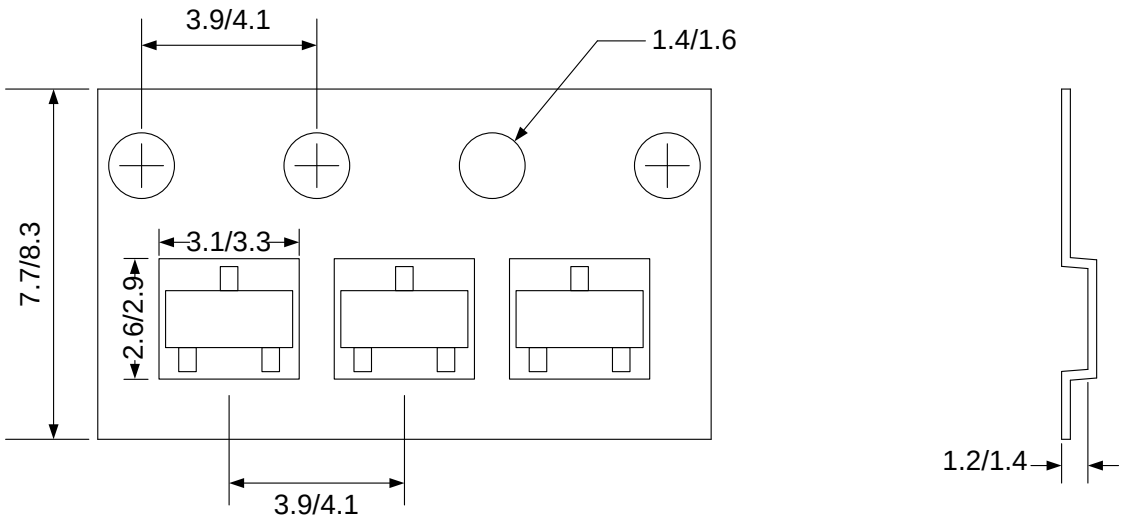


Recommended PCB Layout (Reference only)

Notes: *All dimensions are in millimeters and exclude mold flash and metal burr.*

Tape and Reel Specification

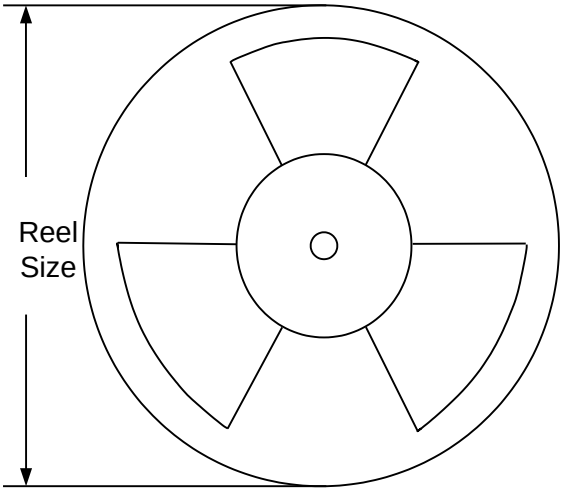
SOT-23 Taping Orientation



Dimensions In mm

Feeding direction ⟶

Carrier Tape & Reel Specification for Packages



Package Types	Tape Width (mm)	Pocket Pitch(mm)	Reel Size (Inch)	Qty per Reel(pcs)
SOT-23	8	4	7"	3000

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Revision Number	Revision Date	Description	Pages changed
0.9	03/14/2019	Initial Release	
1.0	03/14/2020	Production Release	

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