SY205207DXC

Ultra-Low Capacitance TVS Protection

General Description

SY205207DXC is an ultra-low capacitance transient voltage suppressor (TVS) designed to provide electrostatic discharge (ESD) protection for high-speed data interfaces against transient events. The device has a typical capacitance of 0.2pF. It complies with IEC61000-4-2 (ESD) (±20kV air, ±20kV contact discharge), IEC61000-4-5 (surge) (9A, 8/20μs).

Each SY205207DXC device can protect one high-speed data line. The combined features of ultra-low capacitance, ultra-small size and high ESD robustness make SY205207DXC ideal for high-speed data ports and high-frequency lines. The low clamping voltage of the SY205207DXC guarantees minimum stress on the protected IC.

The SY205207DXC is available in a compact DFN 0.6×0.3-2 package.

Features

- Transient protection for high-speed data lines
  - IEC61000-4-2 (ESD) ±20kV (air) ±20kV (contact)
  - IEC61000-4-5 (surge) 9A (8/20μs)
- For 24V and below operating voltage
- Package optimized for high-speed lines
- Ultra-small package (0.6mm×0.3mm×0.3mm)
- Can be used for one data, control or power line
- Ultra-low capacitance: 0.2pF (typical)

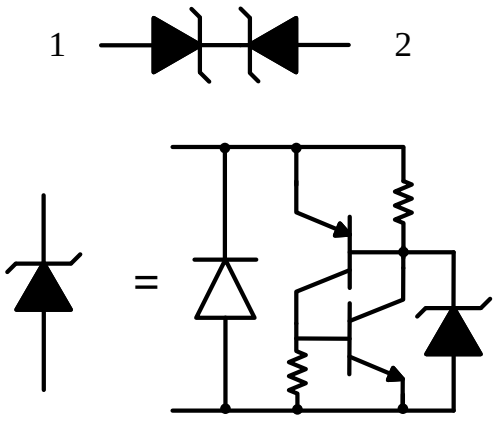
Applications

- USB3.x
- Near Field Communication (NFC) lines
- RF signal lines

Mechanical Characteristics

- DFN 0.6×0.3-2 package
- Marking: device code
- Packaging: tape and reel

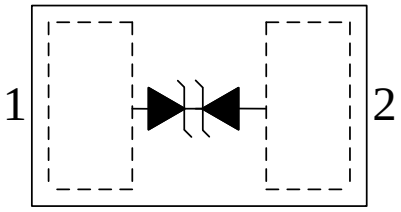
Circuit Diagram



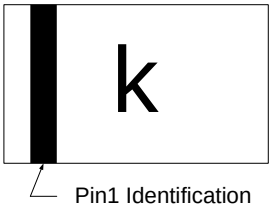
Ordering Information

Part Number	Package Type	Top Mark
SY205207DXC	DFN0.6×0.3-2 RoHS Compliant and Halogen Free	k

Pinout (Top View)



Marking Codes



Note: "k" is device code, fixed.

Absolute Maximum Rating			
Parameter	**Symbol**	**Value**	**Units**
Maximum Peak Pulse Current (8/20μs)	I_{PP}	9	A
Maximum Peak Pulse Power (8/20μs)	P_{PK}	50	W
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	±20 ±20	kV
Operating Temperature	T_{OPT}	-40/+85	℃
Storage Temperature	T_{STG}	-55/+150	°C

Electrical Characteristics (T_A = 25℃)						
Parameter	**Symbol**	**Test Condition**	**Min**	**Typ**	**Max**	**Unit**
Nominal Reverse Working Voltage	V_{RWM}				24.5	V
Reverse Leakage Current @ V_{RWM}	I_R	V_R = 24V, TA = 25°C		0.01	1	μA
Reverse Triggering Voltage @ I_{t1}	V_{t1}	I_{t1} = 50μA	25.5	30	40	V
Clamping Voltage @ I_{PP}	V_C (1)	I_{PP} = 9A, t_p = 8/20μs Combination Waveform, R_S = 12 Ω		5.5		V
Clamping Voltage @ I_{PP}	V_C(1)	I_{PP} = 16A, t_p = 10/100ns		7		V
Dynamic Resistance	R_{DYN}(1) (2)	t_p = 10/100ns		0.23		Ω
Dynamic Resistance	C_{ESD}(1)	V_R = 0V, f = 1MHz		0.2	0.35	pF

Notes 1: Guaranteed by design and not subject to production test.

Notes 2: R_{DYN} calculated based on I_{PP}=8A to I_{PP}=16A, t_p = 10/100ns.

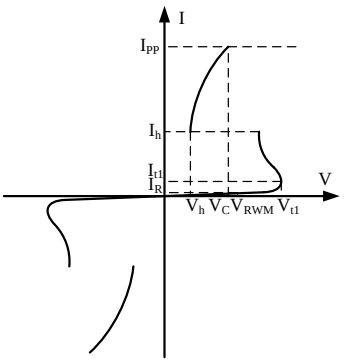
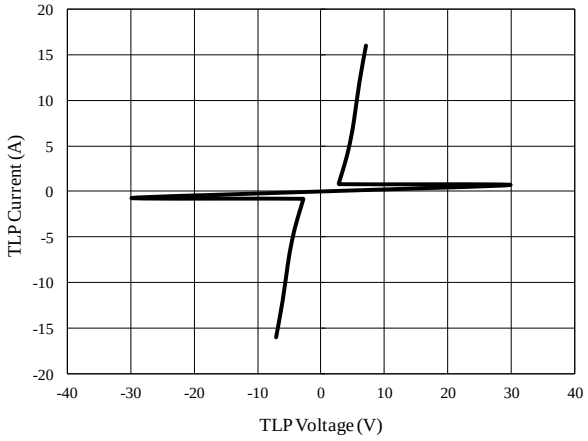


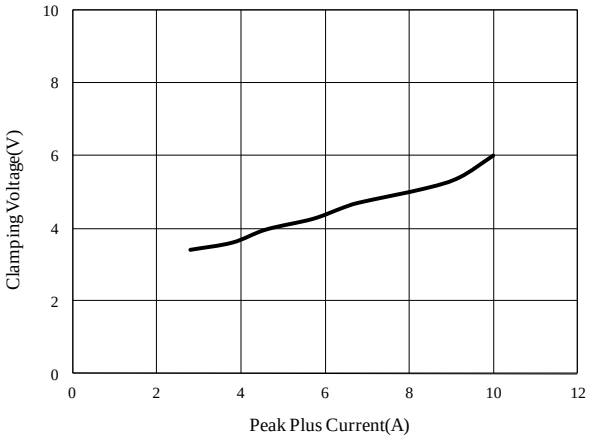
Figure 1. Bi-Directional TVS

Typical Characteristics

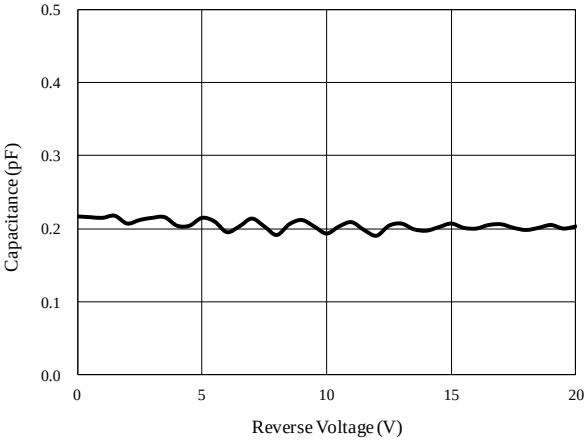
TLP Testing of I/O to I/O



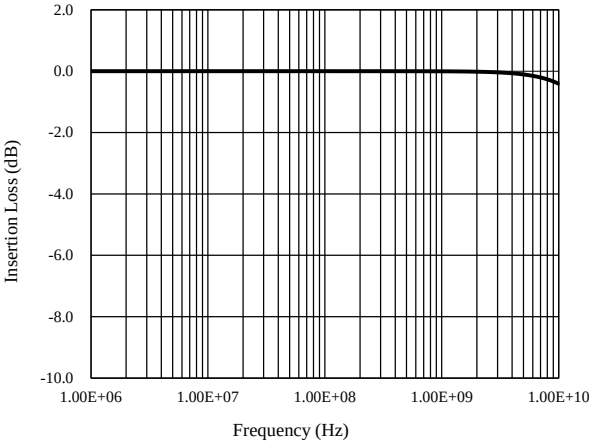
Clamping Voltage vs. Peak Pulse Current (8/20μs)



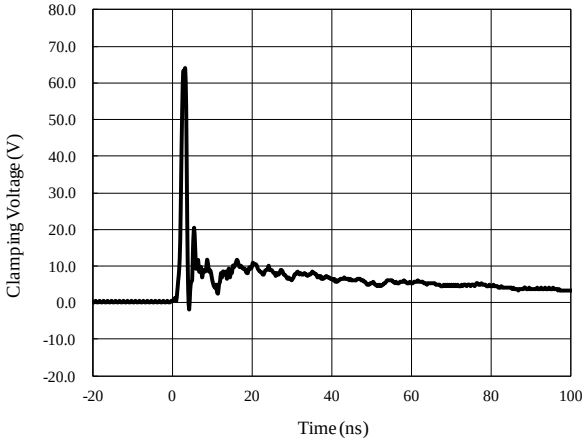
Capacitance vs. Voltage of I/O to I/O



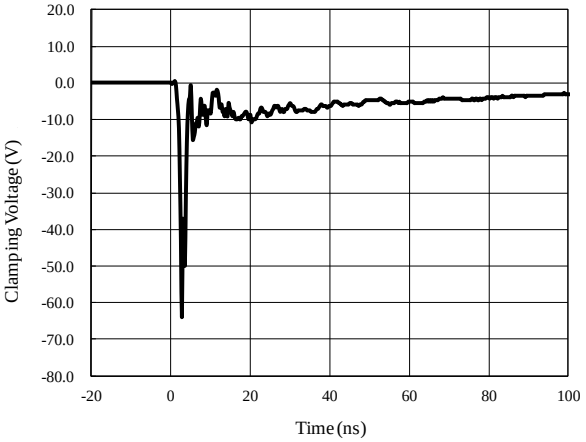
Insertion Loss S21 of I/O to I/O



ESD Clamping of I/O to I/O (+8kV Contact per IEC 61000-4-2)



ESD Clamping of I/O to I/O (-8kV Contact per IEC 61000-4-2)



Application Information

ESD Protection for USB Type-C

SY205207DXC can be used for ESD protection for USB Type-C. The pin connections are shown in figure 2 below. SY205207DXC must be placed between one data line and GND.

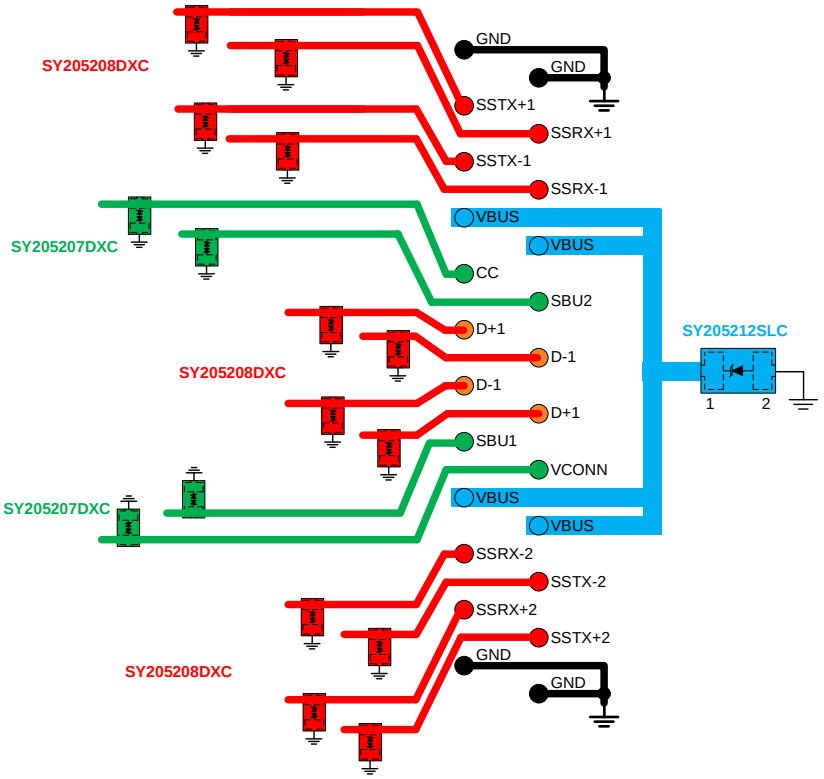


Figure 2. Typical ESD Protection for USB Type-C

ESD Protection for NFC Interface

SY205207DXC can also be used for Near Field Communication (NFC) antenna ESD protection. The high operating voltage (24V) does not clip the NFC signal and the small capacitance can avoid harmonic distortion of the RF signal. The typical application circuit is shown in figure 3.

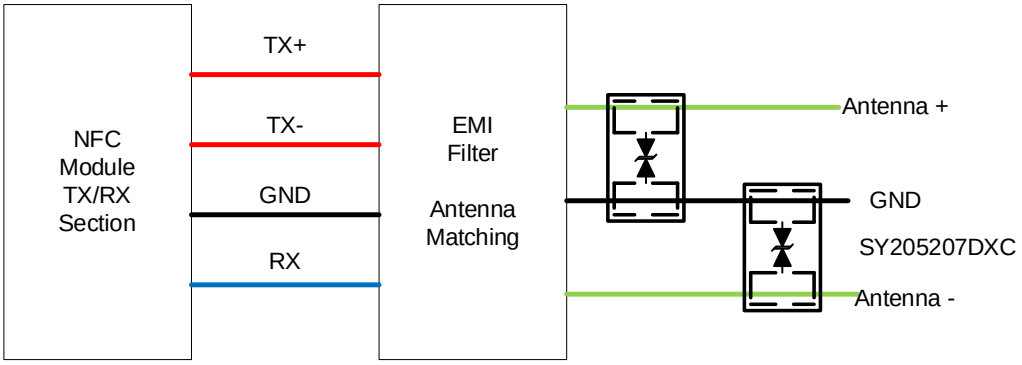


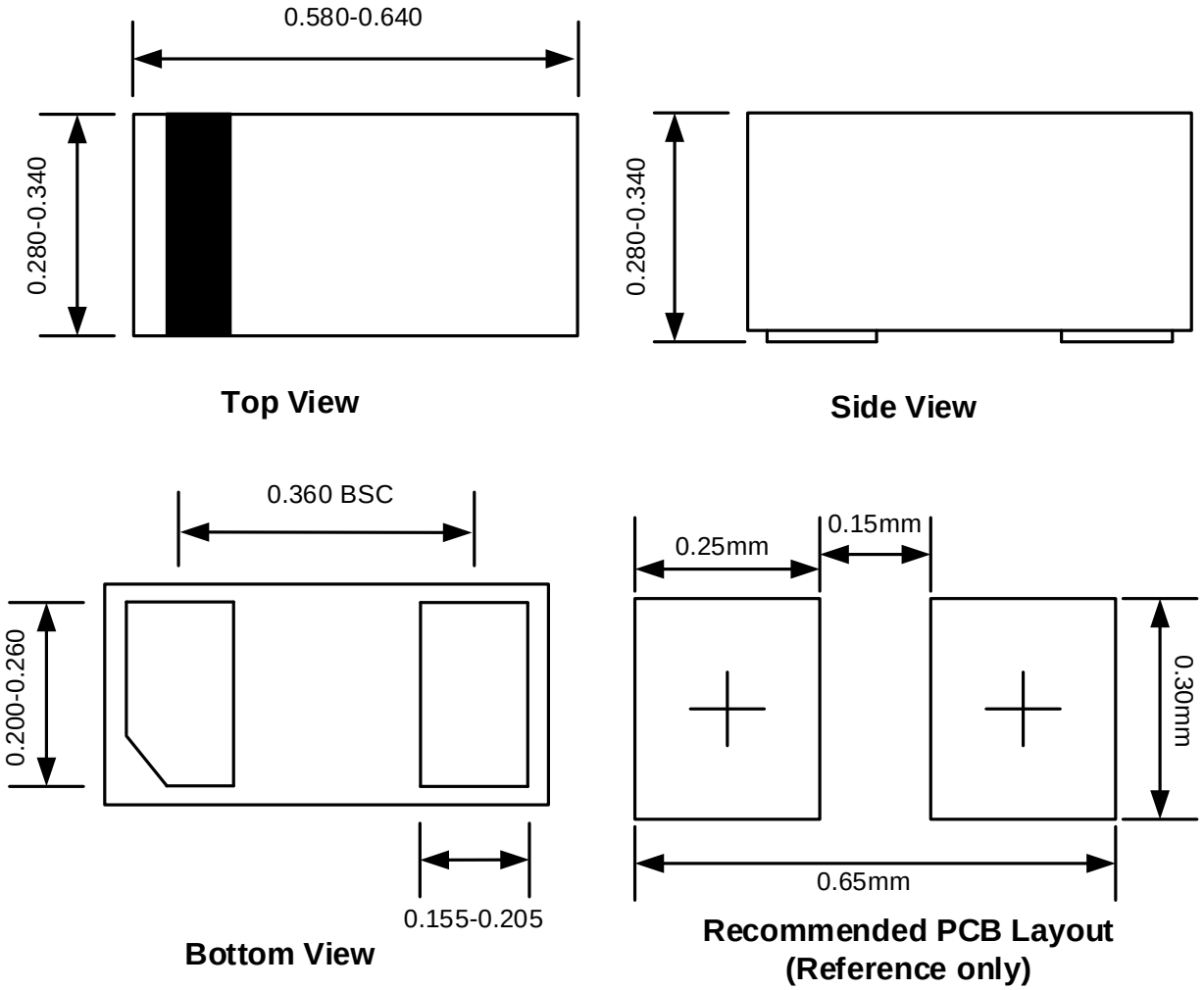
Figure 3. Typical ESD Protection for NFC Antenna

PCB Layout Guidelines

For optimum ESD protection and circuit performance, the following PCB layout guidelines are recommended:

- The distance between the SY205207DXC pin to the GND reference path should be as short as possible.
- Use a large via to connect SY205207DXC pin to the ground.
- Place SY205207DXC as close to the connector port as possible to reduce parasitic inductance and prevent ESD coupling into adjacent traces.
- Avoid running critical signals near board edges.

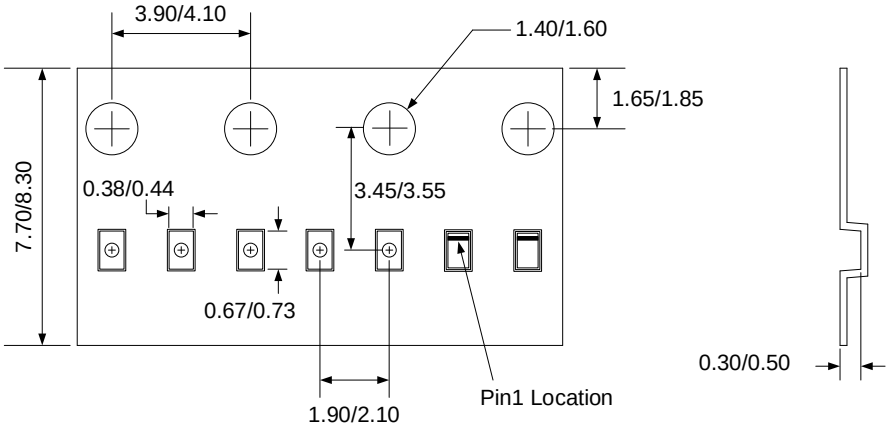
DFN0.6×0.3-2 Package Outline



Notes: All dimension in millimeter and exclude mold flash & metal burr

Tape and Reel Specification

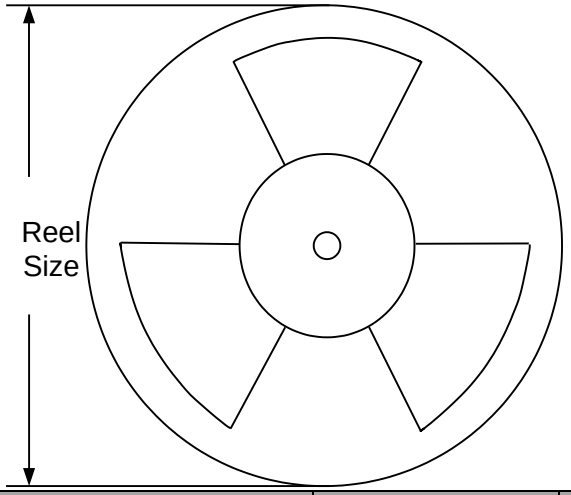
DFN0.6×0.3-2 Taping Orientation



Dimensions In mm

Feeding direction ⟶

Carrier Tape & Reel Specification for Packages



Package Types	Tape Width (mm)	Pocket Pitch(mm)	Reel Size (Inch)	Qty per Reel (pcs)
DFN0.6×0.3-2	8	2	7"	10000

Revision History

Revision Number	Revision Date	Description	Pages changed
0.9	04/23/2021	Initial Release	
1.0	04/23/2022	Production Release	

Revision history is for reference only and may not be comprehensive or complete.

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