

General Description

SY205263DVC is an ultra-low capacitance transient voltage suppressor (TVS) designed to provide electrostatic discharge (ESD) protection for high-speed data interfaces. With a typical capacitance of 0.6pF, SY205263DVC is designed to protect against over-voltage and over-current transient events. It complies with IEC 61000-4-2 (ESD), ($\pm 20\text{kV}$ air, $\pm 20\text{kV}$ contact discharge), and IEC 61000-4-5 (surge) (12A, 8/20 μs).

The combined features of ultra-low capacitance, ultra-small size and high ESD robustness make SY205263DVC ideal for high-speed data ports and high-frequency lines (e.g., USB 3.0 and DVI) applications. The low clamping voltage of the SY205263DVC guarantees minimum stress on the protected device.

Each SY205263DVC device can protect four high-speed data lines. The SY205263DVC is available in a DFN 2.5mm \times 1.0mm-10 pin package.

Features

- Protects Four Data Lines
- For Operating Voltage of 3.3V and Below
- Ultra-Low Capacitance: 0.6pF for each channel
- Ultra-Small Package: 2.5mm x 1.0mm x 0.55mm
- Low Leakage Current: 0.01 μA @ V_{RWM} (Typical)
- Low Clamping Voltage
- Transient Protection for High-Speed Data Lines
 - IEC 61000-4-2 (ESD) $\pm 20\text{kV}$ (Air) $\pm 20\text{kV}$ (Contact)
 - IEC 61000-4-5 (Surge) 12A (8/20 μs)
- Each I/O pin can withstand over 1000 ESD strikes for $\pm 8\text{kV}$ contact discharge.

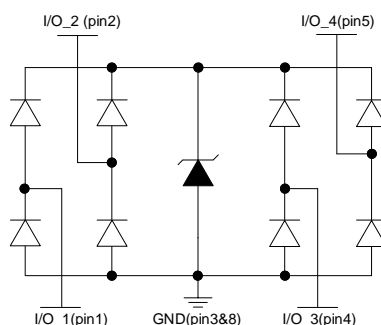
Applications

- Serial ATA
- PCI Express
- Desktops, Servers, and Notebooks
- MDDI Ports
- USB 2.0, 3.0 and 3.1
- Display Ports
- HDMI 1.3, 1.4 and 2.0
- Digital Visual Interfaces (DVI)

Mechanical Characteristics

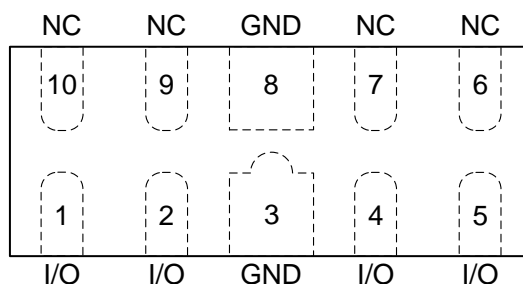
- DFN2.5 \times 1.0-10 Package
- Marking: Device Code, Date Code
- Packaging: Tape and Reel

Circuit Diagram



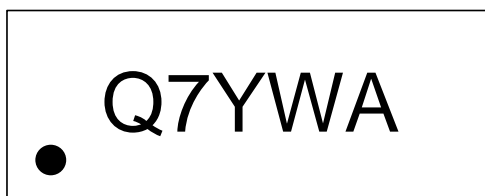
Ordering Information

Part Number	Package Type	Top Mark
SY205263DVC	DFN2.5×1.0-10 RoHS Compliant and Halogen Free	Q7YWA



Pinout (Top View)

Marking Codes



Note 1: “Q7” is device code, fixed.

Note 2: “YWA” is date code.

Absolute Maximum Rating			
Parameter	Symbol	Value	Units
Maximum Peak Pulse Current (8/20μs)	I _{PP}	12	A
Maximum Peak Pulse Power (8/20μs)	P _{PK}	60	Watts
ESD per IEC 61000-4-2 (Air)	V _{ESD}	±20	kV
ESD per IEC 61000-4-2 (Contact)			
Operating Temperature	T _{OPT}	-40/+125	°C
Storage Temperature	T _{STG}	-55/+150	°C

Electrical Characteristics (T _A = 25°C)						
Parameter	Symbol	Test Condition	Mini	Typ	Maxi	Units
Nominal Reverse Working Voltage	V _{RWM}				3.3	V
Reverse Leakage Current @ V _{RWM}	I _R	V _{RWM} = 3.3V, T _A = 25°C		0.01	0.1	μA
Triggering Voltage @ I _{t1}	V _{t1}	I _{t1} = 1mA	3.6			V
Holding Voltage @ I _h	V _h	I _h = 100mA	0.8			V
Clamping Voltage @ I _{PP}	V _C ¹	I _{PP} = 12A, t _p = 8/20μs		5.0		V
Clamping Voltage @ I _{PP}	V _C ¹	I _{PP} = 16A, t _p = 10/100ns		4.5		V
Dynamic Resistance	R _{DYN} ^{1,2}	t _p = 10/100ns		0.2		Ω
Parasitic Capacitance	C _{ESD} ¹	V _R = 3.3V, f = 1MHz		0.60		pF

Note 1: Guaranteed by design and not subject to production test.

Note 2: R_{DYN} calculated based on I_{PP}=8A to I_{PP}=16A, t_p = 10/100ns.

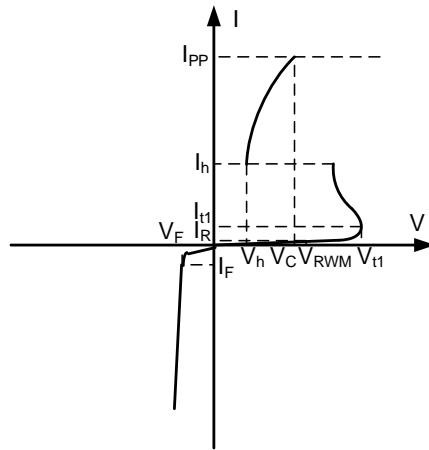
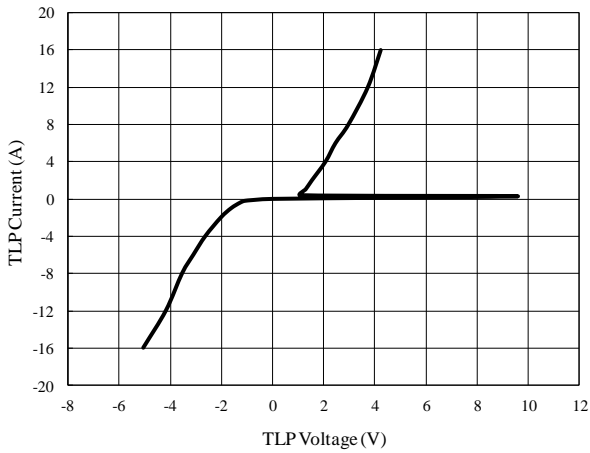


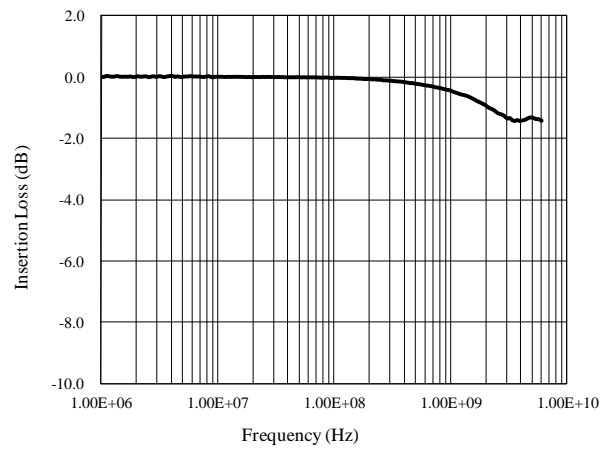
Figure 1. Uni-directional TVS

Typical Characteristics

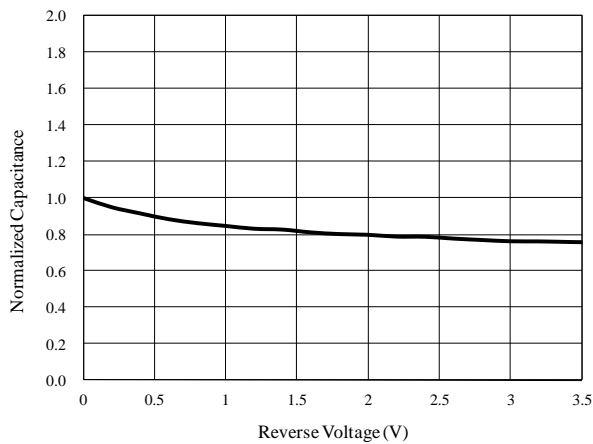
TLP Testing of I/O to GND



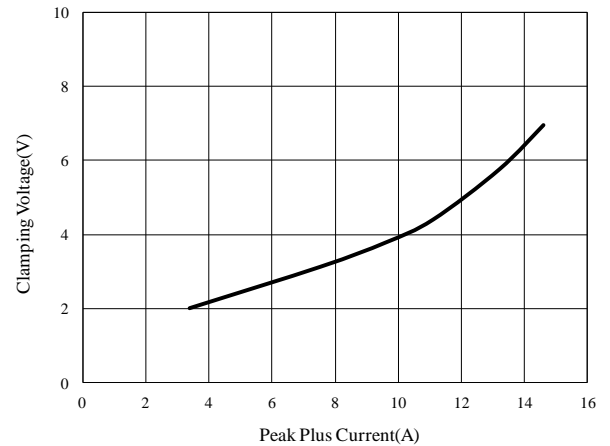
Insertion Loss S21 of I/O to GND



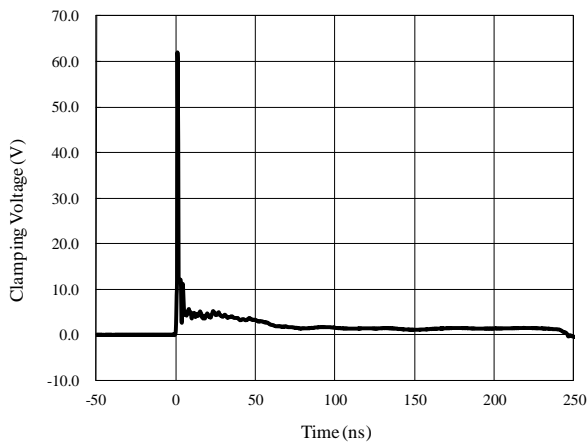
Normalized Capacitance vs. Voltage of I/O to GND



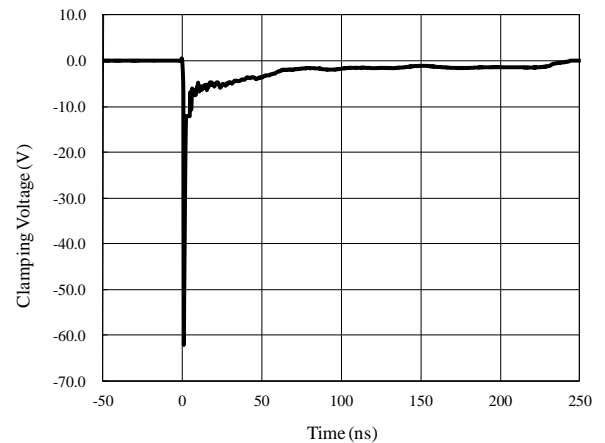
Clamping Voltage vs. Peak Pulse Current (8/20μs)



ESD Clamping of I/O to GND (+8kV Contact per IEC 61000-4-2)



ESD Clamping of I/O to GND (-8kV Contact per IEC 61000-4-2)



Application Information

SY205263DVC provides ESD protection for four data lines simultaneously. The pin connections are shown in the figure below.

Four parallel data lines, from the protected device to the I/O port connector, can directly connect to the four SY205263DVC I/O pins. Pin3 and Pin8 of SY205263DVC are the GND pins, which should connect to the GND reference on the PCB. The connection traces should be as short as possible to minimize the parasitic inductance.

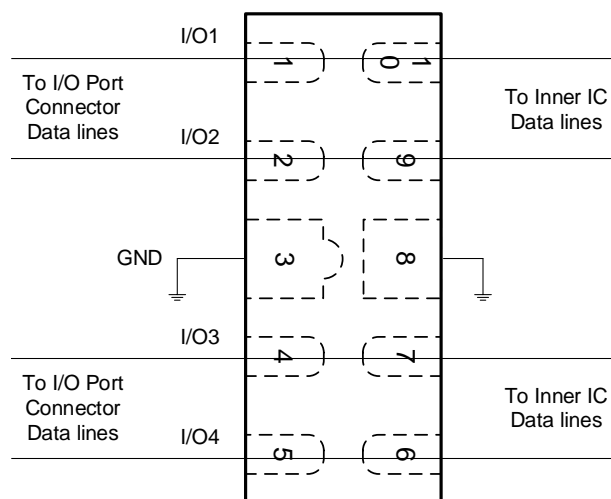


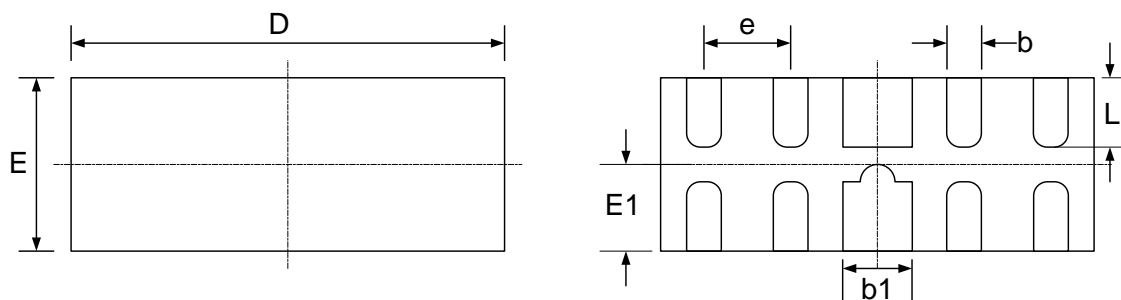
Figure 2. SY205263DVC Pin Connections in PCB

PCB Layout Guidelines

For optimum ESD protection and circuit performance, the following circuit board guidelines are recommended:

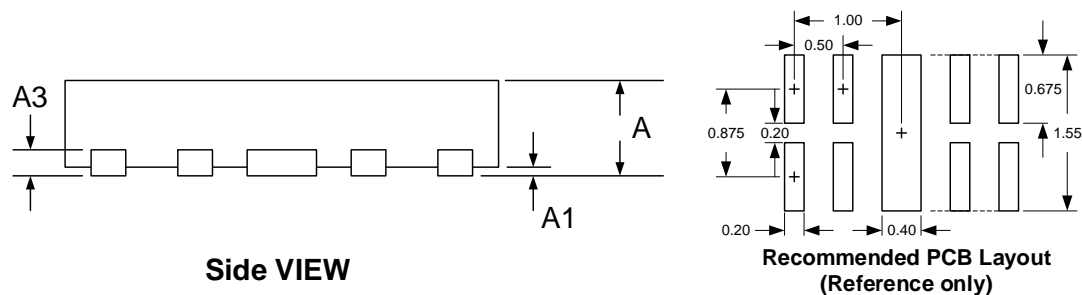
- Place SY205263DVC as close to the connector or terminal ports as possible.
- Use a large via to connect the SY205263DVC pin to the ground.
- Avoid running signals near board edges.
- The SY205263DVC should be placed near the protected line.
- The distance between the SY205263DVC ground pin and the GND reference path should be as short as possible.

DFN2.5×1.0-10 Package Outline



TOP VIEW

BOTTOM VIEW



Side VIEW

Recommended PCB Layout
(Reference only)

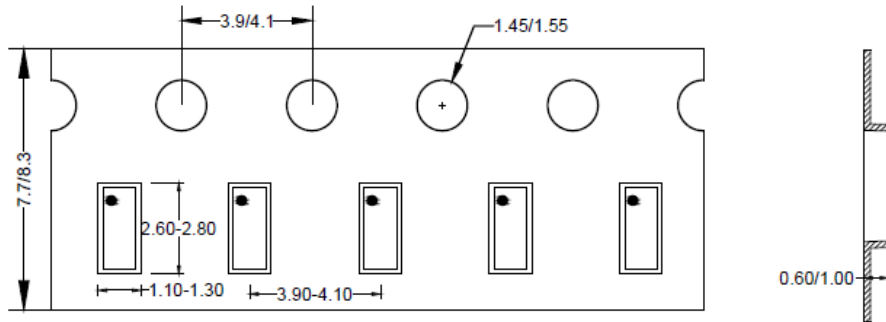
Package Dimensions

Symbol	Dimensions (mm)	
	Minimum	Maximum
A	0.500	0.600
A1	0.000	0.050
A3	0.150REF.	
b	0.150	0.250
b1	0.350	0.450
E1	0.460	0.560
D	2.450	2.550
E	0.950	1.050
e	0.500 BSC	
L	0.330	0.430

Note: All dimensions are in millimeters and exclude mold flash and metal burr.

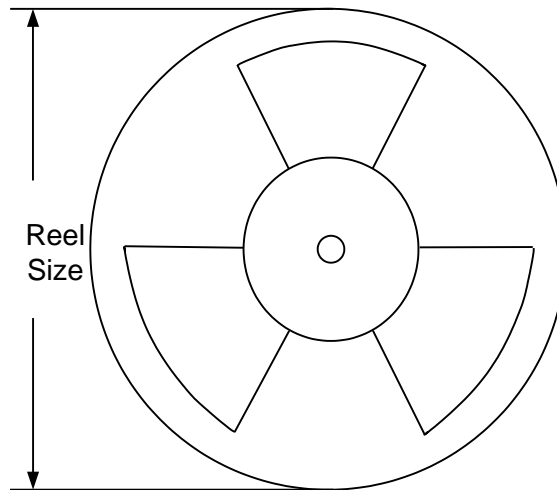
Tape and Reel Specification

DFN2.5x1.0-10 Taping Orientation



Feeding direction →

Carrier Tape & Reel Specification for Packages



Package Types	Tape Width (mm)	Pocket Pitch(mm)	Reel Size (Inch)	Qty per Reel(pcs)
DFN2.5x1.0-10	8	4	7"	3000



Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Revision Number	Revision Date	Description	Pages changed
0.9	10/21/2020	Initial Release	
1.0	10/21/2021	Production Release	

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