SY21245

High Efficiency, 8A, 40V Input Synchronous Buck Converter

General Description

The SY21245 high efficiency synchronous Buck converter can deliver 8A output current over a wide input voltage range from 4V to 40V. The SY21245 employs a constant on-time and ripple-based control strategy to achieve fast transient responses. The SY21245 integrates the top MOSFET and bottom MOSFET with very low $R_{DS(ON)}$ to minimize the conduction loss.

Silergy's constant on-time (COT) ripple-based control method supports high input/output voltage ratios (low duty cycles), and fast transient response while maintaining a near constant operating frequency over line, load, and output voltage ranges. This control method provides stable operation without complex compensation and even with low ESR ceramic capacitors.

The SY21245 also provides input under voltage lockout, cycle-by-cycle current limit, over temperature protection, over voltage protection and output short circuit protection. The SY21245 is available in a compact QFN3.5×3.5-20 package.

Features

- Low $R_{DS(ON)}$ for Internal MOSFETs: 25mΩ Top, 12mΩ Bottom
- Wide Input Voltage Range: 4V ~ 40V
- Up to 8A Output Current Capability
- Precise ± 1% 0.6V Reference
- COT Ripple-Based Control to Achieve Fast Transient Response
- Internal Soft-Start Limits the Inrush Current
- Power Good Indicator
- Output Auto-Discharge Function
- 350kHz/500kHz Selectable Switching Frequency
- PFM/FCCM Selectable Light Load Operation Mode
- Programmable Valley Current Limit Threshold
- Cycle-by-Cycle Peak and Valley Current Limit Protection
- Hiccup Mode Output Short Circuit Protection
- Auto-Recovery Mode Output Over Voltage Protection
- Auto-Recovery Mode Over Temperature Protection
- Input Under Voltage Lockout (UVLO)
- RoHS-Compliant and Halogen-Free
- Compact Package: QFN3.5×3.5-20

Applications

- LCD TV
- Set-Top Box
- Notebook
- High-Power AP Router

Typical Application

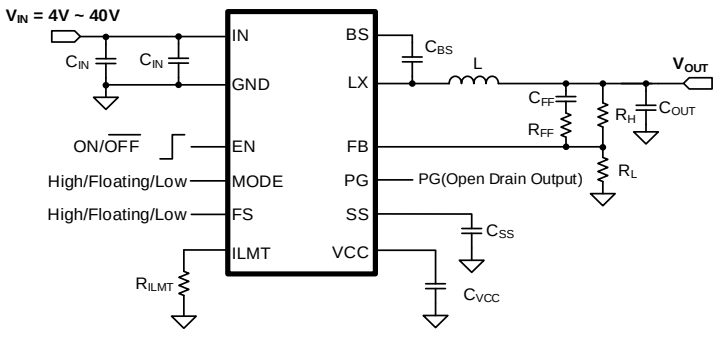


Figure 1. Typical Application Circuit

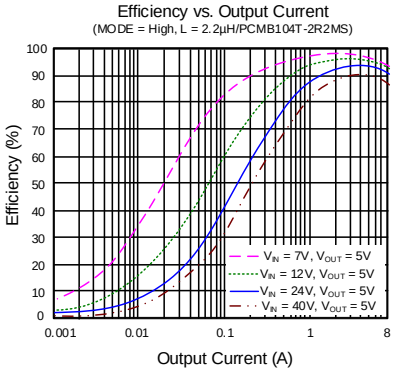


Figure 2. Efficiency vs. Output Current

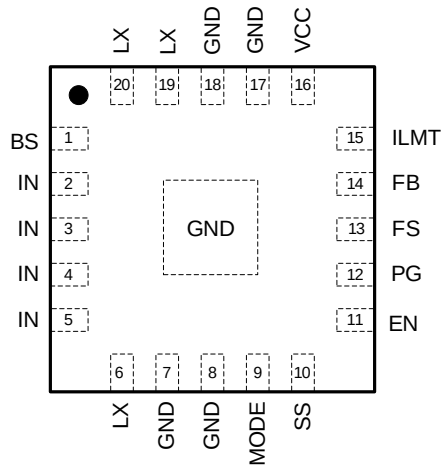
Ordering Information

SY21145 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Part Number	Package Type	Top Mark
SY21245RBC	QFN3.5×3.5-20 RoHS-Compliant and Halogen-Free	**BDY*xyz***

x = year code, y = week code, z = lot number code

Pinout (top view)



Pin Description

Pin No	Pin Name	Pin Description
1	BS	Bootstrap pin. Supply top FET gate driver. Connect a 0.1μF ceramic capacitor between the BS pin and the LX pin.
2, 3, 4, 5	IN	Input pin. Decouple this pin to the GND with at least a 10μF ceramic capacitor.
6, 19, 20	LX	Inductor pin. Connect this pin to the switching node of the inductor.
7, 8, 17, 18, Exposed pad	GND	Ground pin.
9	MODE	Light load operation mode selection pin. Pull this pin low for PFM operation; pull this pin high or leave it floating for FCCM operation.
10	SS	Soft-start time programming pin. Connect a capacitor from this pin to ground to program the soft-start time. t_{SS} (ms) = C_{SS} (nF) × 0.6V/6μA. Leave this pin floating for default 1ms soft-start time application.
11	EN	Enable control pin of the device. Pull this pin high to turn on the device; pull this pin low to turn off the device. Do not leave this pin floating.
12	PG	Power good indicator pin. Open drain output when the output voltage is within 90% to 122% of the regulated value.
13	FS	CCM switching frequency operation selection pin. Pull this pin low for 350kHz; pull this pin high or leave it floating for 500kHz.
14	FB	Output feedback pin. Connect this pin to the center point of resistor divider.
15	ILMT	Valley current limit threshold programming pin. $I_{LMT,BOT}$ (A) = 3600/R_{ILMT} (kΩ). Leave this pin floating for the default 6A valley current limit threshold.
16	VCC	Internal 3.3V LDO output pin. Power supply for internal circuits and driving circuit. Decouple this pin to ground with at least a 4.7μF ceramic capacitor.

Block Diagram

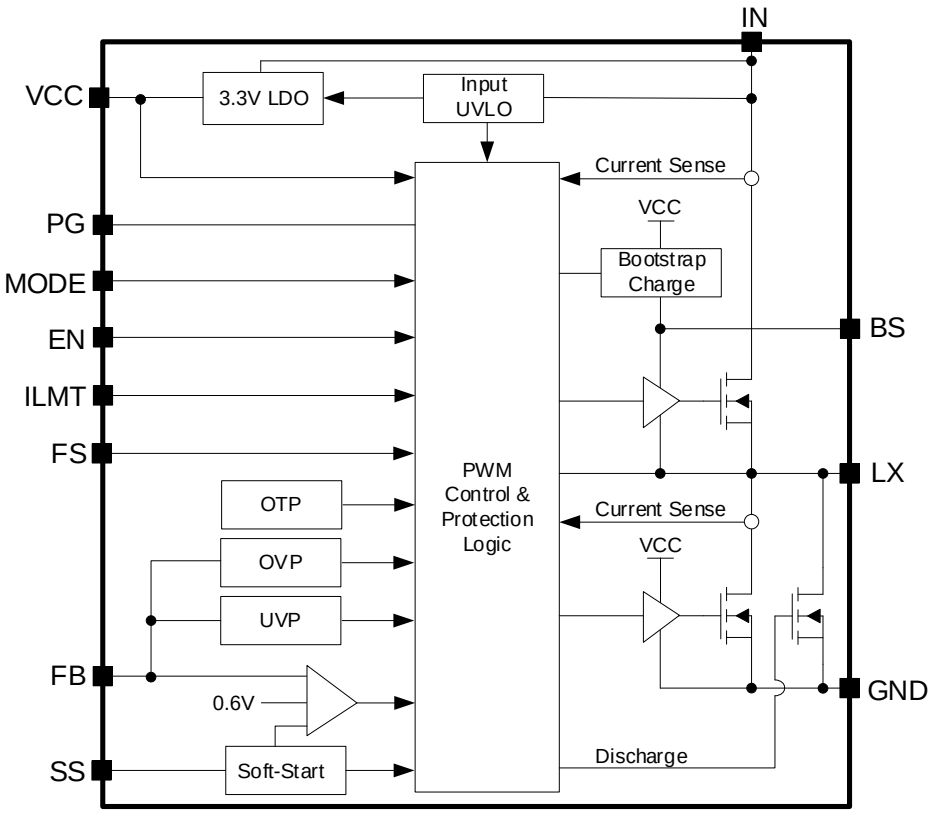


Figure 3. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
IN	-0.3	40	V
BS-LX, VCC, FB	-0.3	4	
ILMT, FS, PG, EN, MODE, SS, LX	-0.3	V_{IN} + 0.3	
Dynamic LX Voltage in 10ns Duration	V_{GND} - 5	V_{IN} + 3	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering, 10s)		260	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	28	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	4	
P_D Power Dissipation T_A = 25°C	3.6	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
Input Voltage	4	40	V
Continuous Output Current		8	A
Junction Temperature, Operating	-40	125	°C

Electrical Characteristics

(V_{IN} = 12V, C_{OUT} = 66µF, C_{FF} = 470pF, R_{FF} = 1kΩ, T_J = 25°C, I_{OUT} = 1A unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input	Input Voltage Range	V_{IN}		4		40	V
	Input UVLO Threshold	$V_{IN,UVLO}$				3.9	
	Input UVLO Hysteresis	$V_{IN,HYS}$			0.3		
	Quiescent Current	I_Q	I_{OUT} = 0A, V_{FB} = V_{REF} × 105%		60		µA
	Shutdown Current	I_{SHDN}	EN = Low			4	
Output	Voltage Range	V_{SET}		0.6		24	V
	Feedback Reference Voltage	V_{REF}		0.594	0.6	0.606	
	FB Input Current	I_{FB}	V_{FB} = 3.3V	-50		50	nA
	Soft-Start Charging Current	I_{SS}			6		µA
	Internal Soft-Start Time	t_{SS}	Leave SS pin floating		1		ms
	Discharge Current	I_{DIS}	V_{OUT} = 5V		100		mA
	OVP Threshold	V_{OVP}	V_{FB} rising	116	122	128	%V_{REF}
	OVP Hysteresis	$V_{OVP,HYS}$			10		
	OVP Delay Time	$t_{OVP,DLY}$			15		µs
	UVP Threshold	$V_{OUT,UVP}$	V_{FB} falling	45	50	55	%V_{REF}
	UVP Delay Time	$t_{UVP,DLY}$			200		µs
	UVP Hiccup On-Time	$t_{HICCUP,ON}$	Leave SS pin floating		3		ms
	UVP Hiccup Off-Time	$t_{HICCUP,OFF}$	Leave SS pin floating		21		
MOSFET	Top FET $R_{DS(ON)}$	$R_{DS(ON),TOP}$			25		mΩ
	Bottom FET $R_{DS(ON)}$	$R_{DS(ON),BOT}$			12		
	Top FET Current Limit Threshold	$I_{LMT,TOP}$	R_{ILMT} = 300kΩ		10		A
	Bottom FET Current Limit Threshold Program Range	$I_{ILMT,RNG}$	R_{ILMT} = 300kΩ ~ 600kΩ (Note 4)	6		12	
	Bottom FET Current Limit Threshold	$I_{LMT,BOT}$	R_{ILMT} = 300kΩ	9.6	12	14.4	
	Bottom FET Reverse Current Limit Threshold	$I_{LMT,RVS}$	MODE = High	3.5			
Enable (EN)	Input Voltage High	$V_{EN,H}$		1.5			V
	Input Voltage Low	$V_{EN,L}$				0.4	
	Leakage Current	I_{EN}				1	µA
MODE	Input Voltage High	$V_{MODE,H}$		V_{CC} - 0.8			V
	Input Voltage Low	$V_{MODE,L}$				0.4	
	Leakage Current	I_{MODE}				1	µA
Frequency	FS Input Voltage High	$V_{FS,H}$		V_{CC} - 0.8			V
	FS Input Voltage High	$V_{FS,L}$				0.4	
	FS Leakage Current	I_{FS}				1	µA

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
	Switching Frequency	f_{SW}	Leave FS pin floating, V_{OUT} = 5V, CCM	400	500	600	kHz
	Minimum On-Time	$t_{ON,MIN}$			80		ns
	Minimum Off-Time	$t_{OFF,MIN}$			160		
Power Good	Rising Threshold	$V_{PG,R}$	V_{FB} rising, PG from low to high	85	90	95	%V_{REF}
	Falling Threshold	$V_{PG,F}$	V_{FB} falling, PG from high to low	81	85	89	
	OVP Threshold	$V_{PG,OVP}$	V_{FB} rising, PG from high to low	116	122	128	
	OVP Recovery Threshold	$V_{PG,REC}$	V_{FB} falling, PG from low to high	104	110	116	
	Delay Time	$t_{PG,DLY}$	Low to high		200		µs
			High to low		10		
	Low Voltage	$V_{PG,LOW}$	Sink 5mA to PG pin, V_{FB} = 0V			0.4	V
VCC	Output Voltage	V_{CC}		3.15	3.3	3.45	
OTP	Temperature	T_{OTP}	(Note 4)		150		℃
	Temperature Hysteresis	T_{HYS}	(Note 4)		15		

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Package thermal resistance is measured in the natural convection at T_A = 25°C on a four-layer Silergy Evaluation Board.

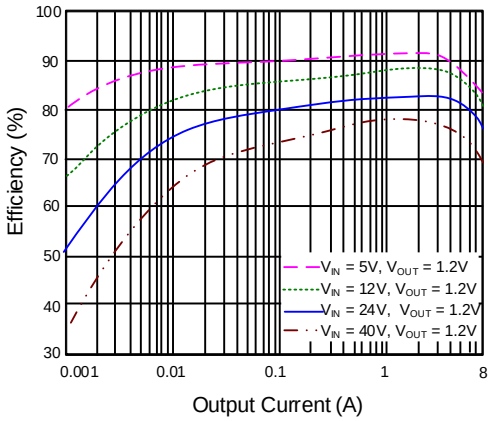
Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Guaranteed by design.

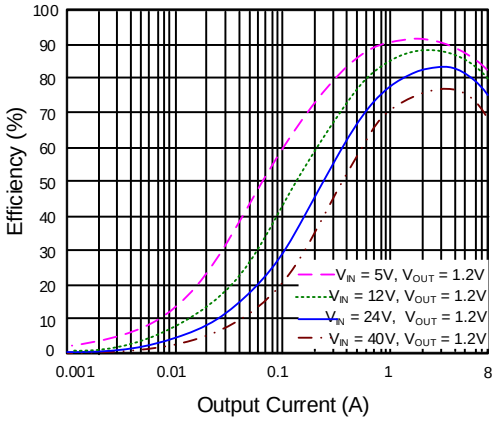
Typical Performance Characteristics

(V_{IN} = 12V, C_{OUT} = 66µF, C_{FF} = 470pF, R_{FF} = 1kΩ, T_J = 25°C, f_{SW} = 500kHz unless otherwise specified)

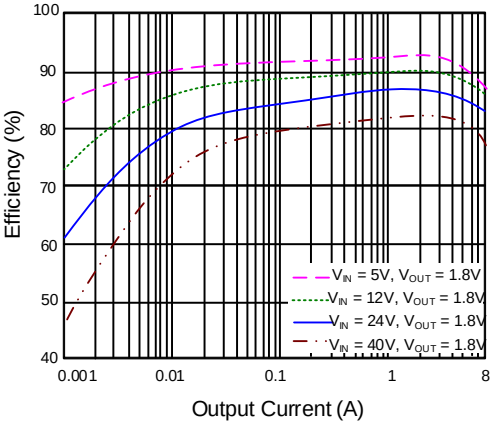
Efficiency vs. Output Current
(MODE = Low, L = 1.0µH/PCMB104T-1R0MS)



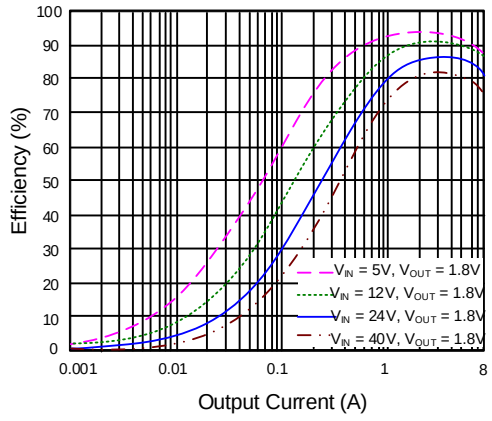
Efficiency vs. Output Current
(MODE = High, L = 1.0µH/PCMB104T-1R0MS)



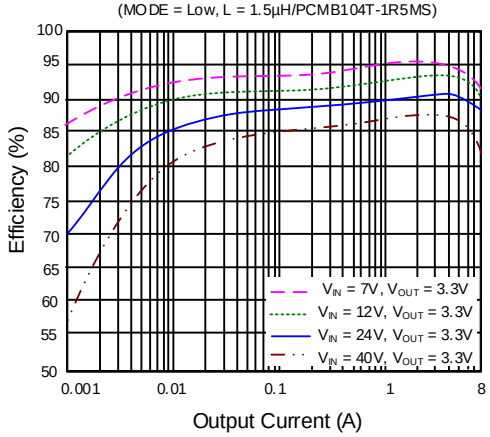
Efficiency vs. Output Current
(MODE = Low, L = 1.0µH/PCMB104T-1R0MS)



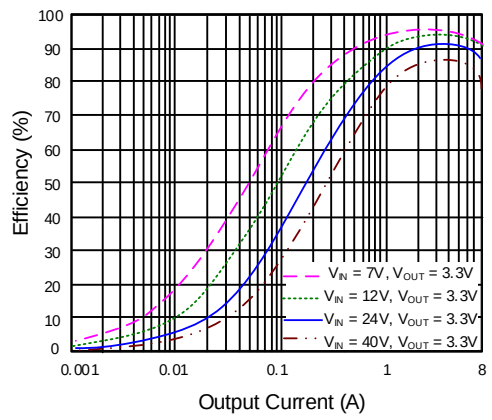
Efficiency vs. Output Current
(MODE = High, L = 1.0µH/PCMB104T-1R0MS)



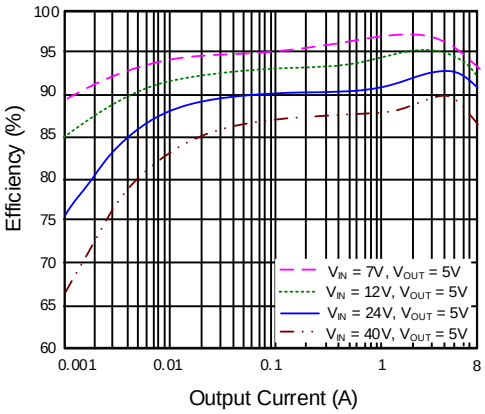
Efficiency vs. Output Current
(MODE = Low, L = 1.5µH/PCMB104T-1R5MS)



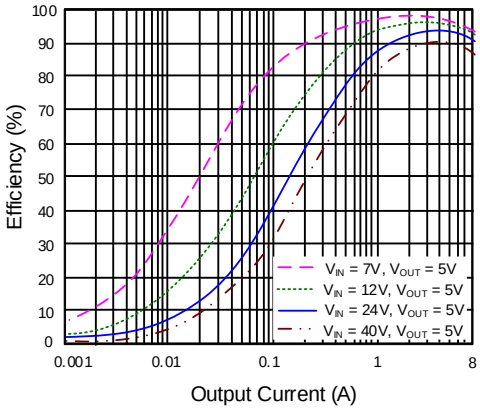
Efficiency vs. Output Current
(MODE = High, L = 1.5µH/PCMB104T-1R5MS)



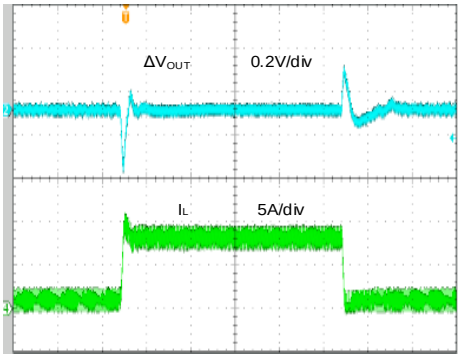
Efficiency vs. Output Current
(MODE = Low, L = 2.2μH/PCMB104T-2R2MS)



Efficiency vs. Output Current
(MODE = High, L = 2.2μH/PCMB104T-2R2MS)

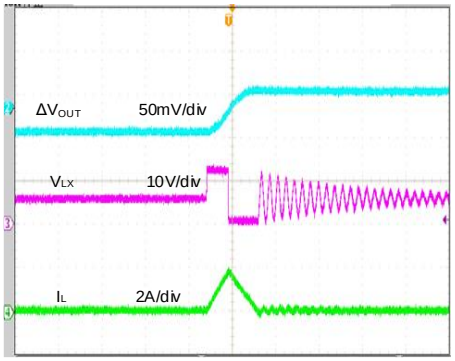


Load Transient
(V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 0.8A ~ 8A)



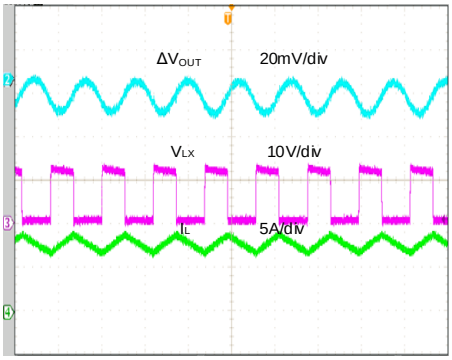
Time (100μs/div)

Output Ripple
(V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 0A, Mode = Low)



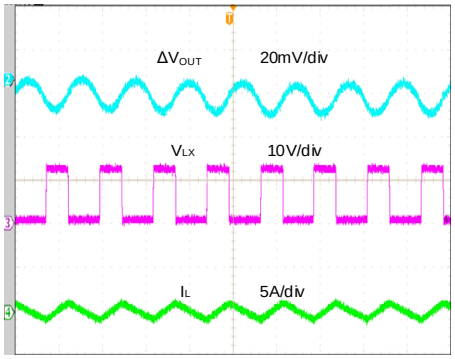
Time (2μs/div)

Output Ripple
(V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 8A)



Time (2μs/div)

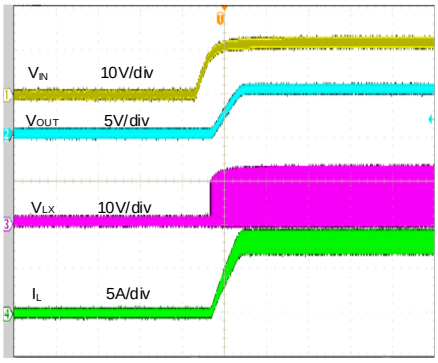
Output Ripple
(V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 0A, Mode = High)



Time (2μs/div)

Startup from V_{IN}

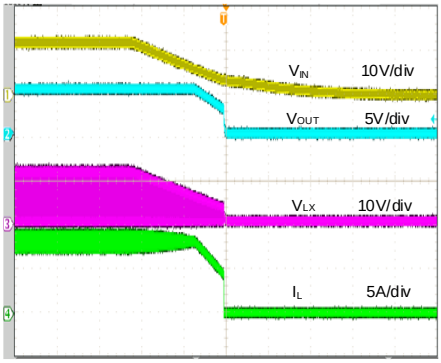
(V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 8A)



Time (2ms/div)

Shutdown from V_{IN}

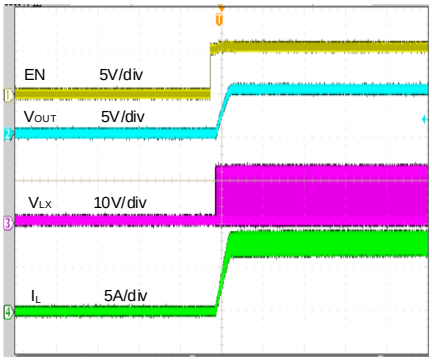
(V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 8A)



Time (4ms/div)

Startup from Enable

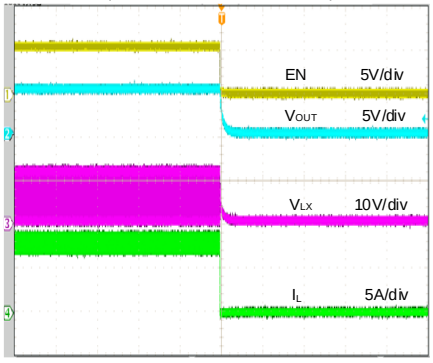
(V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 8A)



Time (4ms/div)

Shutdown from Enable

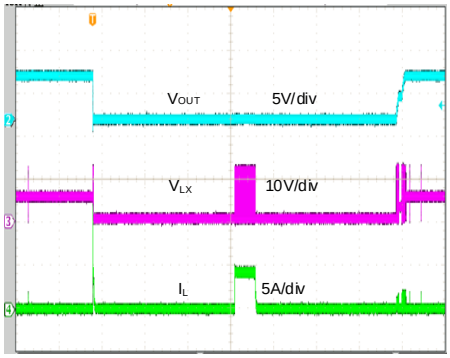
(V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 8A)



Time (800μs/div)

Output Short Circuit Protection

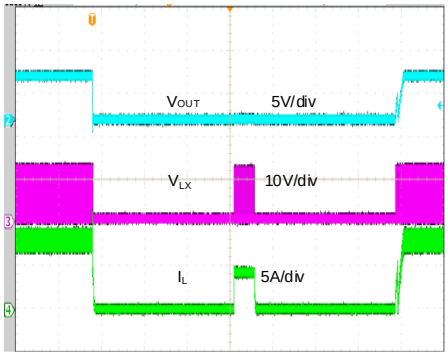
(V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 0A ~ short)



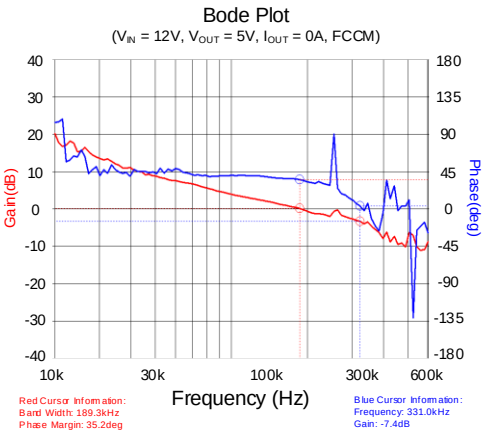
Time (10ms/div)

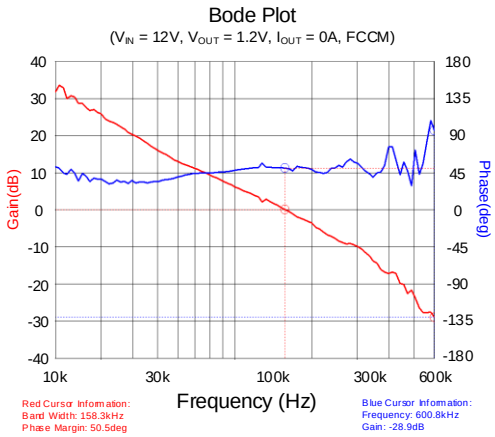
Output Short Circuit Protection

(V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 8A ~ short)



Time (10ms/div)





Detailed Description

General Features

Constant On-Time Architecture

Fundamental to any constant on-time (COT) architecture is the one-shot circuit or on-time generator, which determines how long to turn on the top FET. Each on-time (t_{ON}) is a "fixed" voltage ration,

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{SW}}$$

For example, considering that a hypothetical converter targets 3.3V output from a 12V input at 500kHz, the target on-time is

$$\frac{3.3\text{V}}{12\text{V}} \times \frac{1}{500\text{kHz}} = 550\text{ns}$$

Each t_{ON} pulse is triggered by the feedback comparator when the output voltage as measured at FB node drops below the regulated value. After one t_{ON} period, a minimum off-time ($t_{OFF,MIN}$) is imposed before any further switching is initiated, even if the output voltage is lower than the regulated value. This approach avoids making any switching decisions during the noisy periods just after switching events and while the switching node (LX) is rapidly rising or falling.

In a COT architecture, there is no fixed clock, so the top FET can turn on almost immediately after a load transient and subsequent switching pulses can be quickly initiated, ramping the inductor current up to meet load requirements with minimal delays. Traditional current mode or voltage mode control methods must simultaneously monitor the feedback voltage, current feedback and internal ramps and compensation signals to determine when to turn off the top FET and turn on the bottom FET. Considering these small signals in a switching environment are difficult to be noise-free after transmitting large current, making those architectures difficult to apply in noisy environments, even under low duty cycle operation.

Minimum Duty Cycle and Maximum Duty Cycle

In the COT architecture, there is no limitation for small duty cycle, since at very low duty cycle operation, once the on-time is close to the minimum on time, the switching frequency can be reduced as needed to always ensure a proper operation.

Under T_J = -40℃ ~ 125℃ condition, the device can support adjustable output and up to 70% duty cycle operation under 500kHz operation.

Instant-PWM Operation

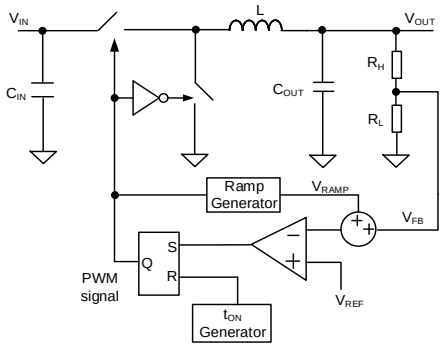


Figure 4. Instant-PWM

Silergy's COT ripple-based control strategy adds several proprietary improvements to the traditional COT architecture. Whereas most legacy based on COT implementations require a dedicated connection to the output voltage terminal to calculate the t_{ON} duration, instant-PWM control method derives this signal internally. Another improvement optimizes operation with low ESR ceramic output capacitors. In many applications it is desirable to utilize very low ESR ceramic output capacitors, but legacy COT converters may become unstable in these cases because the beneficial ramp signal that results from the inductor current flowing into the output capacitor maybe become too small to maintain stable operation. For this reason, instant-PWM synthesizes a virtual replica of this signal internally. This internal virtual ramp and the feedback voltage are combined and compared to the reference voltage. When the sum is lower than the reference voltage, the t_{ON} pulse is triggered as long as the minimum off-time has been satisfied and the inductor current as measured in the bottom FET is lower than the bottom FET current limit threshold. As the t_{ON} pulse is triggered, the bottom FET turns off and the top FET turns on. Then the inductor current ramps up linearly during the t_{ON} period. At the conclusion of the t_{ON} period, the top FET turns off, the bottom FET turns on and the inductor current ramps down linearly. This action also initiates the minimum off-time timer to ensure sufficient time for stabilizing any transient

conditions and settling the feedback comparator before the next cycle is initiated. This minimum off-time is relatively short so that during fast speed load transient t_{ON} can be retriggered with minimal delay, allowing the inductor current to ramp quickly to provide sufficient energy to the load side.

In order to avoid shoot-through, a dead time (t_{DEAD}) is generated internally between the top FET off and the bottom FET on period or the bottom FET off and the top FET on period.

Light Load Operation Mode Selection

PFM or FCCM light load operation is selected by MODE pin. Pull MODE pin low for PFM operation, and pull this pin high or leave it floating for FCCM operation.

If PFM light load operation is selected, under light load conditions, typically

$$I_{OUT} < \frac{1}{2} \times \Delta I_L$$

The current through the bottom FET will ramp to near zero before the next t_{ON} time. When this occurs, the bottom FET turns off, preventing recirculation current that can seriously reduce efficiency under these light load conditions. As load current is further reduced, the combined feedback and ramp signals remain much higher than the reference voltage, the instant-PWM control loop will not trigger another t_{ON} until needed, so the apparent operating switching frequency will correspondingly drop, further enhancing efficiency. The switching frequency can be lower than audible frequency area under deep light load or null load conditions. Continuous conduction mode (CCM) resumes smoothly as soon as the load current increases sufficiently for the inductor current to remain above zero at the time of the next t_{ON} cycle. The Buck converter enters CCM once the load current exceeds the critical level. After that, the switching frequency stays fairly constant over the output current range. The critical level of the load current is determined with

$$I_{OUT} = \frac{\Delta I_L}{2} = \frac{V_{OUT} \times (1 - D)}{2 \times f_{SW} \times L}$$

If FCCM light load operation is selected, under light load conditions, the bottom FET still turns on even when the inductor current crosses zero. Current flow will continue until the next t_{ON} cycle appears. The Buck converter always operates under continuous conditions mode and keeps fairly constant switching frequency over all the output current range.

Input Under Voltage Lockout (UVLO)

To prevent operation before the internal circuitry is ready and to ensure that the top and bottom FETs can be sufficiently enhanced, the device incorporates one input under voltage lockout protection.

The device remains in a low current state and LX switching actions are inhibited until V_{IN} exceeds its own UVLO (rising) threshold. At that time, if EN is enabled, the device will start up by initiating a soft-start ramp. If V_{IN} falls below $V_{IN,UVLO}$ less than the input UVLO hysteresis, LX switching actions will again be suppressed.

If the input UVLO threshold is low for some high input UVLO threshold requirement applications, use EN to adjust the input UVLO by adopting two external divided resistors.

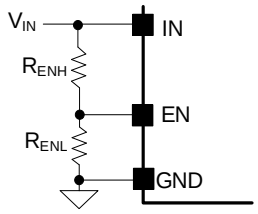


Figure 5. UVLO Adjustment

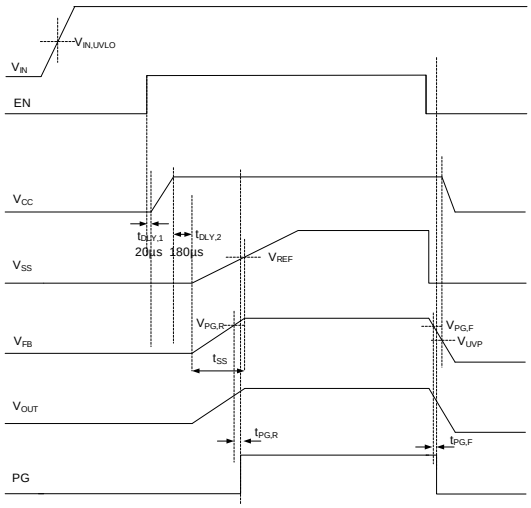
Enable Control

The EN input is a high-voltage capable input with logic-compatible threshold. When EN is driven > 1.5V, normal device operation will be turned on. When driven < 0.4V, the device will be turned off, reducing the input current to < 4μA.

It is not recommended to connect EN and IN directly. A resistor in a range of 1kΩ to 1MΩ should be used if EN is pulled high by IN.

Startup and Shutdown

The SY21245 incorporates an internal soft-start circuit to smoothly ramp the output to the desired voltage whenever the device is enabled. Internally, the soft-start circuit clamps the output at a low voltage and then allows the output to rise to the desired voltage over one programmable soft-start time, which avoids high current flow and transients during startup. The startup and shutdown sequence is shown below.



After V_{IN} exceeds its own UVLO (rising) threshold, the VCC is turned on after the delay time $t_{DLY,1}$ if EN is also high, the Buck converter is turned on after another delay time t_{DLY2} after VCC voltage is ready.

When the output voltage is 90% of the regulated value, PG is in the high-impedance state after the delay time $t_{PG,R}$.

If the output is pre-biased to a certain voltage before start-up, the Buck converter disables the switching of both the top FET and the bottom FET until the internal soft-start voltage V_{SS} exceeds the sensed output voltage at the FB node.

The SY21245 provides one programmable soft-start time function. The minimum soft-start time is 1ms (typical) when the SS pin is floating. Connect a capacitor across the SS pin and GND to program the soft-start time, as calculated using the following equation:

$$t_{SS}(ms) = C_{SS}(nF) \times \frac{0.6(V)}{6(\mu A)}$$

Output Power Good Indicator

The Buck power good indicator is an open drain output controlled by a window comparator connected to the feedback signal. If V_{FB} is greater than $V_{PG,R}$ and less than $V_{PG,OVP}$ for at least the power good delay time (low to high), PG will be in the high-impedance state.

PG should be connected to V_{IN} or another voltage source through a resistor (e.g., 100kΩ). After V_{IN} rises until the internal initial power is ready, the PG FET is turned on so that PG is pulled to GND before output voltage is ready. After feedback voltage V_{FB} reaches $V_{PG,R}$, PG is pulled high (after the delay time typical 200µs). When V_{FB} drops to $V_{PG,F}$, or rises to V_{OVP} for the OVP delay time, PG is pulled low (after the delay time typical 10µs).

Output Auto-Discharge Function

SY21245 discharges the output voltage when the Buck converter shuts down from V_{IN} or EN, or OTP, so that output voltage can be discharged in a minimal time, even output load current is zero. The discharge FET in parallel with the bottom FET turns on after the bottom FET turns off when shut down logic is triggered, the discharge FET turns off when the output voltage falls below UVP threshold. The output discharge current is typically 100mA when the LX voltage is 5V. Note that the discharge FET is not active beyond these shutdown conditions.

External Bootstrap Capacitor Connection

This device integrates a floating power supply for the gate driver of the top FET. Proper operation requires a 0.1µF low ESR ceramic capacitor to be connected between BS and LX. This bootstrap capacitor provides the gate driver supply voltage for the N-channel top FET.

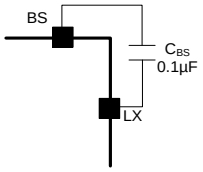


Figure 7. Bootstrap Capacitor Connection

VCC Output

SY21245 integrates VCC, one high performance, low drop-out linear regulator (LDO) and its output voltage set-point is fixed 3.3V, which can power the internal gate drivers, PWM logic, analog circuitry and other blocks. Once the input voltage exceeds its own UVLO (rising) threshold, and EN is high, VCC is turned on and supplied power by V_{IN}. Connect at least a 4.7μF low ESR ceramic capacitor from VCC to GND.

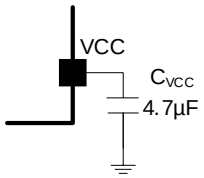


Figure 8. VCC Output

Switching Frequency Select

The SY21245 features a selectable switching frequency of 350kHz or 500kHz using the FS pin. Pull FS low to select 350kHz; pull FS high or leave it floating to select 500kHz.

Fault Protection Modes

Output Current Limit

The Buck converter features cycle-by-cycle "valley" current limit (bottom FET current limit). Inductor current is monitored in the bottom FET when it turns on and as the inductor current ramps down. If the monitored current is higher than the bottom FET current limit threshold, t_{ON} is inhibited until the current returns back to the limit threshold or lower.

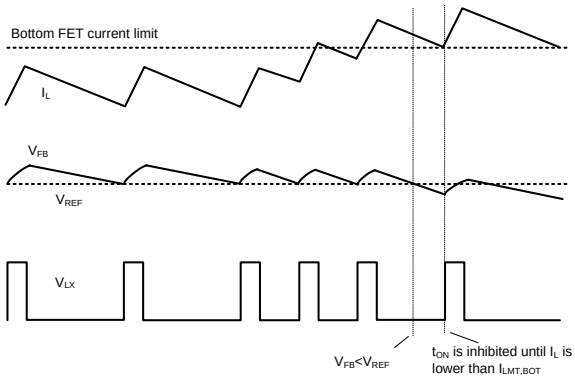


Figure 9. Output Current Limit

The bottom FET current limit threshold can be programmable by the ILMT pin. Leave this pin open for the default 6A bottom FET current limit threshold, and connect one resistor from this pin to GND to program if the bottom FET current limit threshold is not enough.

$$I_{LMT,BOT} = \frac{3600}{R_{LIMT}(k\Omega)}$$

When the valley current limit occurs, the output current limit value is

$$I_{LMT,BOT} = \frac{3600}{R_{LIMT}(k\Omega)} I_{LMT,OUT} = I_{LMT,BOT} + \frac{\Delta I_L}{2}$$

$$I_{LMT,OUT} = I_{LMT,BOT} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

The valley current limit protection limits the inductor current but the OCP itself is one non-latch protection. When the load current is higher than the bottom FET current limit threshold by one half of the peak-to-peak inductor ripple current, the output voltage starts to drop. Once the feedback voltage falls lower than the under voltage protection (UVP) threshold and continues for the UVP delay time, the Buck converter will enter hic-cup status. On the other hand, over temperature protection may also be triggered under the over current condition and the Buck converter will enter auto-recovery status.

When FCCM light load operation is selected, there is one bottom FET reverse current limit to ensure the negative current can be limited to a safe level. During t_{OFF} time, the bottom FET current is monitored. If the monitored current exceeds the reverse current limit threshold, the bottom FET will be turned off and another t_{ON} will be triggered.

The Buck converter also features cycle-by-cycle "peak" current limit (top FET current limit). During t_{ON} time, the top FET current is monitored. If the monitored current exceeds the top FET current limit threshold, the top FET will be turned off, the bottom FET will be turned on. t_{ON} can be not inhibited any more once bottom FET current is lower than the bottom FET current limit threshold.

Output Under Voltage Protection (UVP)

If V_{OUT} < ~50% of the regulated value for approximately 200μs occurring when the output short circuit or the load

current is much heavier than the maximum current capacity, the output under voltage protection (UVP) will be triggered, and the Buck converter will enter into hic-cup protection mode. When SS pin is floating, the hic-cup on time is 3ms, and the hic-cup off time is 21ms. If the output fault conditions are removed, the Buck converter will go back to normal operation in the nearest hic-cup on time.

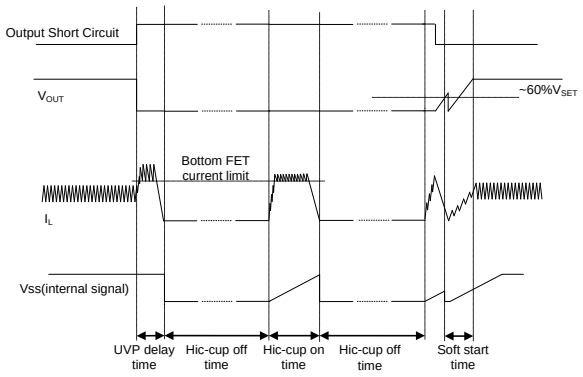


Figure 10. Output Short Circuit Protection

To avoid output overshoot, the internal voltage V_{SS} should be pulled low for a while when V_{FB} exceeds UVP threshold if the output fault conditions are removed during hic-cup on time, then the V_{SS} will rise smoothly to ramp the output to the desired voltage during a new soft-start cycle.

Output Over Voltage Protection (OVP)

This Buck converter includes output over voltage protection (OVP). If the output voltage rises above the feedback regulation level, the top FET naturally remains off and different actions are adopted in different operation mode.

When operating in PFM light load mode, if the output voltage remains high, the bottom FET remains on until the inductor current reaches zero and LX node switching actions are suppressed. LX node switching actions will be recovered once the combined feedback and ramp signals become lower than the reference voltage.

When operating in FCCM light load mode, if the output voltage remains high, the reverse current limit will be triggered and inductor current average value will become negative, trying to make output voltage lower. If the output voltage continues to rise and exceeds the output over voltage threshold for more than OVP delay time, output over voltage protection (OVP) will be triggered, and LX node switching actions will be suppressed. LX node switching actions will be recovered once the combined feedback and ramp signals become lower than the reference voltage. False OVP may happen under light load condition if the inductance value is chosen too low and reverse current limit threshold is triggered just under steady state if the load current is zero.

Over Temperature Protection (OTP)

The Buck converter includes over temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. This will shut down the Buck converter when the junction temperature exceeds 150°C. Once the junction temperature cools down by approximately 15°C, the Buck converter will resume normal operation after a complete soft-start cycle. For continuous operation, provide adequate cooling so that the junction temperature will not exceed the OTP threshold.

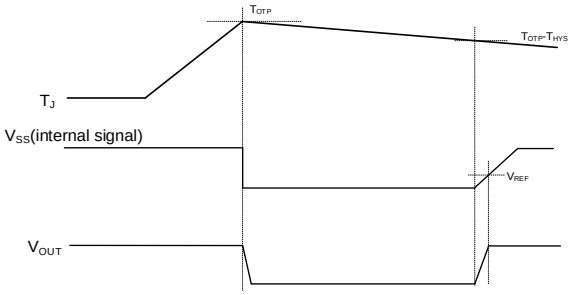


Figure 11. Over Temperature Protection

Design Procedure

Feedback Resistor Divider Selection

Choose R_H and R_L to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_H and R_L. A value of between 10kΩ and 1MΩ is strongly recommended for both resistors. If V_{SET} is 3.3V, R_H = 100kΩ is chosen, then using following equation, R_L can be calculated to be 22.1kΩ.

$$R_L = \frac{0.6V}{V_{SET} - 0.6V} \times R_H$$

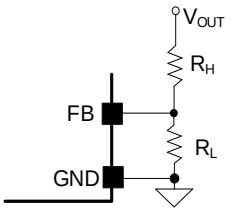


Figure 12. Feedback Resistor Divider

Input Capacitor Selection

Input filter capacitors are needed to reduce the ripple voltage on the input, to filter the switched current drawn from the input supply and to reduce potential EMI. When selecting the input capacitor, be sure to select a voltage rating at least 20% greater than the maximum voltage of the input supply and a temperature rating above the system requirements. X5R series ceramic capacitors are most often selected due to their small size, low cost, surge current capability and high RMS current ratings over a wide temperature and voltage range. However, systems that are powered by a wall adapter or long inductive cable may be susceptible to significant inductive ringing at the input to the device. In these cases, consider adding some bulk capacitance like electrolytic, tantalum or polymer type capacitors. Using a combination of bulk capacitors (to reduce overshoot or ringing) in parallel with ceramic capacitors (to meet the RMS current requirements) is helpful in these cases.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current,

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1-D)}$$

The worst-case condition occurs at D = 0.5, then

$$I_{CIN\_RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

On the other hand, the input capacitor value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification.

Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated by

$$V_{CIN\_RIPPLE,CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1-D)$$

The worst-case condition occurs at D = 0.5, then

$$V_{CIN\_RIPPLE,CAP,MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. In most applications a single 10µF X5R capacitor is sufficient. Take care to locate the ceramic input capacitor as close to the device's IN and GND pin as possible.

Inductor Selection

The inductor is necessary to supply constant current to the output load while being driven by the LX node switching actions.

The Buck converter operates well over a wide range of inductance values. This flexibility allows for optimization to find the best trade-off of efficiency, cost and size for a particular application. Selecting a low inductance value will help reduce size and cost and enhance transient response, but will increase peak inductor ripple current, reducing efficiency and increasing output voltage ripple. The low DC resistance (DCR) of these low inductance value inductors may help reduce DC losses and increase efficiency. On the other hand, choosing higher inductance value inductors tend to have higher DCR and will slow transient response.

A reasonable compromise between size, efficiency, and transient response can be determined by selecting a ripple current (ΔI_L) about 20% ~ 40% of the desired full output load current. Start calculating the approximate inductance value by selecting the input and output voltages, the operating frequency (f_{SW}), the maximum output current ($I_{OUT,MAX}$) and estimating a ΔI_L as some percentage of that current.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Use this inductance value to determine the actual inductor ripple current (ΔI_L) and required peak current inductor current $I_{L,PEAK}$.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

$$I_{L,PEAK} = I_{OUT,MAX} + \frac{\Delta I_L}{2}$$

Select an inductor with a saturation current and thermal rating in excess of $I_{L,PEAK}$.

If FCCM light load operation is selected, make sure the inductance value is high enough to avoid reverse current limit threshold being triggered just under steady state if the load current is zero.

For highest efficiency, select an inductor with a low DCR that meets the inductance, size and cost targets. Low loss ferrite materials is recommended to be selected.

Inductor Design Example

Consider a typical design for a Buck converter providing 3.3V_{OUT} at 8A from 12V_{IN}, operating at 500kHz and using target inductor ripple current (ΔI_L) of 40% or 3.2A. Determine the approximate inductance value at first:

$$L = \frac{3.3V \times (12V - 3.3V)}{12V \times 500kHz \times 3.2A} = 1.495\mu H$$

Next, select the nearest standard inductance value, in this case 1.5μH, and calculate the resulting inductor ripple current (ΔI_L):

$$\Delta I_L = \frac{3.3V \times (12V - 3.3V)}{12V \times 500kHz \times 1.5\mu H} = 3.19A$$

$$I_{L,PEAK} = 8A + \frac{3.19A}{2} = 9.60A$$

The resulting 3.19A ripple current is 3.19A/8A is ~39.9%, well within the 20% ~ 40% target.

$$I_{L,PEAK,RVS} = \frac{3.19A}{2} = 1.56A < I_{LMT,RVS}$$

Finally, select an available inductor with a saturation current higher than the resulting $I_{L,PEAK}$ of 9.60A.

Output Capacitor Selection

The Buck converter provides excellent performance with a wide variety of output capacitor types. Ceramic and POS types are most often selected due to their small size and low cost. Total capacitance is determined by the transient response and output voltage ripple requirements of the system.

Steady State Output Ripple

Steady state output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔI_L) on the output capacitors ESR (ESR ripple) as well as the stored charge (capacitive ripple). When considering total ripple, both should be considered.

$$V_{RIPPLE,\ ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,\ CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

Consider a typical application with ΔI_L = 3.19A using three 22μF ceramic capacitors, each with an ESR of ~6mΩ for parallel total of 66μF and 2mΩ ESR.

$$V_{RIPPLE,\ ESR} = 3.19A \times 2m\Omega = 6.38mV$$

$$V_{RIPPLE,\ CAP} = \frac{3.19A}{8 \times 66\mu F \times 500kHz} = 12.08mV$$

Total ripple = 18.46mV. The actual capacitive ripple may be higher than calculated value because the capacitance decreases with the voltage on the capacitor.

Using a 150μF 40mΩ POS cap, the above result is

$$V_{RIPPLE,\ ESR} = 3.19A \times 40m\Omega = 127.60mV$$

$$V_{RIPPLE,\ CAP} = \frac{3.19A}{8 \times 150\mu F \times 500kHz} = 5.32mV$$

Total ripple = 132.92mV.

Output Transient Undershoot/Overshoot

If very fast load transient must be supported, consider the effect of the output capacitor on the output transient undershoot and overshoot. The Buck converter responds quickly to changing load conditions, however, some considerations must be needed, especially when using small ceramic capacitors which have low capacitance at low output voltages which results in insufficient stored energy for load transient. Output transient undershoot and overshoot have two causes: voltage changes caused by the ESR of the output capacitor and voltage changes caused by the output capacitance and inductor current slew rate.

ESR undershoot or overshoot may be calculated as

$$V_{ESR} = \Delta I_{OUT} \times ESR$$

Using the ceramic capacitor example above and a fast load transient of ± 4A, V_{ESR} = ± 4A × 2mΩ = ± 8mV. The POS capacitor result with the same load transient, V_{ESR} = ± 4A × 40mΩ = ± 160mV.

Capacitive undershoot (load increasing) is a function of the output capacitance, the load step, the inductor value and the input-output voltage difference and the maximum duty factor. During a fast load transient, the maximum duty factor of the Buck converter is a function of t_{ON} and the minimum t_{OFF} as the control scheme is designed to rapidly ramp the inductor current by grouping together many t_{ON} pulses in this case. The maximum duty factor D_{MAX} may be calculated by

$$D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF,MIN}}$$

Given this, the capacitive undershoot may be calculated by

$$V_{UNDERSHOOT,CAP} = -\frac{L \times \Delta I^2{}_{OUT}}{2 \times C_{OUT} \times (V_{IN,MIN} \times D_{MAX} - V_{OUT})}$$

Consider a 4A load increase using the ceramic capacitor case when V_{IN} = 12V.At V_{OUT} = 3.3V, the result is t_{ON} = 550ns, $t_{OFF,MIN}$ = 160ns, D_{MAX} = 550 / (550 + 160) = 0.758 and

$$V_{UNDERSHOOT,CAP} = -\frac{1.5\mu H \times (4A)^2}{2 \times 66\mu F \times (12V \times 0.758 - 3.3V)} = -31.37mV$$

Using the POS capacitor case, the above result is

$$V_{UNDERSHOOT,CAP} = -\frac{1.5\mu H \times (4A)^2}{2 \times 150\mu F \times (12V \times 0.758 - 3.3V)} = -13.80mV$$

Capacitive overshoot (load decreasing) is a function of the output capacitance, the inductor value and the output voltage.

$$V_{OVERSHOOT,CAP} = \frac{L \times \Delta I^2{}_{OUT}}{2 \times C_{OUT} \times V_{OUT}}$$

Consider a 4A load decrease using the ceramic capacitor case above. At V_{OUT} = 3.3V the result is

$$V_{OVERSHOOT,CAP} = \frac{1.5\mu H \times (4A)^2}{2 \times 66\mu F \times 3.3V} = 55.1mV$$

Using the POS capacitor case, the above result is

$$V_{OVERSHOOT,CAP} = \frac{1.5\mu H \times (4A)^2}{2 \times 150\mu F \times 3.3V} = 24.2mV$$

Combine the ESR and capacitive undershoot and overshoot to calculate the total overshoot and undershoot for a given application.

Load Transient Considerations

The SY21245 adopts the COT ripple-based control strategy to achieve good stability and fast transient response. In applications with high step load current, adding an RC network R_{FF} and C_{FF} may further speed up the load transient response. R_{FF} = 1kΩ and C_{FF} = 220pF have been shown to perform well in most applications. Increase C_{FF} will speed up the load transient response if there is no stability issue.

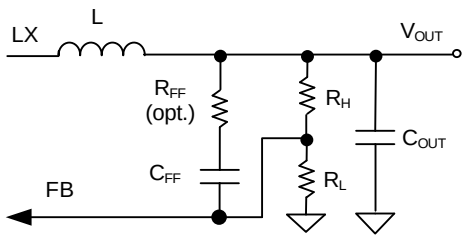


Figure 13. Feed-Forward Network

Note that when C_{OUT} > 500µF and minimum load current is low, set feed-forward values as R_{FF} = 1kΩ and C_{FF} = 2.2nF to provide sufficient ripple to FB for small output ripple and good transient behavior.

Thermal Design Considerations

The maximum power dissipation depends on multiple factors: PCB layout, IC package thermal resistance, local airflow, and the junction temperature relative to ambient. The maximum power dissipation may be calculated as:

$$P_{D,MAX} = \frac{(T_{J,MAX} - T_A)}{\theta_{JA}}$$

where $T_{J,MAX}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

To comply with the recommended operating conditions, the maximum junction temperature is 125°C. The junction to ambient thermal resistance θ_{JA} is layout dependent. For the QFN3.5×3.5-20 package the thermal resistance θ_{JA} is 28°C /W when measured on a standard Silergy four-layer thermal test board. These standard thermal test layouts have a very large area with long 2-oz. copper traces connected to each IC pin and very large, unbroken 1-oz. internal power and ground planes.

Meeting the performance of the standard thermal test board in a typical tiny evaluation board area requires wide copper traces well-connected to the IC's backside pads leading to exposed copper areas on the component side of the board as well as good thermal via from the exposed pad connecting to a wide middle-layer ground plane and, perhaps, to an exposed copper area on the board's solder side.

The maximum power dissipation at T_A = 25°C may be calculated using the following formula:

$$P_{D,MAX} = (125°C - 25°C) / (28°C/W) = 3.57W$$

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J,MAX}$ and thermal resistance θ_{JA}. Use the derating curve in figure below to calculate the effect of rising ambient temperature on the maximum power dissipation.

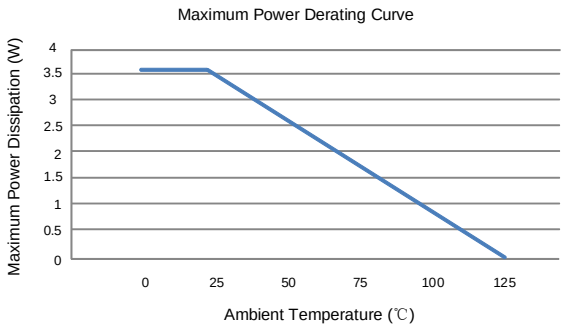
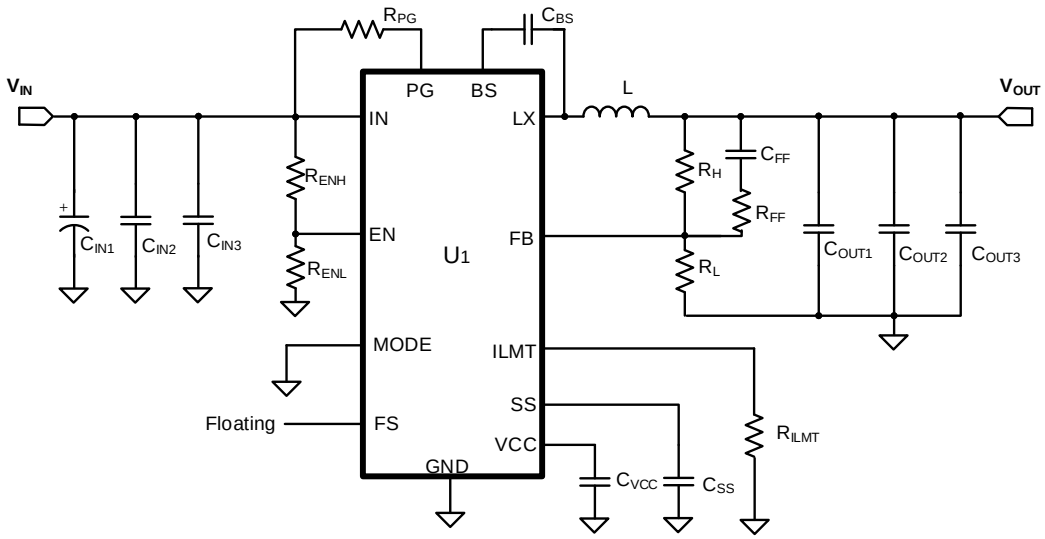


Figure 14. Maximum Power Dissipation

Application Schematic (V_{OUT}=5V)



BOM List

Designator	Description	Part Number	Manufacturer
C_{IN1}	47μF/50V Electrolytic Cap		
C_{IN2}	10μF/50V/X5R,1206	GRM31CR61H106KA12L	m μ Rata
C_{IN3}, C_{BS}	0.1μF/50V/X7R, 0603	GRM188R71H104KA93D	mμRata
C_{FF}	470pF/50V/C0G, 0603	GRM1885C1H471JA01D	mμRata
C_{OUT1}, C_{OUT2}, C_{OUT3}	22μF/16V/X5R, 1206	GRM31CR61C226ME15L	mμRata
C_{VCC}	4.7μF/16V/X5R, 0603	GRM185R61C475KE11D	mμRata
C_{SS}	47nF/50V, 0603	GRM188R71H473KA61D	mμRata
L	2.2μH/15A, inductor	PCMB104T-2R2MS	CYNTEC
R_{PG}, R_H	100kΩ, 1%, 0603		
R_L	13.7kΩ, 1%, 0603		
R_{FF}	1kΩ, 1%, 0603		
R_{ENH}	10kΩ, 1%, 0603		
R_{ENL}	1MΩ, 1%, 0603		
R_{ILMT}	300kΩ, 1%, 0603		

Recommended Components for Typical Applications

V_{OUT} (V)	R_H (kΩ)	R_L (kΩ)	C_{FF} (pF)	L/Part Number
1.2	100	100	220	1.0μH/PCMB104T-1R0MT
1.8	100	49.9	220	1.0μH/PCMB104T-1R0MT
3.3	100	22.1	470	1.5μH/PCMB104T-1R5MS
5.0	100	13.7	470	2.2μH/PCMB104T-2R2MS

Layout Design

Follow these PCB layout guidelines for optimal performance and thermal dissipation.

Input Capacitors: Place the input capacitor very near IN and GND, minimizing the loop formed by these connections. And the input capacitor should be connected to the IN and GND by wide copper plane. A 0.1μF input ceramic capacitor is recommended to reduce the input noise.

Output Capacitors: Guarantee the C_{OUT} negative sides are connected with GND pin by wide copper traces instead of vias, in order to achieve better accuracy and stability of output voltage.

VCC Capacitor: Place the VCC capacitor close to VCC using short, direct copper trace to one nearest GND pin (pin 17 and pin18).

Feedback Network: Place the feedback components (R_H, R_L, R_{FF} and C_{FF}) as close to FB pin as possible. Avoid routing the feedback line near LX, BS or other high frequency signal as it is noise sensitive. Make the feedback sampling point Kelvin connect with C_{OUT} rather than the inductor output terminal.

LX Connection: Keep LX area small to prevent excessive EMI, while providing wide copper traces to minimize parasitic resistance and inductance. Wide LX copper trace between pin 6 and pin 19, 20 should be adopted to improve efficiency.

BS Capacitor: Place the BS capacitor on the same layer as the device, keep the BS voltage path (BS, LX and C_{BS}) as short as possible.

Control Signals: It is not recommended to connect control signals and IN directly. A resistor in a range of 1kΩ to 1MΩ should be used if they are pulled high by IN.

GND Vias: Place adequate number of vias on the GND layer around the device for better thermal performance. The exposed GND pad should be connected by a larger copper area than its size, place four GND vias on it for heat dissipation.

PCB Board: A four-layer layout with 2-oz copper is strongly recommended to achieve better thermal performance. The top layer and bottom layer should place power IN and GND copper plane as wide as possible. Middle1 layer should place all GND layer for conducting heat and shielding middle2 layer signal line from top layer crosstalk. Place signal lines on middle2 layer instead of the other layers, so that the other layers' GND plane not be cut apart by these signal lines.

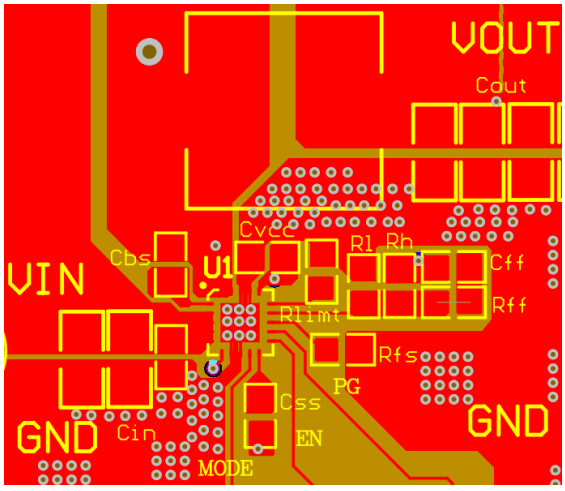
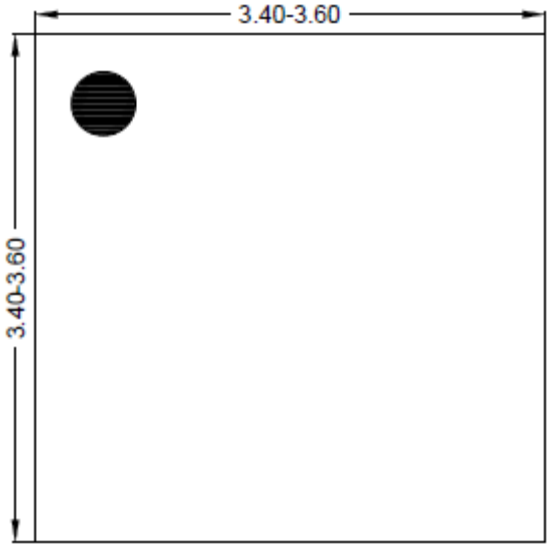
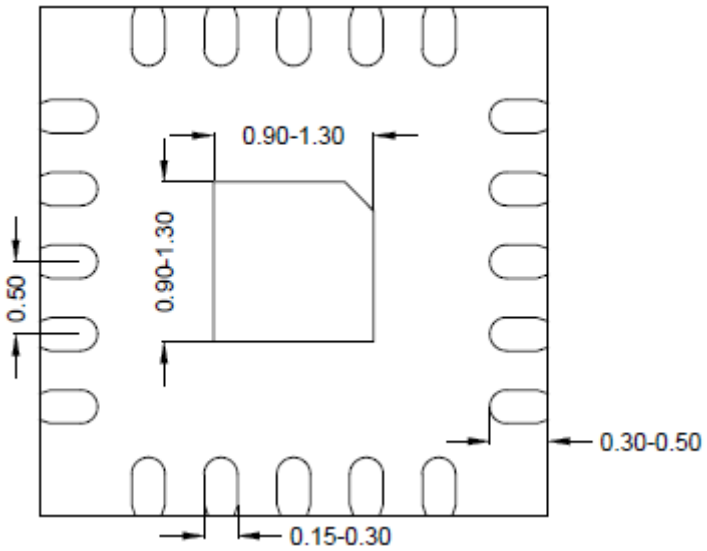


Figure 15. PCB Layout Suggestion

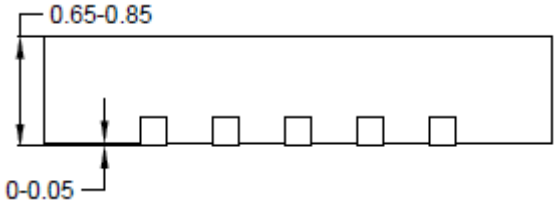
QFN3.5×3.5-20 Package Outline and PCB Layout Design



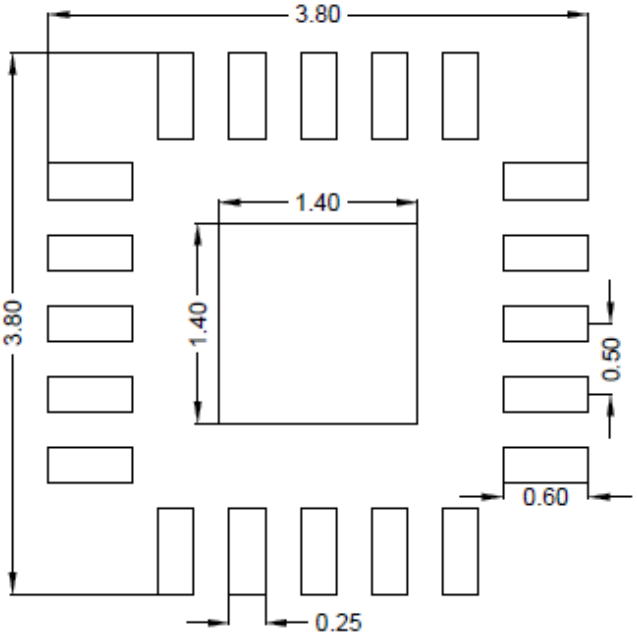
Top view



Bottom view



Side view

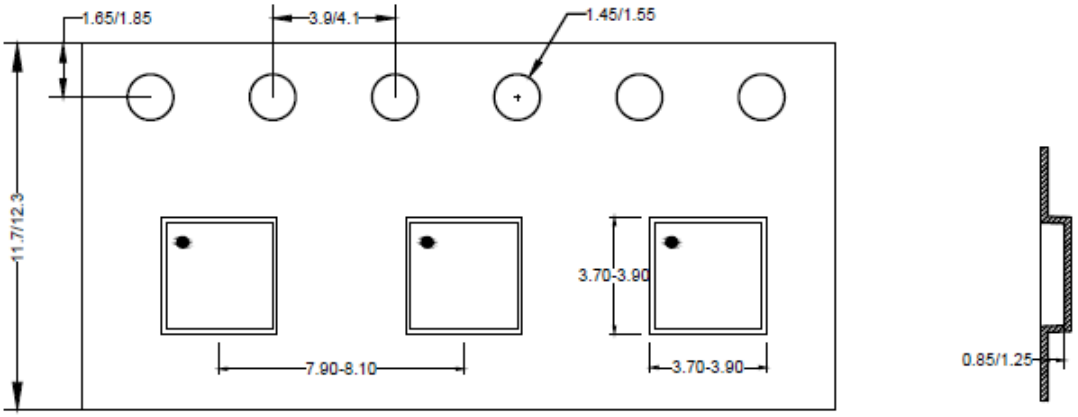


Recommended PCB layout (Reference only)

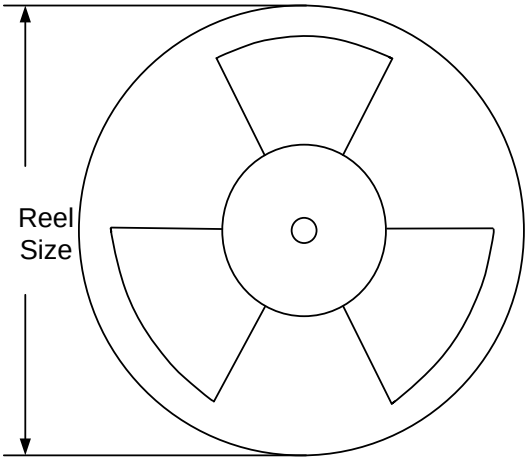
Note: *All dimensions are in millimeters and exclude mold flash and metal burr.*

Taping and Reel Specification

QFN3.5×3.5-20 taping orientation



Carrier Tape and Reel specification for packages



Package Type	Tape Width (mm)	Pocket Pitch (mm)	Reel Size (Inch)	Trailer Length (mm)	Leader Length (mm)	Qty per Reel
QFN3.5×3.5-20	12	8	13"	400	400	3000

Others: NA

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change
Dec.12, 2023	Revision 1.0	Language improvements for clarify
Nov.25, 2020	Revision 0.9	Initial Release

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