SY20826

5.5V/6A, Low $R_{DS(ON)}$ Dual-Channel Load Switch

General Description

The SY20826 is a dual-channel 6A load switch. Its integrated N-channel MOSFETs feature extremely low $R_{DS(ON)}$, helping to reduce power loss during normal operation. The capacitor programmable soft-start time controls the output voltage's slew rate at start-up independently on each channel, minimizing the inrush current. This device also offers independent enable controls for complex system sequencing. It integrates a discharge resistor to ensure quick output discharge when the switches are turned off.

The SY20826 is available in a compact DFN 3mm×2mm-14pin package which requires minimal space and provides improved thermal performance.

Features

- Dual-Channel 6A Load Switch
- Wide Input Voltage Range: 0.8V to 5.5V
- Low Bias Current:
  - 20μA Typical (Both Channels)
  - 18μA Typical (Single Channel)
- Extremely Low $R_{DS(ON)}$ for the Integrated MOSFET: 18mΩ (V_{BIAS}=5V)
- Programmable Soft-Start Time
- Compact Package: DFN3×2-14

Applications

- Notebook Tablet, or Net PCs
- Desktop PCs
- Servers
- Set Top Boxes
- E-Book or MIDs
- Smart TVs
- Routers
- Industrial PCs
- Solid-state Drives (SSD)

Typical Application

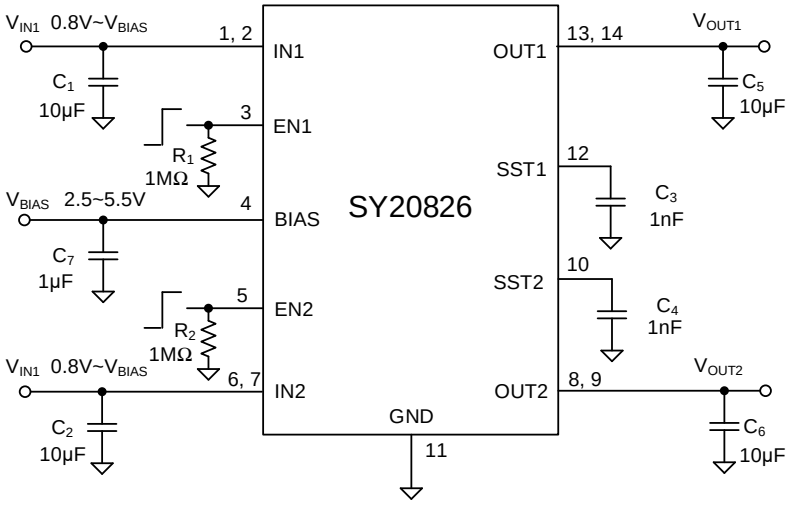


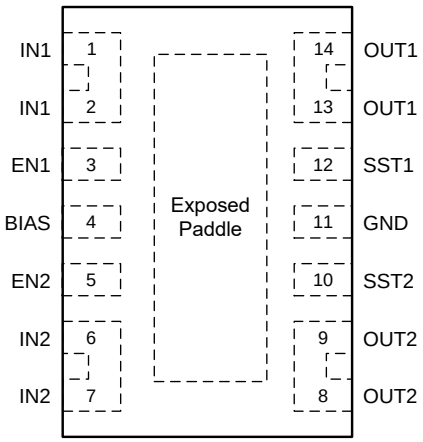
Figure 1. Schematic Diagram

Ordering Information

Ordering Number	Package Type	Top Mark
SY20826DUC	DFN3×2-14 RoHS Compliant and Halogen Free	**Raxyz**

Device code: Ra
x=year code, y=week code, z= lot number code

Pinout (Top View)



(DFN3×2-14)

Pin Name	Pin Number	Pin Description
IN1	1,2	Power input pin for channel 1.
EN1	3	Enable control input for channel 1. Pull HIGH to enable channel 1. Do not leave floating.
BIAS	4	Bias pin. Bias supply for overdriving the gate of the pass switch between input and output. The recommended BIAS voltage range is 2.5V to 5.5V.
EN2	5	Enable control input for channel 2. Pull HIGH to enable channel 2. Do not leave floating.
IN2	6,7	Power input pin for channel 2.
OUT2	8,9	Power output pin for channel 2.
SST2	10	Soft Start pin of channel 2. Connect a capacitor from this pin to the ground for slew rate programming. If not used in can be left floating.
GND	11	Ground pin.
SST1	12	Soft Start pin of channel 1. Connect a capacitor from this pin to the ground for slew rate programming. If not used in can be left floating.
OUT1	13,14	Power output pin for channel 1.
Thermal Pad	Exposed paddle	Thermal pad, tie to GND.

Block Diagram

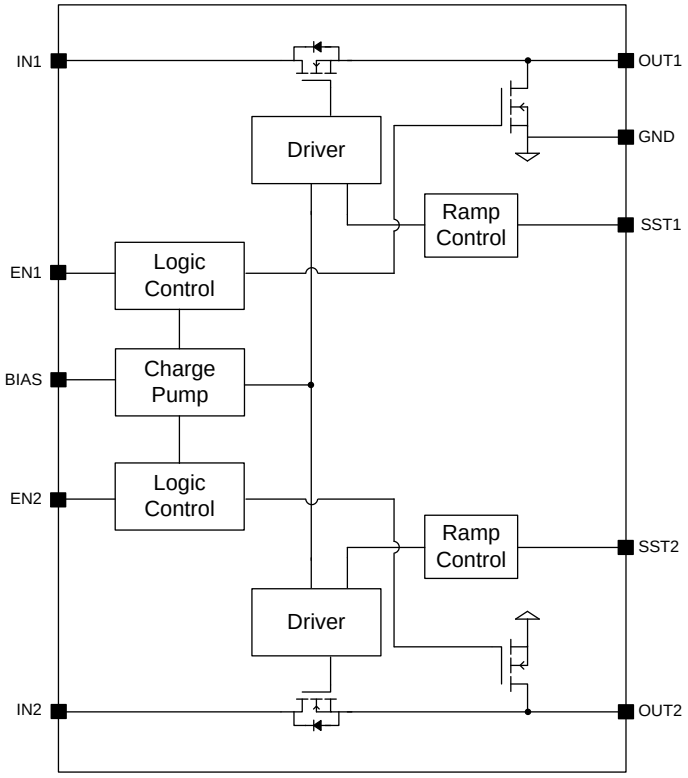


Figure 2. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
IN1, IN2, OUT1, OUT2	-0.3	6	V
SST1, SST2	-0.3	OUT+6	
EN1, EN2, BIAS	-0.3	6	
Lead Temperature (Soldering, 10s)		260	°C
Junction Temperature, Operating	-40	150	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	52.3	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	11.5	
P_D Power Dissipation T_A = 25°C	1.9	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
IN1, IN2, OUT1, OUT2	0.8	V_{BIAS}	V
EN1, EN2	0	V_{BIAS}	
BIAS	2.5	5.5	
Junction Temperature, Operating	-40	125	°C
Ambient Temperature	-40	85	

Electrical Characteristics

(V_{IN} =V_{BIAS}= 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions			Min	Typ	Max	Unit
Input Voltage Range	$V_{IN1,2}$				0.8		V_{BIAS}	V
BIAS Voltage Range	V_{BIAS}				2.5		5.5	V
BIAS Quiescent Current (Single channel)	$I_{Q\_BIAS\_1}$	V_{BIAS}= $V_{IN1,2}$=V_{EN1}=5V, V_{EN2}=0V,$I_{OUT1,2}$=0A				18		μA
		V_{BIAS}= $V_{IN1,2}$=V_{EN1}=2.5V, V_{EN2}=0V,$I_{OUT1,2}$=0A				7		
BIAS Quiescent Current (Both channels)	$I_{Q\_BIAS\_2}$	V_{BIAS}= $V_{IN1,2}$=$V_{EN1,2}$=5V, $I_{OUT1,2}$=0A				20	30	μA
		V_{BIAS}= $V_{IN1,2}$=$V_{EN1,2}$=2.5V, $I_{OUT1,2}$=0A				8	15	
BIAS Shutdown Current	I_{SHD_BIAS}	$V_{EN1,2}$=0V,$V_{OUT1,2}$=0V					2	μA
Input Shutdown Current (per channel)	I_{SHD_IN}	$V_{EN1,2}$=0V, $V_{OUT1,2}$=0V	V_{BIAS}=5V	V_{IN}=5V		0.5	8	μA
				V_{IN}=3.3V		0.1	3	
				V_{IN}=1.8V		0.07	2	
				V_{IN}=0.8V		0.04	1	
			V_{BIAS}=2.5V	V_{IN}=2.5V		0.13	3	
				V_{IN}=1.8V		0.07	2	
				V_{IN}=1.2V		0.05	2	
				V_{IN}=0.8V		0.04	1	
Integrate FET RON (per channel)	$R_{DS(ON)}$	V_{BIAS}=5V, V_{IN}=0.8V to 5V, I_{OUT}=200mA, T_A=25°C				18	25	mΩ
		V_{BIAS}=5V, V_{IN}=0.8V to 5V, I_{OUT}=200mA, -40°C <T_A<85°C				18	27	
		V_{BIAS}=3.3V,V_{IN}=0.8V to 3.3V, I_{OUT}=200mA, T_A=25°C				20	27	
		V_{BIAS}=3.3V,V_{IN}=0.8V to 3.3V, I_{OUT}=200mA, -40°C <T_A<85°C				20	30	
EN Turn-on Threshold	V_{EN_ON}				1.2			V
EN Turn-off Threshold	V_{EN_OFF}						0.4	V
Output Discharge Resistor	R_{DIS}					190	270	Ω
Output Voltage Rise Time	t_{RISE}	R_L=10Ω, C_L=0.1μF, C_{SST}=1nF, V_{EN}=5V	V_{IN}= V_{BIAS} =5V			1730		μs
			V_{IN}= 0.8V,V_{BIAS}=5V			360		
			V_{IN}= V_{BIAS} =2.5V			2200		
			V_{IN}=0.8V,V_{BIAS}=2.5V			815		
Output Voltage Fall Time	t_{FALL}	R_L=10Ω, C_L=0.1μF, C_{SST}=1nF, V_{EN}=5V	V_{IN}= V_{BIAS} =5V			2		μs
			V_{IN}= 0.8V,V_{BIAS}=5V			2		
			V_{IN}= V_{BIAS} =2.5V			2		
			V_{IN}=0.8V,V_{BIAS}=2.5V			2		
Turn on delay Time	t_{D_ON}	R_L=10Ω, C_L=0.1μF, C_{SST}=1nF, V_{EN}=5V	V_{IN}= V_{BIAS} =5V			490		μs
			V_{IN}= 0.8V,V_{BIAS}=5V			325		
			V_{IN}= V_{BIAS} =2.5V			915		
			V_{IN}=0.8V,V_{BIAS}=2.5V			745		
Turn off delay Time	t_{D_OFF}	R_L=10Ω, C_L=0.1μF, C_{SST}=1nF, V_{EN}=5V	V_{IN}= V_{BIAS} =5V			6		μs
			V_{IN}= 0.8V,V_{BIAS}=5V			6		
			V_{IN}= V_{BIAS} =2.5V			15		
			V_{IN}=0.8V,V_{BIAS}=2.5V			15		

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. The device is mounted on a 2x2 FR-4 substrate PCB featuring 2oz copper. It includes the minimum recommended pad on the top layer, along with thermal vias connecting to the ground plane on the bottom layer. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single-layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. The exposed pad of the DFN3×2-14 package is the case position for θ_{JC} measurement.

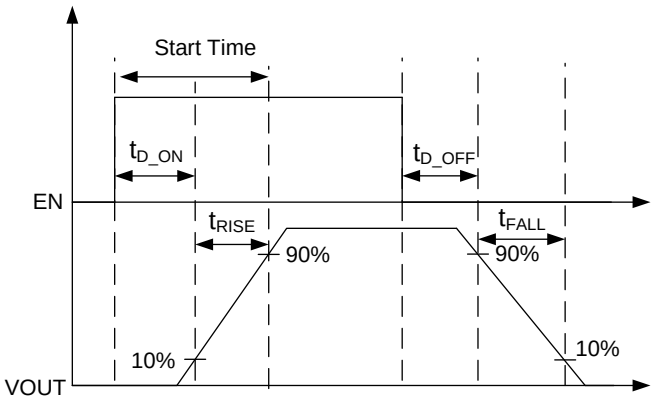
Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4. Recommended Soft-Start Time Program Table:

Condition: RISE TIME (μs) 10% - 90%, C_L = 0.1μF, C_{IN} = 1μF, R_L = 10Ω, TYPICAL VALUES at 25°C, V_{BIAS} = 5V, 25V X7R 10% CERAMIC CAP, under different V_{IN}.					
SST Cap (pF)	5V	3.3V	1.8V	1.5V	1.2V
0	210	154	104	93	81
220	555	385	231	209	178
470	1022	680	406	342	272
1000	1764	1208	714	616	488
2200	3808	2536	1450	1260	1024
4700	8200	5568	3192	2768	2296

Recommended Formula for C_{SST} & Soft-Start Slew Rate Calculation:

$$\frac{dV}{dt} = \frac{2.56}{C_{SST}(pF) + 145(pF)} (V/us),$$



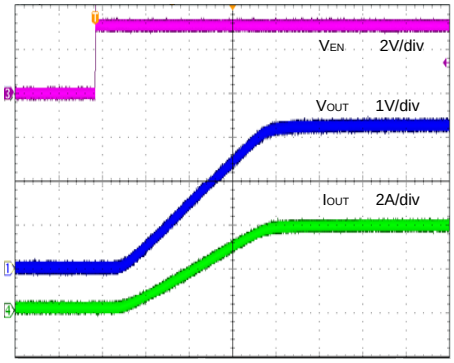
A capacitor to GND on the SSTx pins sets the slew rate for each channel. To ensure desired performance, a capacitor with a minimum voltage rating of 25V should be used on the SSTx pin to reduce voltage derating.

(The equation accounts for 10% to 90% of measurement on VOUT).

Typical Performance Characteristics

Startup from Enable

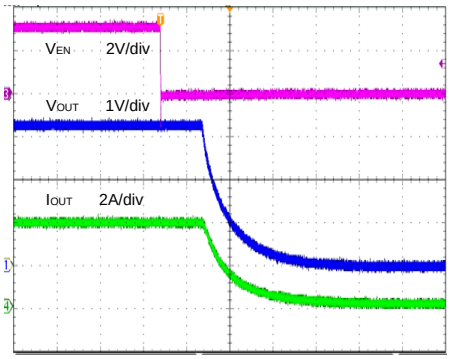
(VBIAS=VIN=3.3V, Io=4A)



Time (800μs/div)

Shutdown from Enable

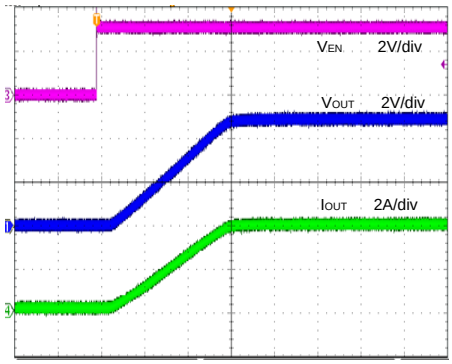
(VBIAS=VIN=3.3V, Io=4A)



Time (10μs/div)

Startup from Enable

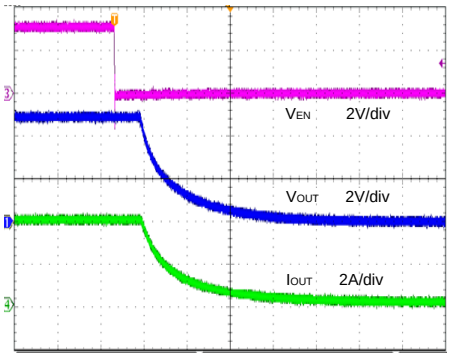
(VBIAS=VIN=5V, Io=4A)



Time (800μs/div)

Shutdown from Enable

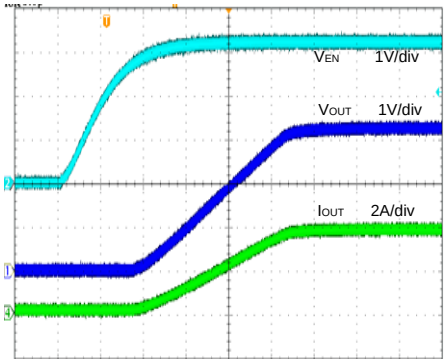
(VBIAS=VIN=3.3V, Io=4A)



Time (10μs/div)

Startup from BIAS

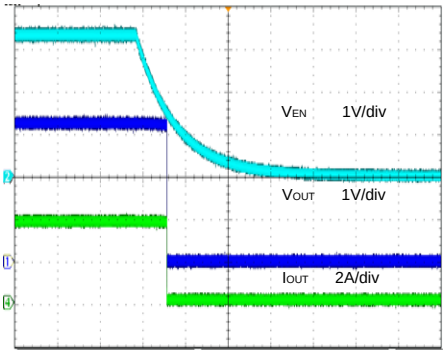
(VBIAS=VIN=3.3V, Io=4A)



Time (800μs/div)

Shutdown from BIAS

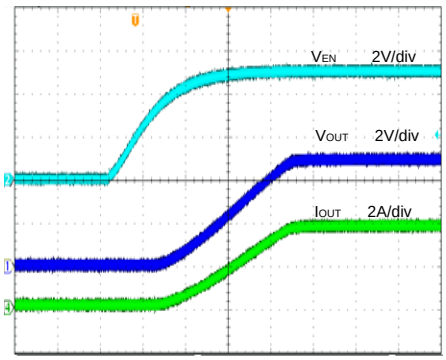
(VBIAS=VIN=3.3V, Io=4A)



Time (100ms/div)

Startup from BIAS

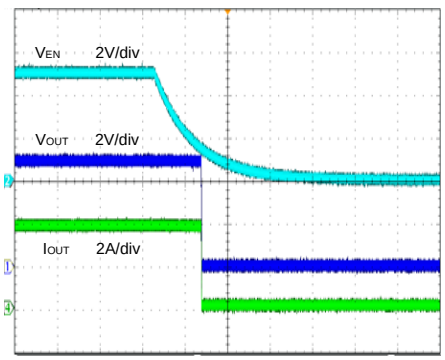
(VBIAS=VIN=5V, Io=4A)



Time (800μs/div)

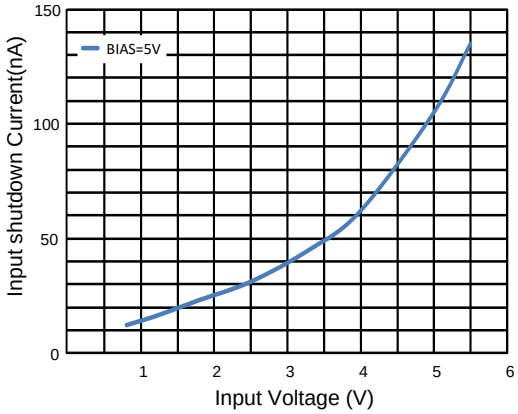
Shutdown from BIAS

(VBIAS=VIN=5V, Io=4A)

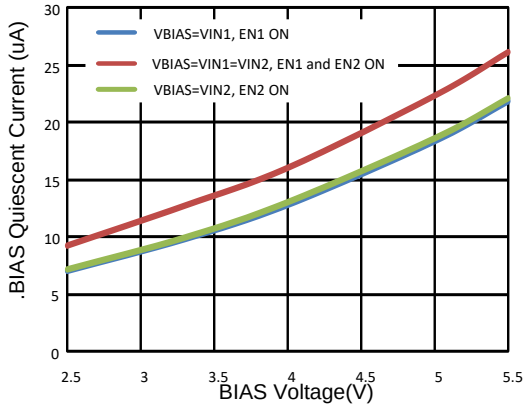


Time (100ms/div)

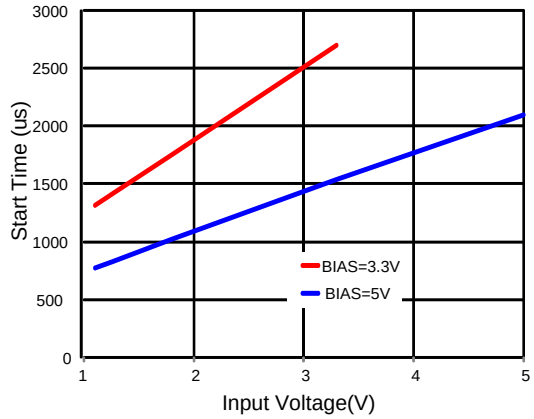
Input shutdown Current(per Channel) vs. Input Voltage



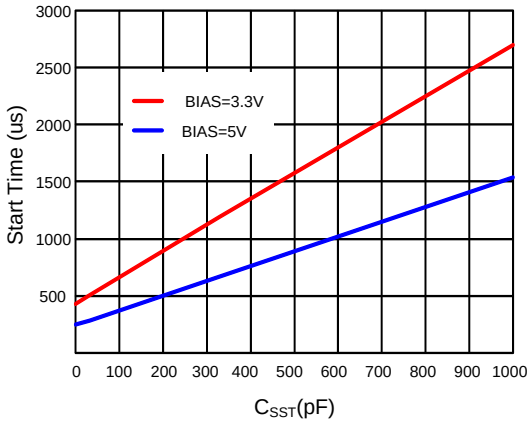
BIAS Quiescent Current vs. BIAS Voltage



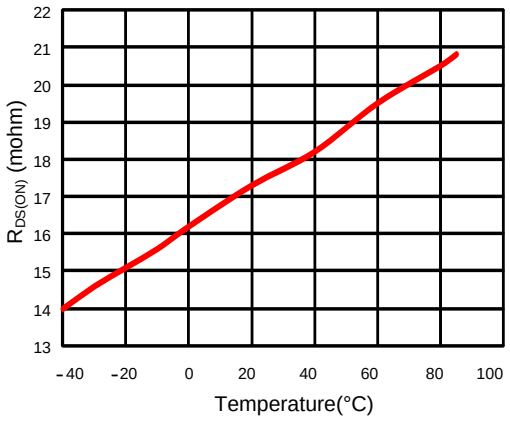
Start Time Vs. Input Voltage (C_{SST}=NULL)



Start Time vs. CT (V_{IN}=3.3V)



Temperature vs. $R_{DS(ON)}$



Application Information

The SY20826 is a dual-channel 6A load switch. The extremely low $R_{DS(ON)}$ of the integrated MOSFETs helps to reduce power loss during normal operation. The programmable soft-start time controls the slew rate of the output voltage during start-up and minimizes the inrush current. The switch offers independent enable control for complex system sequencing. Additionally, it integrates a discharge resistor to swiftly discharge the output when the switch is turned off.

The SY20826 is available in a compact DFN3×2-14 package which requires minimal space and provides better thermal performance.

EN ON/OFF Control:

The EN pins control the state of the switches. Asserting EN high enables the switch. EN is active-high and has a low threshold, making it capable of interfacing with low-voltage signals. This pin cannot be left floating and must be tied either high or low for proper functionality.

Input Capacitor:

In most applications, it is recommended to bypass INx to GND using a 10μF ceramic capacitor, placed as close as possible to the device. If the power source exhibits significant inductance due to long lead lengths, the input capacitor helps to clamp any overshoot caused by the device's tank circuit.

V_{IN} and V_{BIAS} Voltage Range:

For optimal R_{ON} performance, make sure $V_{IN} \le V_{BIAS}$.
The device will still be functional if $V_{IN} > V_{BIAS}$ but the R_{ON} may exceed the typical value listed in Electrical Characteristics.

Soft-Start Time Program:

Connect a capacitor from SST pins to GND to control the slew rate of the output voltage at power-on. This pin can be left floating to obtain a predetermined slew rate (minimum T_{SST}) on the output. Use the following equation to determine the soft-start time:

$$SR_{OUT} = \frac{2.56}{C_{SST}(pF)+145(pF)} (v/\mu s)$$

$$t_{RISE} = 0.8 \times \frac{V_{IN}}{SR_{OUT}} (\mu s)$$

PCB Layout Guide:

For best performance of the SY20826, the following guidelines must be strictly followed:

1. Keep all power traces as short and wide as possible. It's recommended to use a 2-layer or 4-layer board for thermal performance and better capability of current flow.
2. It is recommended to place a minimum of 6 vias around each power pin to efficiently distribute current across different layers of the PCB.
3. Place the input/output and BIAS capacitors close to the device for better transient performance.

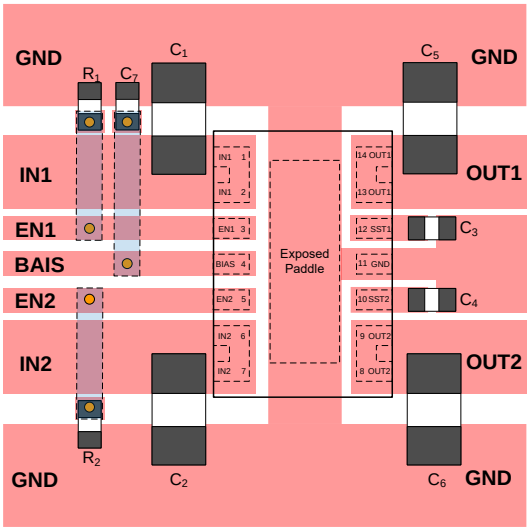
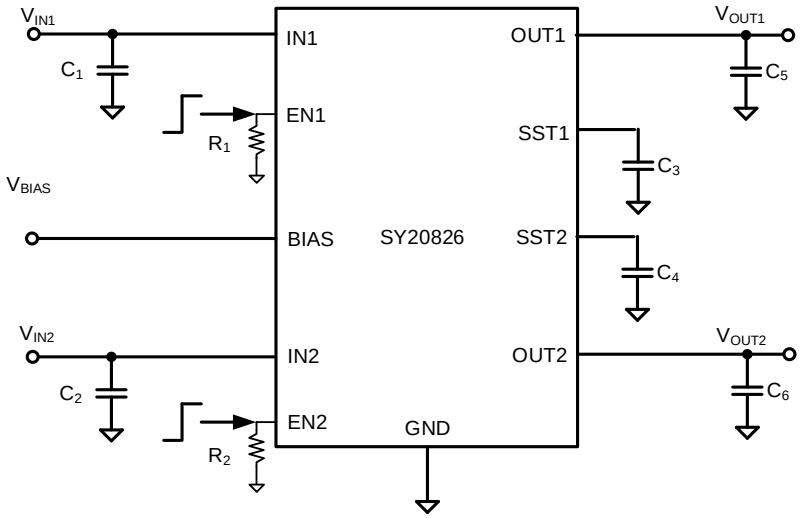


Figure 3. PCB Layout Suggestion

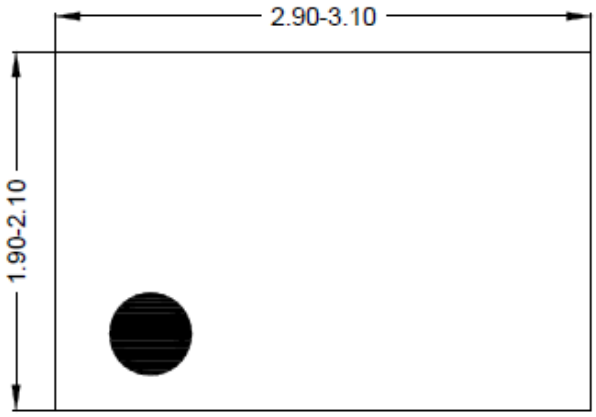
Schematic



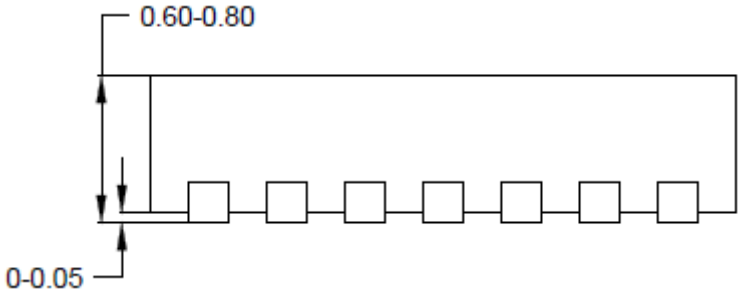
BOM List

Reference Designator	Description	Part Number	Manufacturer
C_1	10μF/10V, 0805, X5R	GRM21BR71A106K	Murata
C_2	10μF/10V, 0805, X5R	GRM21BR71A106K	Murata
C_3	1nF/50V, 0603, X5R	GRM1885C1H102J	Murata
C_4	1nF/50V, 0603, X5R	GRM1885C1H102J	Murata
C_5	10μF/10V, 0805, X5R	C1608X5R1E105K	Murata
C_6	10μF/10V, 0805, X5R	C1608X5R1E105K	Murata
R_1	1MΩ, 0603		
R_2	1MΩ, 0603		

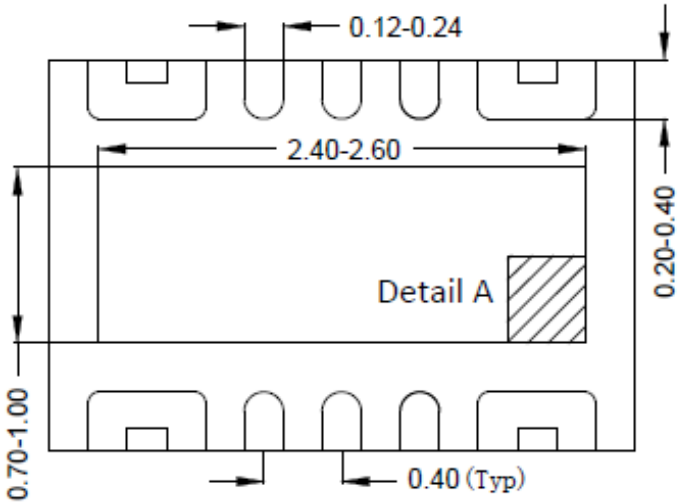
DFN3×2-14 Package Outline Drawing

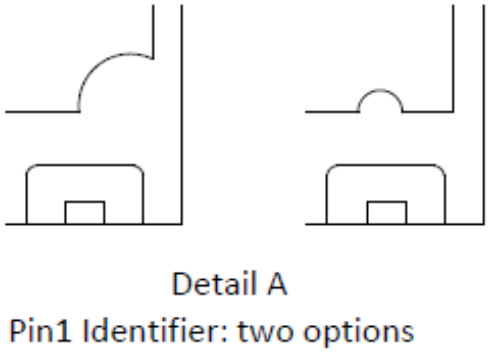


Top View

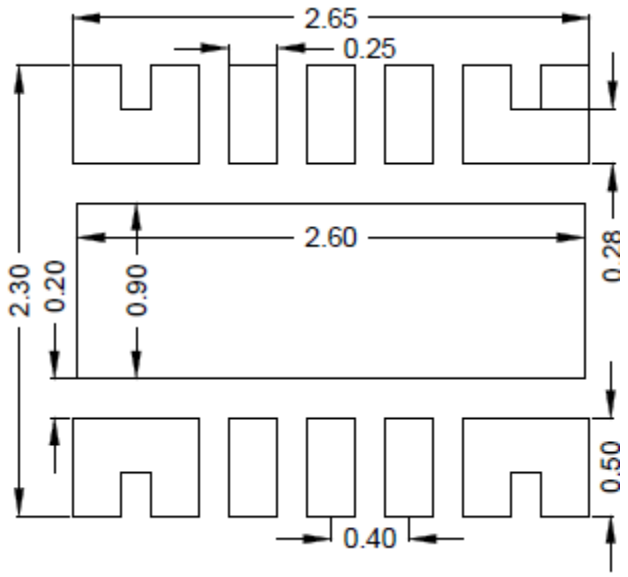


Side View





Bottom View

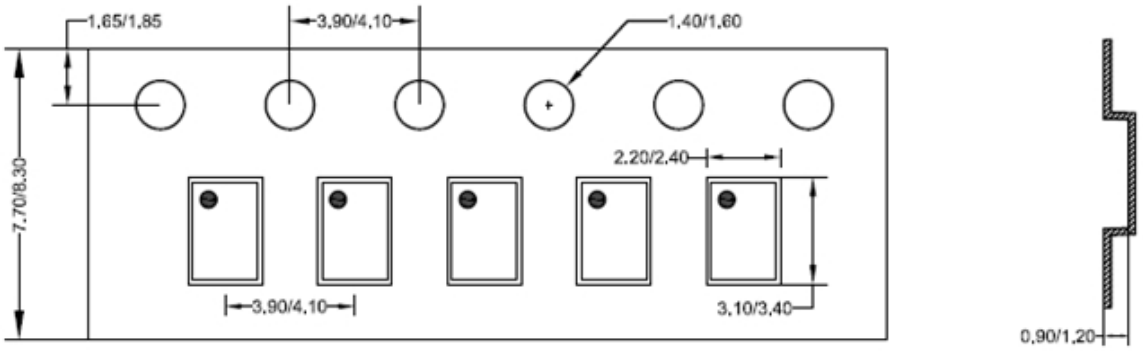


Recommended PCB Layout
(Reference Only)

Note: All dimensions are in millimeters and exclude mold flash and metal burr.

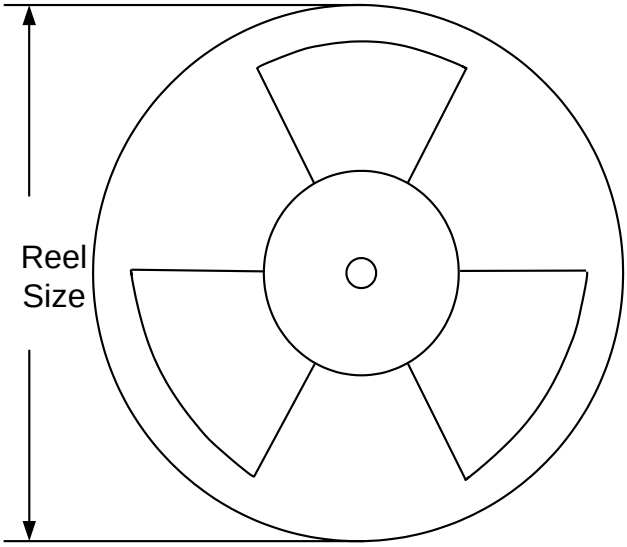
Taping & Reel Specification

DFN3×2 Taping Orientation



Feeding direction ⟶

Carrier Tape & Reel Specification for Packages



Package type	Tape width (mm)	Pocket pitch (mm)	Reel size (Inch)	Trailer length (mm)	Leader length (mm)	Qty per reel (pcs)
DFN3×2-14	8	4	7"	400	160	3000

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change
Jan.12, 2024	Revision 1.0	Language improvements for clarity.
Oct.28, 2021	Revision 0.9A	Update the taping spec (Pin 1 is on the upper left.)
Jan.23, 2018	Revision 0.9	Initial Release

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