SY20805

High-Current Overvoltage Protection Switch With Integrated Reverse Blocking MOSFETs

General Description

The SY20805 is an overvoltage protection switch with high current capability used for preventing damage to the downstream systems with low voltage ratings. Programmable OVP can be configured using a simple external resistor divider. It operates with a wide input voltage range from 2.5V to 30V.

An integrated reverse blocking FET with 20V rating prevents the leakage current from the output to the input when the input power supply is removed, but the output is not discharged. The low power path resistance R_{PWPT} helps reduce power loss during normal operation. The enable control can be used for turning off the power path. A precision current monitor output provides a voltage proportional with the current flowing through the device. The SY20805 integrates over-temperature protection shutdown and auto-recovery with hysteresis to protect against over-temperature events.

The SY20805 is available in a compact CSP1.73×1.73-12 package.

Features

- Input Voltage Range: 2.5V to 30V
- 20V Integrated Reverse Blocking FET Rating
- Extremely Low Power Path Resistance R_{PWPT}
  - R_{PWPT}=53mΩ (Typical)
- Programmable OVP Through External Resistor Divider, ±3% Accuracy (max)
- Internal Soft-Start to Prevent In-Rush Current
- Thermal Shutdown Protection and Auto-Recovery
- Current Indicator with ±5% Accuracy
- RoHS Compliant and Halogen Free
- Compact Package: CSP-12 (1.73mm×1.73mm)

Applications

- Smartphones
- Tablet PCs
- Mobile Devices

Typical Application

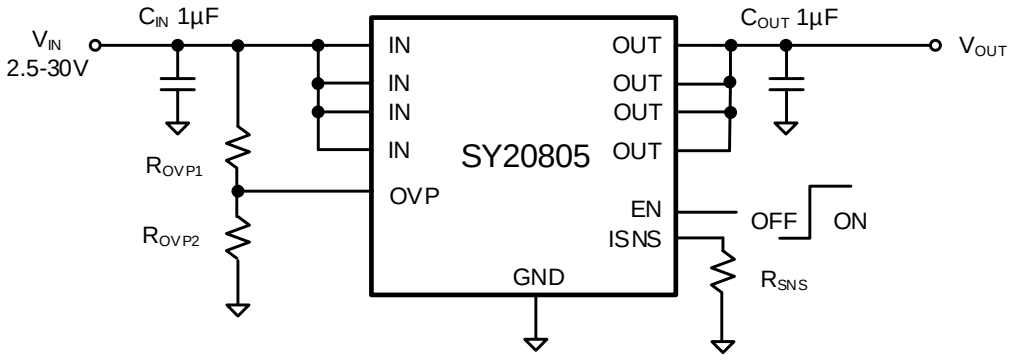


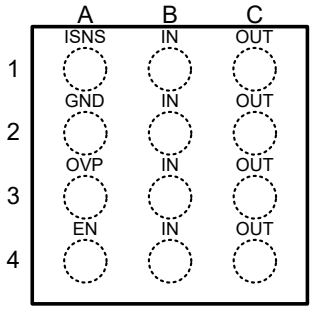
Figure 1. Schematic Diagram

Ordering Information

Ordering Part Number	Package Type	Top Mark
SY20805PLC	CSP1.73×1.73-12 RoHS Compliant and Halogen Free	**ZQ*xyz***

x=year code, y=week code, z= lot number code

Pinout (top view)



Pin Name	Pin Number	Pin Description
IN	B1,B2,B3,B4	Power input pin. Connect the IN pins together. Decouple high frequency noise by connecting at least a 0.1μF MLCC to ground.
OUT	C1,C2,C3,C4	Output voltage pin. Connect the OUT pins together for normal operation.
ISNS	A1	Current indicator pin. Connect a resister R_{SNS} from this pin to ground. The current flow is mirrored internally to charge R_{SNS} for the indication. The ratio of power current to mirrored current is 2.5k. The voltage on the ISNS pin equals to $V_{ISNS}=(I_{OUT}/2.5k)\times R_{SNS}$.
EN	A4	EN control pin. High logic enables all the internal circuit; low logic disables the internal energy flow path.
OVP	A3	External OVP program pin. Connect resistor divider to this pin to program the OVP threshold. The internal reference is at 1.26V. Pull down this pin to ground to disable external program function.
GND	A2	Power ground pin.

Block Diagram

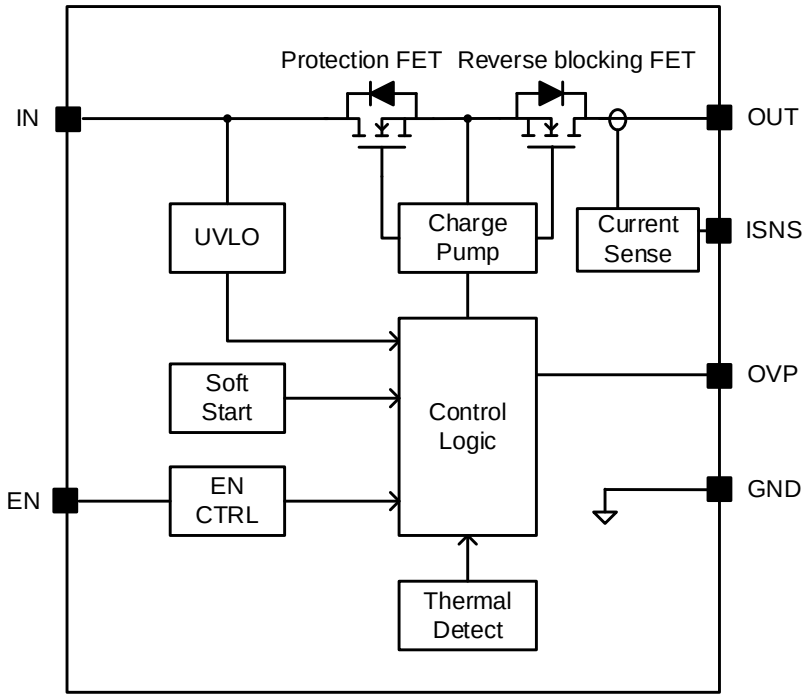


Figure 2. Block Diagram

Absolute Maximum Ratings (Note 1)

IN, EN, OVP ---------- 30V
OUT ---------- 20V
ISNS ---------- 6V
Continues IN, OUT Current ---------- 3A
Peak IN, OUT Current (10ms) ---------- 5A
Power Dissipation, P_D @ T_A = 25°C CSP, ---------- 1.67 W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 60 °C/W
θ_{JC} ---------- 7 °C/W
Junction Temperature Range ---------- 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions (Note 3)

IN, EN, OVP ---------- less than 30V
OUT ---------- less than 20V
ISNS ---------- less than 6V
Continues IN, OUT Current ---------- less than 3A
Peak IN, OUT Current (10ms) ---------- less than 5A
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{IN} = 2.5V to 30V, R_{ISNS}=1k, C_{IN}=1μF, C_{OUT}=1μF, TA = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.5		30	V
Input UVLO Threshold	V_{UVLO}				2.4	V
UVLO Hysteresis	V_{HYS}			0.1		V
Reverse Blocking Range	V_{RB}				20	V
Bias Current	I_{BIAS}	V_{IN}=5V		100		μA
Reverse Blocking Current	I_{RB}	V_{IN}=0V, V_{OUT}=16V, EN=0V		2	5	μA
Shutdown Current	I_{SD}	V_{IN}=5V, EN=0V		6	10	μA
		V_{IN}=30V, EN=0V		9	15	μA
Enable Threshold	V_{EN}	Rising	1.2			V
		Falling			0.5	V
OVP Program Threshold	V_{OVP}		1.22	1.26	1.30	V
Resistance of Power Path	R_{PWPT}	V_{IN}=5V, I_{OUT}=200mA, from IN to OUT	30	53	70	mΩ
Current Indicator Accuracy	V_{ISNS}	I_{OUT}=0.5A, R_{SNS}=1k	186	200	214	mV
		I_{OUT}=1.0A, R_{SNS}=1k	380	400	420	mV
Maximum Current Capability (Note 4)	I_{MAX}			5		A
Output Load Capacitance	C_{OUT}	V_{IN}=5V			1000	μF
Deglitch Time	t_{DG}	Time from 2.5V<V_{IN}<V_{OVP} to V_{OUT}=10% of V_{IN}	6	11	16	ms
Switch Turn-on Time	t_{ON}	V_{IN}=5V, V_{OUT}=10% of V_{IN} to 90% V_{IN}	0.7	1.2	1.7	ms
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			20		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single-layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

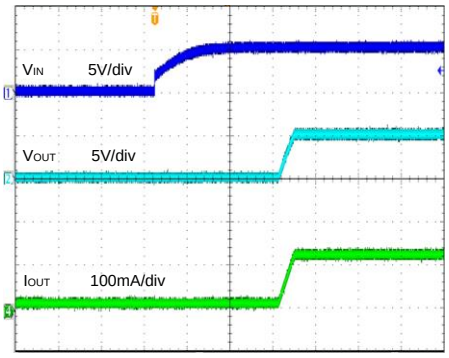
Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: These characteristics are design-guaranteed, not test items.

Typical Operating Characteristics

Power-up Response

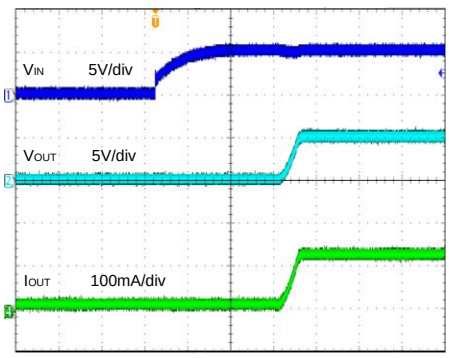
(V_{IN}=0V→ 5.0V,C_{OUT}=100μF,R_L=40Ω)



Time (4ms/div)

Power-up Response

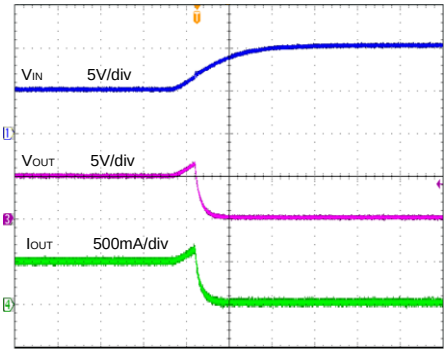
(V_{IN}=0V→ 5.0V,C_{OUT}=1000μF,R_L=40Ω)



Time (4ms/div)

Overvoltage Fault Response

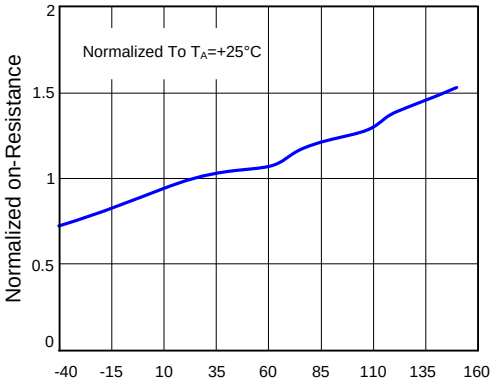
(V_{IN}=5.0V→ 10.0V,V_{OVP}=6.4V)



Time (800μs/div)

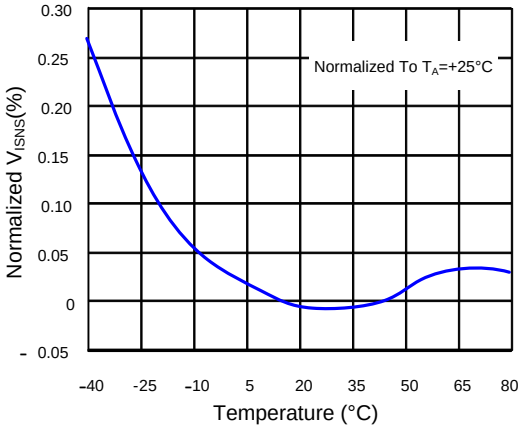
Normalized R_{ON} vs. Temperature

(V_{IN}=5.0V,R_L=100Ω)



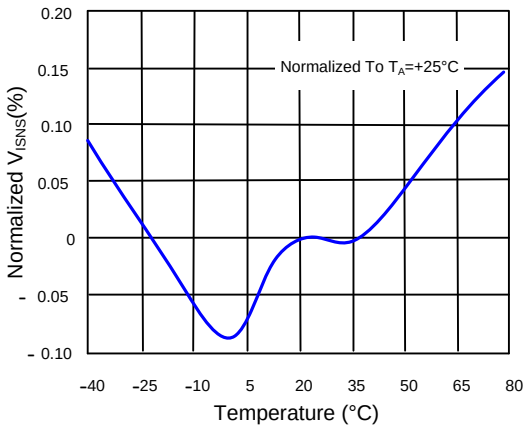
Normalized V_{ISNS} vs. Temperature

(V_{IN}=5V,R=2.5kΩ,I=3A)

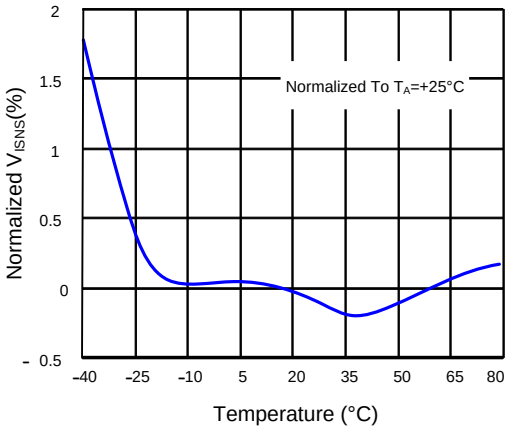


Normalized V_{ISNS} vs. Temperature

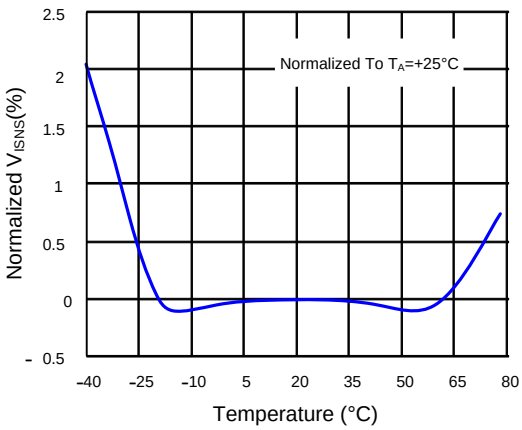
(V_{IN}=5V,R=1kΩ,I=3A)



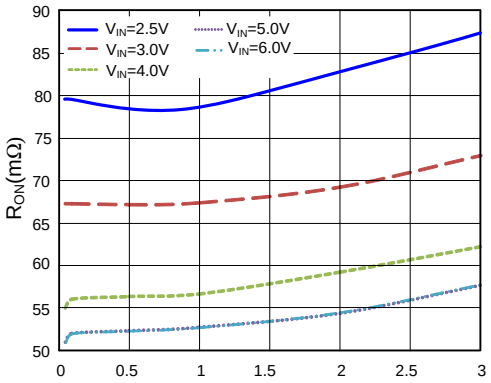
Normalized V_{ISNS} vs. Temperature
(V_{IN}=5V,R=2.5kΩ,I=1A)



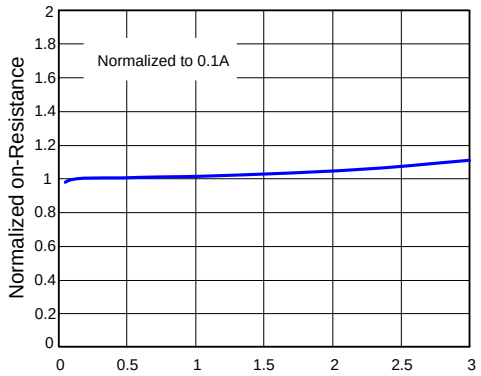
Normalized V_{ISNS} vs. Temperature
(V_{IN}=5V,R=1kΩ,I=1A)



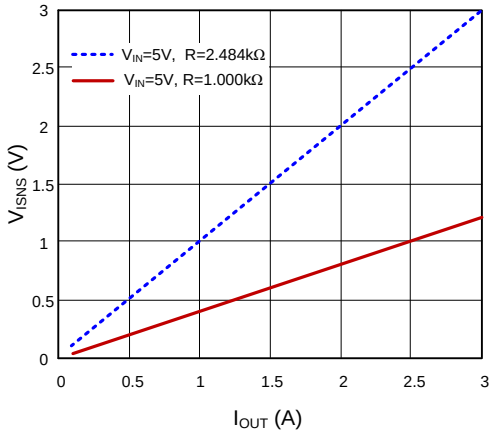
R_{ON} vs. Output Current



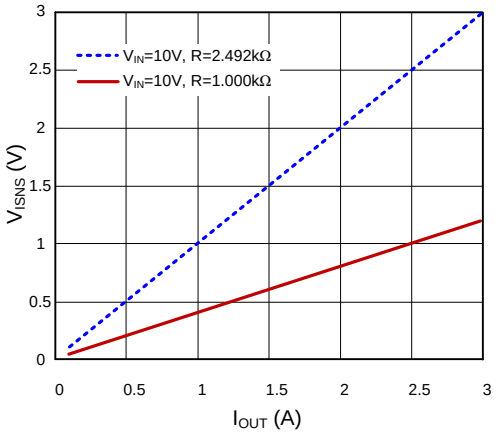
Normalized R_{ON} vs. Output Current
(V_{IN}=5.0V)



Current Indicator



Current Indicator



General Operation Description

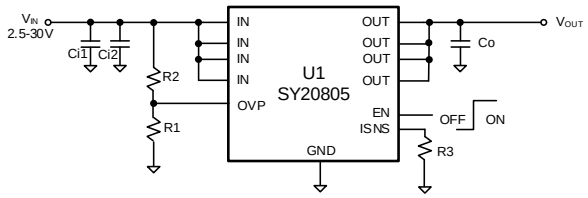
The SY20805 is an overvoltage protection switch with high current capability used to prevent damage to the downstream circuits with low voltage ratings. It can be used in smartphone applications, PCs, tablets, and other mobile devices.

The SY20805 operates with a wide input voltage range from 2.5V to 30V. The OVP threshold cana be configured using an external resistor-divider. An integrated, reverse blocking, 20V rated FET prevents the leakage current from the output to the input when the input power supply is removed or shorted suddenly, but the output is not discharged. The extremely low power path resistance R_{PWPT} helps reduce power loss during the normal operation.

The enable control can be used for turning off the power path or to enable a flexible startup sequence. A precision current monitor output provides a voltage proportional with the current flowing through the device.

The SY20805 integrates a over-temperature protection shutdown and auto-recovery with hysteresis to protect against over temperature events. It has a default setting of 5A, (8A max) over-current protection, and auto-recovery once over the overload condition is removed. Each auto-recovery process is composed of deglitch time (t_{DG}) and switch turn-on time (t_{ON}).

Application Schematic



BOM List

Designator	Description	Part Number
U1		SY20805PLC
Ci1	CHIP CAP X7R 10μF +/-10% 50V 0603	
Ci2	CHIP CAP X7R 1μF +/-10% 50V 1206	
Co	CHIP CAP X7R 10μF +/-10% 50V 0603	
R1	22.1k,+/-1%,0603	
R2	88.7k,+/-1%,0603	
R3	1k,+/-1%,0603	

Over Voltage Protection

The internal OVP threshold of SY20805 is 1.26V with approximately 20mV hysteresis. When the voltage on the OVP pin rises above the OVP threshold, the OVP will be triggered and the internal power switch will be turned off. When the voltage on the OVP pin falls below the OVP threshold, minus the voltage hysteresis, the OVP will recover, and the power switch will be turned on again. Selecting the external resistor-divider values, R_{OVP1} and R_{OVP2}, can program the input overvoltage level, as shown in equation (1).

$$V_{INOVP}= (R_{OVP1}+R_{OVP2})\times 1.26/R_{OVP2} \quad (1)$$

Leakage Current Reverse Blocking

The SY20805 integrates back-to-back power MOSFETs to enable reverse current blocking. The reverse blocking function is implemented by switching off the internal back-to-back MOSFETs when the reverse voltage from OUT to IN exceeds 80mV. The SY20805 can block the reverse energy flowing from OUT to IN when the input power source is removed, or the input is shorted to ground. It can protect the downstream battery powered system and extend the battery life. When the voltage from IN to OUT exceeds 50mV, the reverse blocking is disabled and the power MOSFETs are turned on.

High Accuracy Current Indicator

A precision current monitor output provides a voltage proportional with the current flowing through the device at the ISNS pin. The internal current source is configured to be proportional to the current flowing through the power switch. Connect a resistor R_{SNS} from ISNS to GND. The voltage at the ISNS pin can be estimated as shown in equation (2). The voltage rating of this pin is 6V and the SY20805 has an internal default current limit of approximately 5A. It is recommended to use a R_{SNS} resistor value lower than the value calculated using the equation (3). When the current exceeds the default current limit, the power FET will switch off and restart automatically. The rated accuracy of 5% is achieved at output currents above 1A. A better than 7% accuracy is achieved at 0.5A output current, as shown in Figure 3. and Figure 4. respectively.

$$V_{ISNS}=(I_{OUT}/2.5k)\times R_{SNS} \quad (2)$$

$$R_{SNS}<(V_{ISNS\_MAX}/I_{MAX})\times 2.5k \quad (3)$$

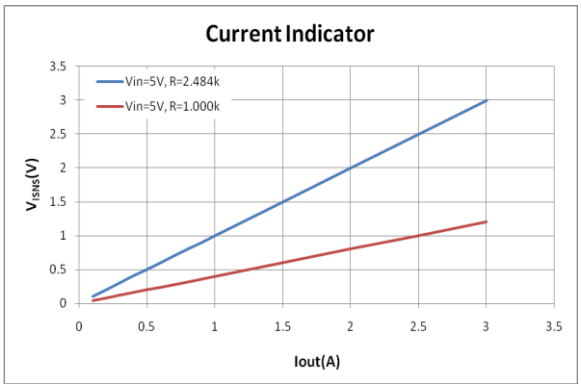


Fig. 3 Relationship between V_{ISNS} and I_{OUT} with different R_{SNS}

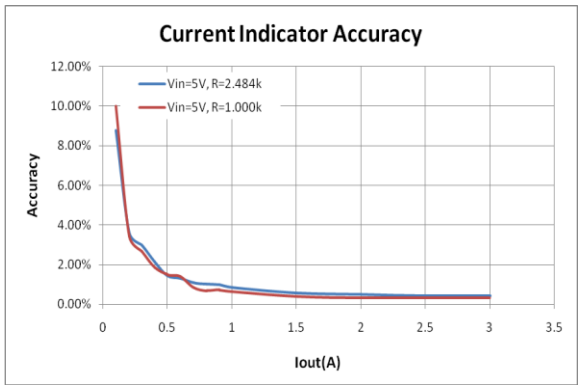
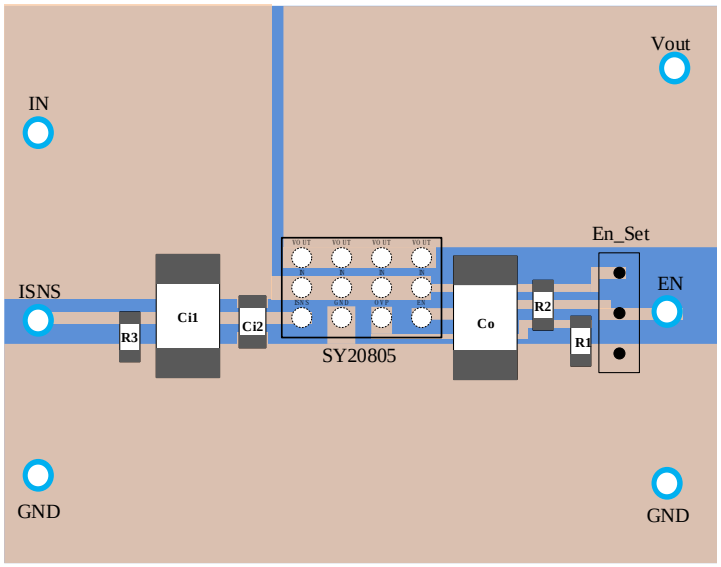
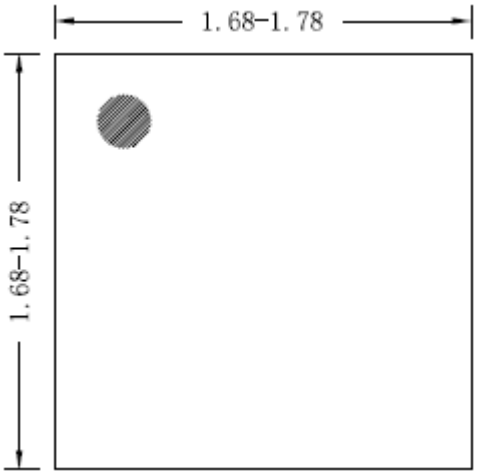


Fig.4 Accuracy of current indicator with different R_{SNS}

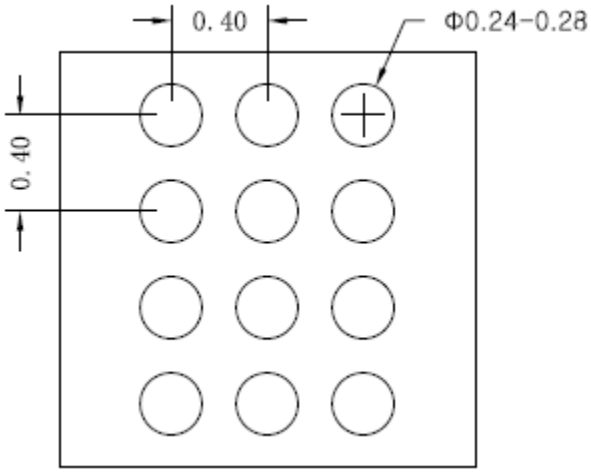
PCB Layout Suggestion



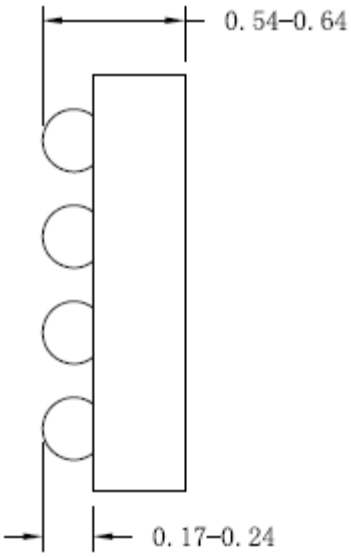
CSP1.73×1.73-12 Outline Drawing



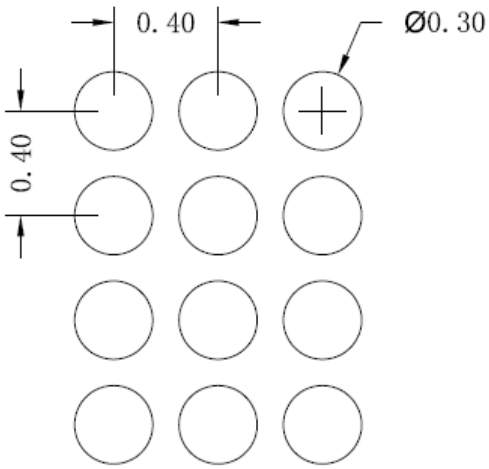
Top View



Bottom View



Side View

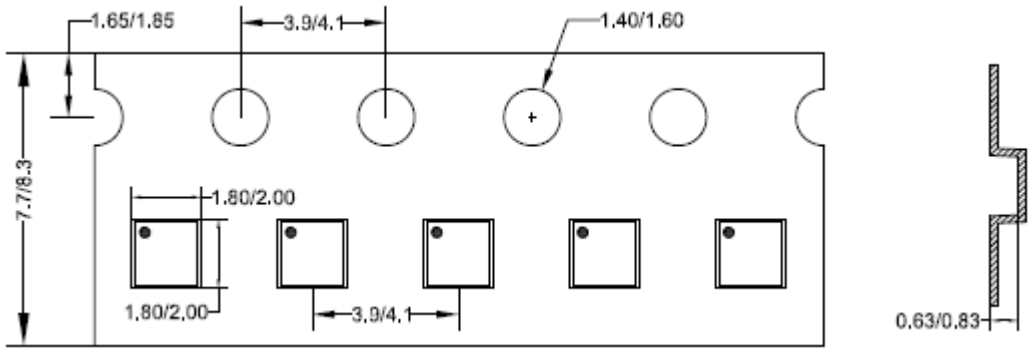


Recommended PCB layout

Note: All dimensions are in millimeters and exclude mold flash and metal burr.

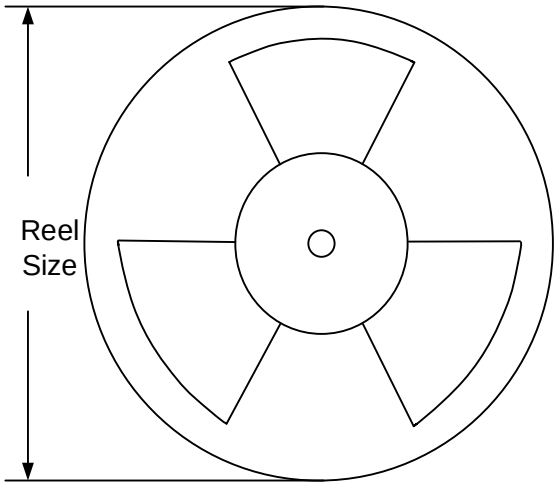
Taping & Reel Specification

CSP1.73×1.73 Taping Orientation



Feeding direction

Carrier Tape & Reel Specification for Packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
CSP1.73×1.73	8	4	7"	400	400	3000

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