SY20817A

2.5V to 16V Protection Switch with Blocking FET Control

General Description

The eFuse SY20817A is a highly integrated circuit protection and power management solution in a compact package. The device uses few external components and provides multiple protection modes. It is a robust defense against overload, short circuit, and excessive inrush current conditions.

Extremely low power path resistance $R_{DS(ON)}$ helps to reduce power loss during normal operation. An open drain indicator pin is provided to show the operation status of the device. The device integrates overtemperature protection and auto-recovery with hysteresis to protect against overcurrent events.

The current limit level can be easily configured using a single external resistor. For applications with specific voltage ramp requirements, the SST pin can be set with a single capacitor to ensure the desired output ramp rate. Additionally, to prevent current flow from the load to the source during shutdown, an external NFET can be connected in back-to-back (B2B) configuration with the SY20817A output and controlled by the BFET pin.

The SY20817A is available in a compact QFN 2mm×2mm-12pin package.

Features

- Input Voltage Range: 2.5V to 16V
- Extremely Low Power Path Resistance $R_{DS(ON)}$
- $R_{DS(ON)}$=30mΩ (Typical)
- 1A to 5A Programmable Current Limit
- Open Drain Indicator Pin for Operation Status
- ±10% I_{LIMIT} Accuracy at 3A
- Programmable OUT Slew Rate
- Auto output discharge during shutdown
- Built-in Thermal Shutdown
- Compact Package: QFN2x2-12

Applications

- Power Banks
- LCD Panels
- HDD and SSD Drives
- Set Top Boxes
- Servers / AUX Supplies
- Fan Controls
- PCI/PCIe Cards
- Adapter Powered Devices

Typical Application Circuit

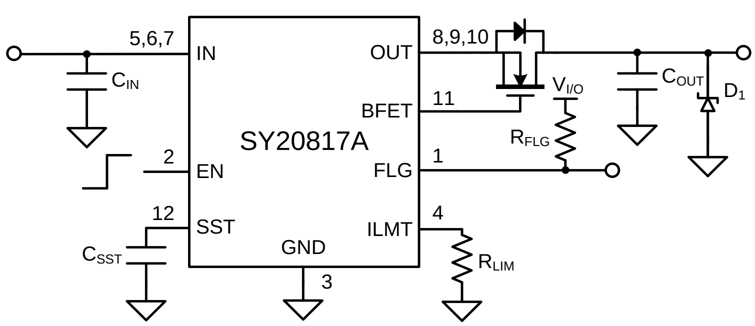


Figure 1. Schematic Diagram

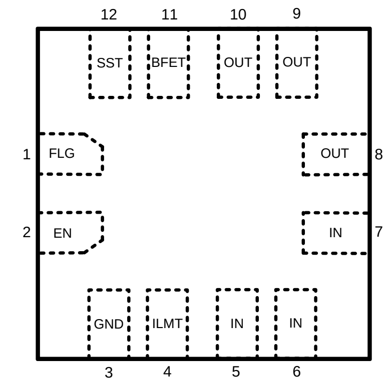
Ordering Information

SY20817 □(□□)□
Temperature Code
Package Code
Optional Spec Code

Ordering Number	Package Type	Top Mark
SY20817ATLC	QFN2×2-12	***Yexyz***

Device code: Ye
x=year code, y=week code, z= lot number code

Pinout (Top View)



(QFN2×2-12)

Pin Name	Pin Number	Pin Description
FLG	1	Open drain indicator pin. The pin will be pulled down when overcurrent, short circuit or thermal shutdown occurs. High impedance otherwise.
GND	3	Ground pin.
IN	5,6,7	Input voltage and supply voltage; connect a 0.1 μF or greater ceramic capacitor from IN to GND as close to the device as possible.
OUT	8,9,10	Power-switch output.
BFET	11	Connect this pin to the gate of an external blocking NFET. This pin can be left floating if it is not used.
EN	2	Pull high to enable. Do not leave it floating.
SST	12	Connect a capacitor from this pin to GND to control the ramp rate of the voltage at OUT pin during device turn-on.
ILMT	4	A resistor from this pin to GND will set the overcurrent limit.

Block Diagram

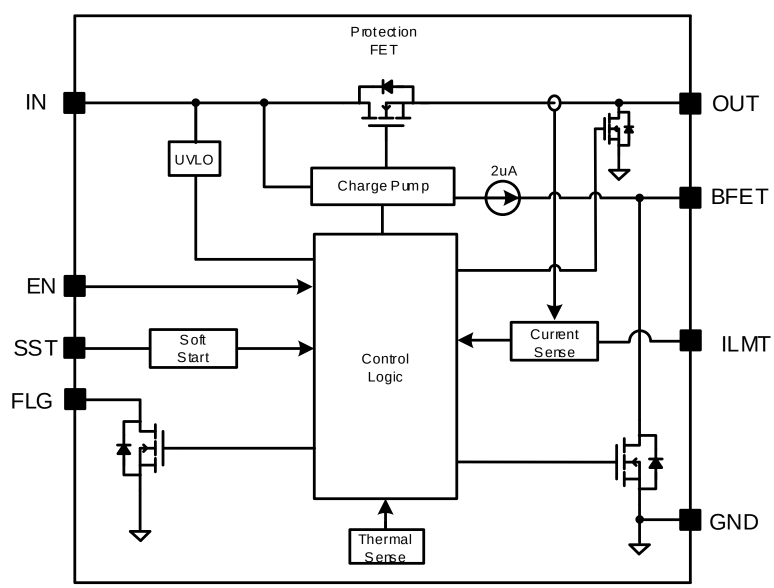


Figure 2. Block Diagram

Absolute Maximum Ratings (Note 1)

IN, EN, FLG -- -0.3V to 18V
OUT -- -0.3V to IN+0.3V
BFET -- -0.3V to 26V
ILMT, SST -- -0.3V to 3.6V
FLG Continuous Output Sink Current -- 25mA
BFET Continuous Output Sink Current -- 20mA
Power Dissipation, P_D @ T_A = 25°C-- 2.7W
Package Thermal Resistance (Note 2)
θ_{JA} -- 46°C/W
θ_{JC} --18°C/W
Junction Temperature Range -- -40°C to +150°C
Lead Temperature (Soldering, 10 sec.) -- 260°C
Storage Temperature Range -- -65°C to 150°C

Recommended Operating Conditions (Note 3)

IN -- 2.5V to 16V
BFET -- 0V to IN+6V
EN -- 0V to 16V
SST, ILMT -- 0V to 3V
OUT Continuous Output Current -- 0A to 5A
FLG Continuous Output Sink Current -- 0mA to 10mA
Junction Temperature Range -- -40°C to 125°C
Ambient Temperature Range -- -40°C to 85°C

Electrical Characteristics

($-40 \le T_J \le 125°C$, V_{IN} = 12 V, V_{EN} = 2 V, R_{ILMT} =1.1kΩ, C_{SST} = OPEN, R_{FLG} =10kΩ. Typical values are at 25°C. All voltages are with respect to GND, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.5		16	V
IN Rising UVLO Threshold Voltage	V_{UVLO}				2.45	V
Hysteresis	$V_{UVLO-HYS}$			100		mV
Shutdown Current	I_{SHDN}	EN=0V		2		μA
Bias Current	I_Q	EN=2V		62		μA
ON Resistance	$R_{DS(ON)}$	T_J = 25°C	24	30	36	mΩ
		T_J = 125°C		45	52	mΩ
OUT Overload Current limit	I_{OC}	R_{ILMT} = 5.5kΩ	0.80	1.00	1.20	A
		R_{ILMT} = 3.65kΩ	1.30	1.50	1.70	A
		R_{ILMT} = 2.75kΩ	1.80	2.00	2.20	A
		R_{ILMT} = 1.85kΩ	2.70	3.00	3.30	A
		R_{ILMT} = 1.1kΩ	4.50	5.00	5.50	A
Soft-Start Time Range	t_{SST}	Note 4	0.5		60	ms
Soft-Start Time Accuracy			-30%		30%	t_{SST}
Turn-On Delay Time	$t_{d(ON)}$	EN → H to I_{VIN} = 100 mA, 1A resistive load at OUT		200		μs
Turn-Off Delay Time	$t_{d(OFF)}$	EN → L to 0.9×OUT		100		μs
Output Discharge Resistor	R_{DIS}	V_{IN}=5V, EN=0, V_{OUT}=0.1V		100		Ω
BFET Charging Current	I_{BFET}	V_{BFET} = V_{OUT}		2		μA
BFET Clamp Voltage	$V_{BFET-MAX}$	V_{BFET} - V_{IN}		6.0		V
BFET Discharging Resistance to GND	$R_{BFET-DIS}$	V_{EN} = 0 V, I_{BFET} = 10mA	15	26	36	Ω
BFET Turn-On Duration	$t_{BFET-ON}$	EN→H to V_{BFET} = 12V, C_{BFET} = 1nF		6.0		ms
		EN→H to V_{BFET} = 12V, C_{BFET} = 10nF		60		ms
BFET Turn-Off Duration	$t_{BFET-OFF}$	EN→L to V_{BFET} = 1V, C_{BFET} = 1nF		7.5		μs
		EN→L to V_{BFET} = 1V, C_{BFET} = 10nF		8.5		μs
EN Pin Logic-High Voltage	V_{ENH}		1			V
EN Pin Logic-Low Voltage	V_{ENL}				0.4	V
FLG Output Low Voltage	V_{FLGL}	I_{FLG} = 1mA			200	mV
Over Current FLG Deglitch	t_{FLG}			2.6		ms
Thermal Shutdown Threshold	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			20		°C

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a Silergy’s test board.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4. Recommended Current Soft-start Time Programming Table:

SST cap (nF)	None	10	47	100
SR (V/ms)	6.67	1.74	0.37	0.17

Recommended formulas for C_{SS} and soft-start slew rate calculations:

$$SR_{OUT} = \frac{17\mu}{C_{SST}(nF)}(V/ms)$$

$$t_{SST} = 0.8 \times \frac{VIN}{SR_{OUT}}(ms)$$

(For a 12V application, using a 100nF SST capacitor will result in an OUT rise time of 56ms.)

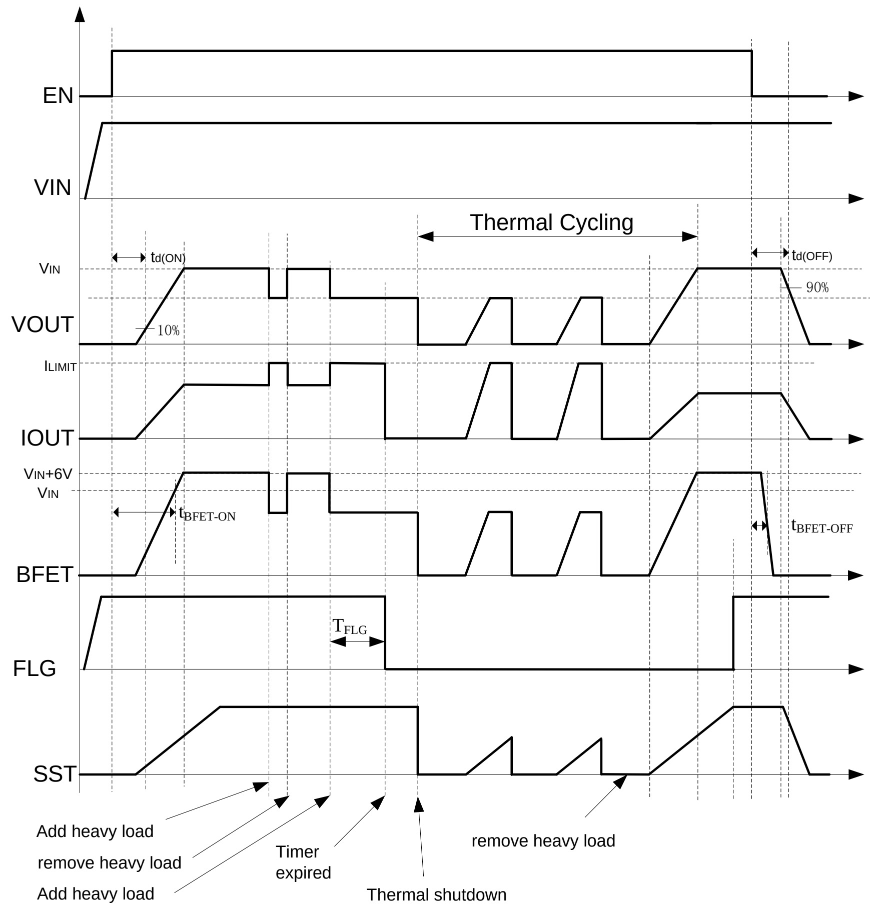
Note 5. Recommended Current Limit Program Table:

Current Limit Resistance (kΩ)	5.5	2.75	2.2	1.85	1.55	1.4	1.2	1.1
Current Limit (A)	1.0	2.0	2.5	3.0	3.5	4.0	4.5	5.0

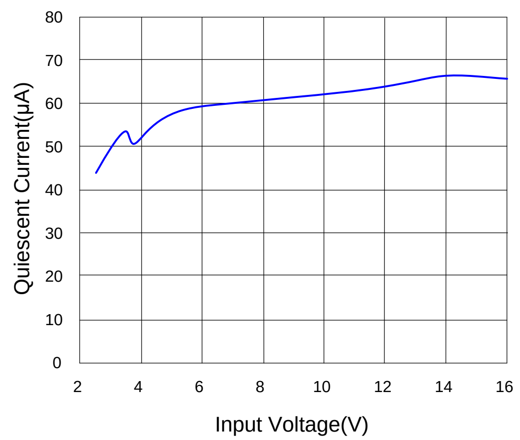
Recommended formula for R_{LIM} & current limit calculation:

$$R_{ILMT} = \frac{5.5K}{I_{LIM}}(\Omega)$$

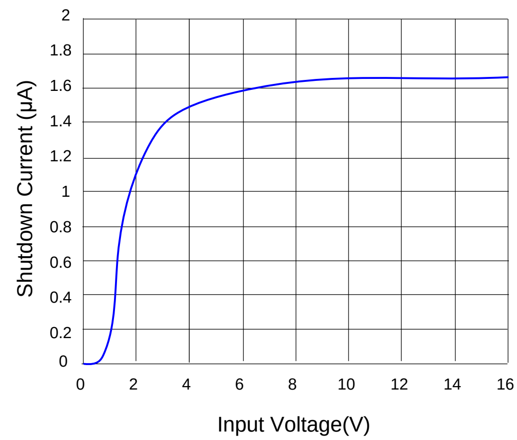
Timing Diagram



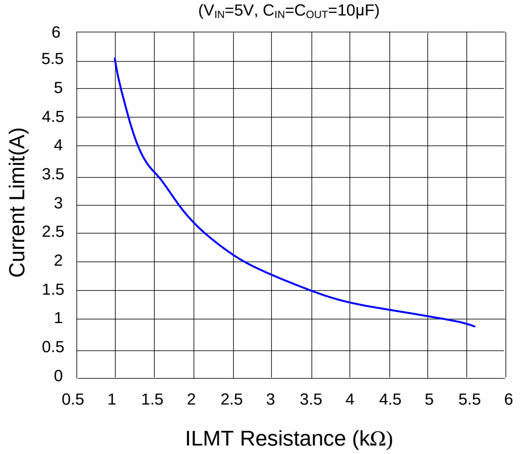
Typical Performance Characteristics



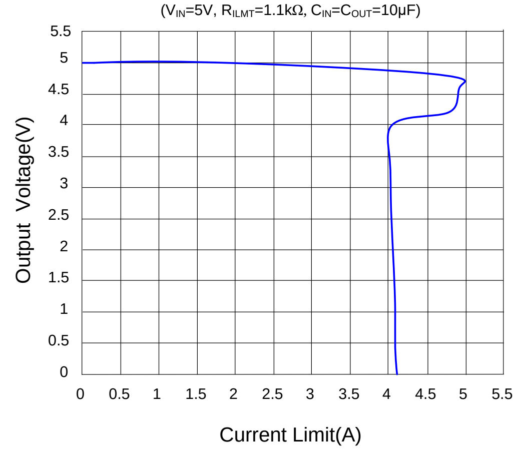
Quiescent Current vs. Input Voltage



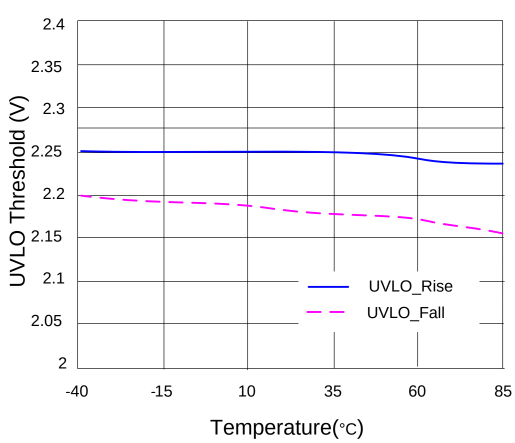
Shutdown Current vs. Input Voltage



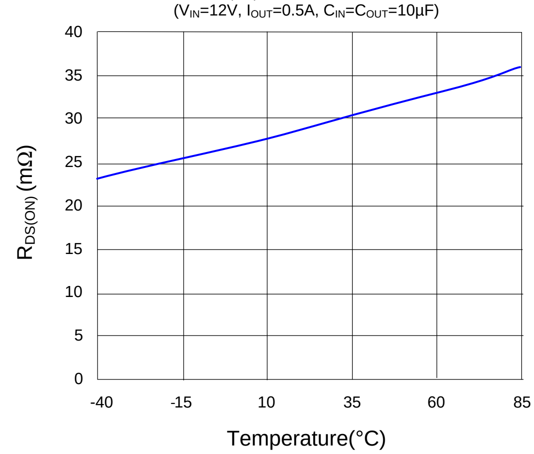
Current Limit vs. R_{LIM}
(V_{IN}=5V, C_{IN}=C_{OUT}=10μF)



Output Voltage Vs. Current Limit
(V_{IN}=5V, R_{ILMT}=1.1kΩ, C_{IN}=C_{OUT}=10μF)



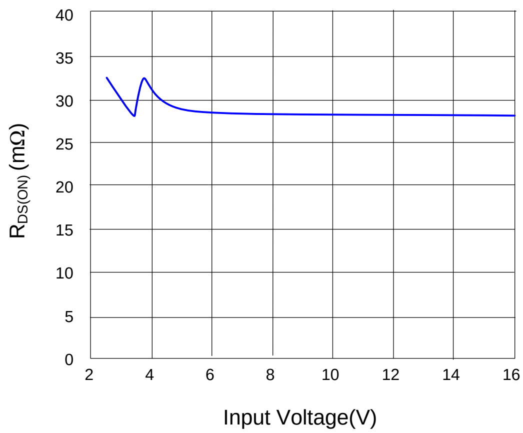
UVLO Threshold vs. Temperature



$R_{DS(ON)}$ vs. Temperature
(V_{IN}=12V, I_{OUT}=0.5A, C_{IN}=C_{OUT}=10μF)

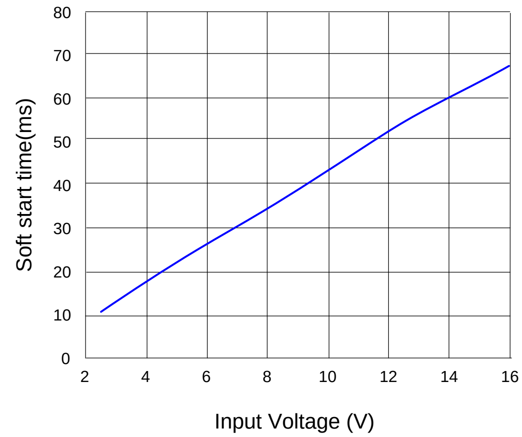
$R_{DS(ON)}$ vs. Input Voltage

(I_{OUT}=0.5A, C_{IN}=C_{OUT}=10μF)



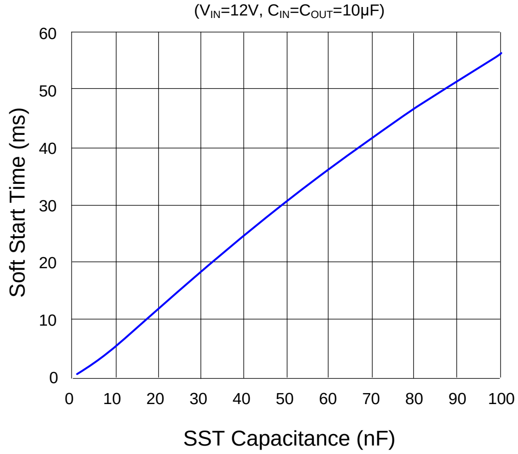
Soft Start Time vs. Input Voltage

(C_{SST}=100nF,C_{IN}=C_{OUT}=10μF)



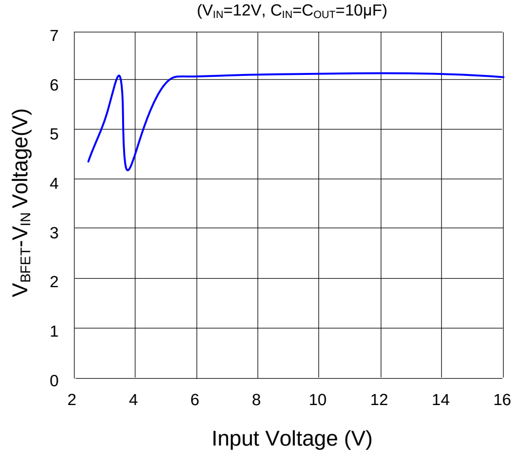
Soft Start Time vs. SST Capacitance

(V_{IN}=12V, C_{IN}=C_{OUT}=10μF)



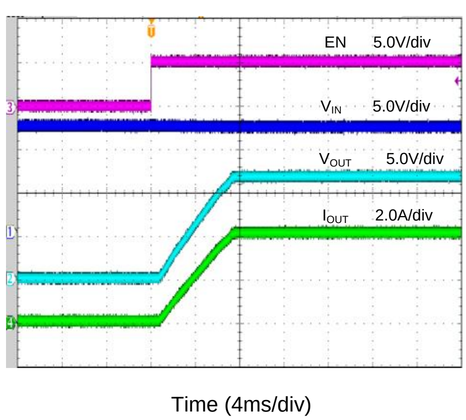
V_{BFET}-V_{IN} Voltage vs. Input Voltage

(V_{IN}=12V, C_{IN}=C_{OUT}=10μF)



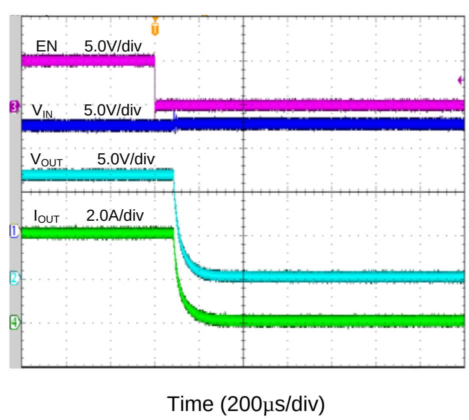
Startup from Enable

(V_{IN}=12V, C_{IN}=C_{OUT}=10μF, 3Ω Load)



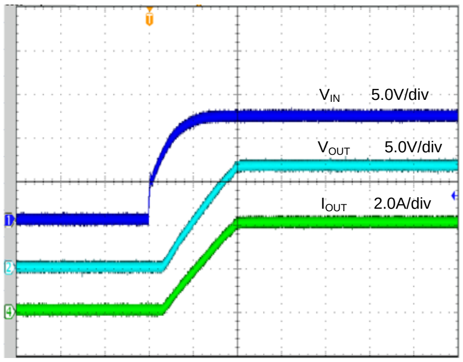
Shutdown from Enable

(V_{IN}=12V, C_{IN}=C_{OUT}=10μF, 3Ω Load)



Startup from V_{IN}

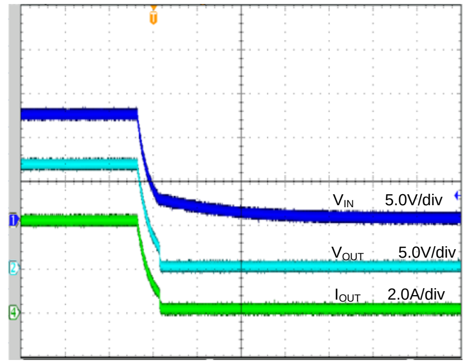
(V_{IN}=12V, C_{IN}=C_{OUT}=10μF, 3Ω Load)



Time (4ms/div)

Shutdown from V_{IN}

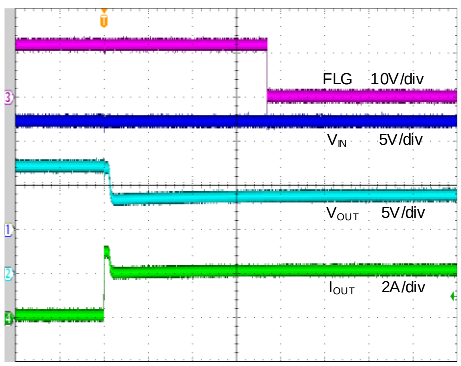
(V_{IN}=12V, C_{IN}=C_{OUT}=10μF, 3Ω Load)



Time (4ms/div)

OCP Response

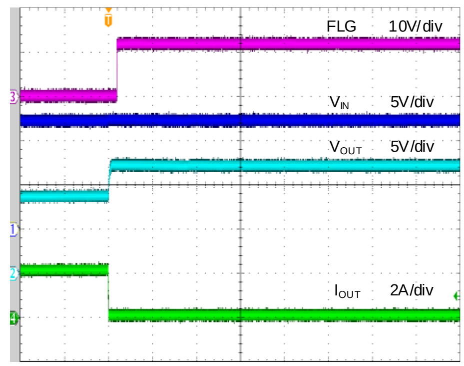
(V_{IN}=12V, C_{IN}=C_{OUT}=10μF, I_{LIMIT}=2.5A, Null load to 4Ω Load)



Time (800μs/div)

OCP Recovery

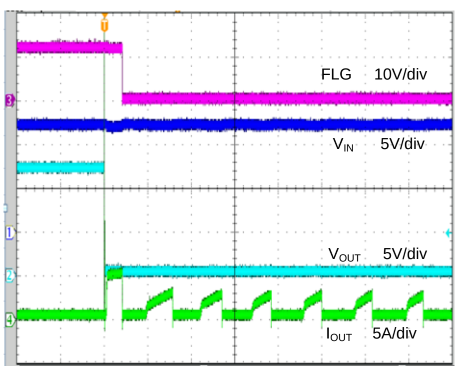
(V_{IN}=12V, C_{IN}=C_{OUT}=10μF, I_{LIMIT}=2.5A, 4Ω Load to Null load)



Time (800μs/div)

Short Circuit Response

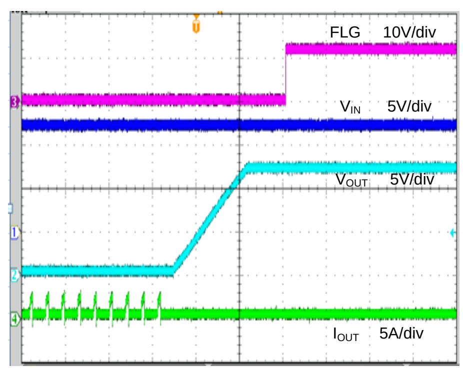
(VIN=12V, C_{IN}=C_{OUT}=10μF,I_{LIMT}=5A,Null load to short circuit)



Time (1ms/div)

Short Circuit Recovery

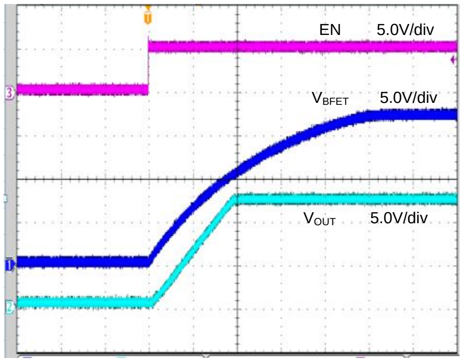
(VIN=12V, C_{IN}=C_{OUT}=10μF,I_{LIMT}=5A, remove short circuit)



Time (4ms/div)

BFET Turn On

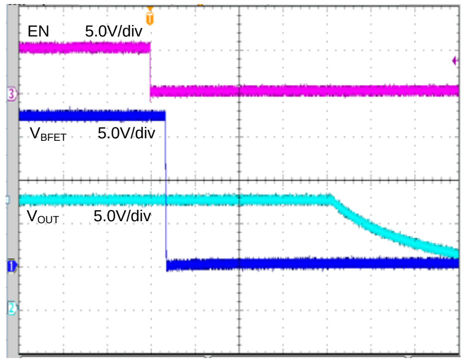
(V_{IN}=12V, C_{IN}=C_{OUT}=10μF, I_{LIMT}=5A, C_{BFET}=1nF, EN On)



Time (4ms/div)

BFET Turn Off

(V_{IN}=12V, C_{IN}=C_{OUT}=10μF, I_{LIMT}=5A, C_{BFET}=1nF, EN Off)



Time (20μs/div)

Application Information

Soft Start Time Programming:

Connect a capacitor from this pin to GND to control the slew rate of the output voltage at power-on. This pin can be left floating to obtain a predetermined slew rate (minimum t_{SST}) on the output.

SST cap (nF)	None	10	47	100
SR (V/ms)	6.67	1.74	0.37	0.17
t_{SST}/V_{IN}=12V(ms)	1.4	5.5	26	56

The C_{SST} and soft-start slew rate can be calculated using the following equations:

$$SR_{OUT} = \frac{17\mu}{C_{SST}(nF)}(V/ms)$$

$$t_{SST} = 0.8 \times \frac{V_{IN}}{SR_{OUT}}(ms)$$

BFET Control:

The SY20817A features a BFET pin designed to disconnect the input supply from the rest of the system in the event of a power failure at VIN. The BFET pin operation is controlled by either an input UVLO event or EN (see Table 1).

When EN is held low or the input voltage is below the UVLO threshold, the internal MOSFET is turned off, and the BFET pin is discharged, effectively blocking current flow from VOUT to VIN. The BFET is capable of sourcing a charging current of 2 µA (typical) and sinking (discharging) current from the gate of the external FET via a 26Ω internal discharge resistor, ensuring a fast turn-off. The BFET clamp voltage is 6V (typical), so it is recommended to choose a low gate voltage N-FET with low $R_{DS(ON)}$. If the application does not require the reverse current blocking function, the BFET pin can be left floating.

Table 1. BFET

EN > V_{EN}H	V_{IN}>V_{UVLO}	BFET MODE
H	H	Charge
X	L	Discharge
L	X	Discharge

Overcurrent Protection:

The device continuously monitors the load current, ensuring it remains within the programmed limit set by R_{ILMT}. Following the startup sequence and during regular operation, the current limit is configured to the IOC (overcurrent limit). For optimal stability of the internal regulation loop, it is recommended to use a 1% resistor within the range of 1.1k to 5.5k for R_{ILMT}.

The R_{ILIM} and current limit can be calculated using the following formula:

$$I_{OC} = \frac{5.5K}{R_{ILMT}}(A)$$

When an overcurrent condition (I_{OC}<I_{LOAD}<1.6×I_{OC}) occurs, the device maintains a constant output current and reduces the output voltage accordingly. Thermal shutdown protection occurs if the fault is present long enough to activate thermal shutdown. The device will remain off until the junction temperature drops by approximately 20°C, then it will restart. The device will continue to cycle on/off until the overcurrent condition is removed.

When a short condition (I_{LOAD}>1.6×I_{OC}) is detected, the power path will be turned off immediately. It will then try to restart again with the current limit.

FLG Response:

The FLG open-drain output is activated (active low) when overtemperature, current limit, or short circuit conditions are detected. During normal operation, the pin is pulled high by an external pull-up resistor. The FLG output stays active until the fault condition is resolved.

The SY20817A is designed to prevent false FLG reporting by incorporating internal deglitch circuits specifically designed for current limit conditions, eliminating the need for additional external circuitry. This ensures that FLG is not accidentally activated during routine operations, such as starting into a heavy capacitive load. Note that overtemperature conditions are not deglitched, causing an immediate activation of the FLG signal.

Supply Filter Capacitor:

A 1µF or larger input ceramic capacitor is strongly recommended to be placed close to the device. Without an input capacitor, an output short can cause ringing on the input, which could destroy the internal circuitry when the input transient exceeds the absolute maximum supply voltage, even for a short duration.

Output Filter Capacitor:

A 1µF output ceramic capacitor is recommended to be placed close to the device and output connector to reduce voltage drop during load transient. Higher output capacitor values can further reduce the drop during high-current applications.

In a short circuit scenario, the output could be exposed to a negative voltage caused by the parasitic wiring inductance. It is strongly recommended to connect a

Schottky diode in parallel. This diode will absorb large negative voltage spikes to keep the output voltage within the range of the absolute voltage rating.

Output discharge

The SY20817A integrates an 100Ω pull-down resistor for quick output discharge. The resistor is activated when the switch is turned off.

PCB Layout Guide:

For best performance of the SY20817A, the following guidelines must be followed:

1. Keep all VBUS traces as short and wide as possible and use at least 2-ounce copper for all VBUS traces.
2. Place the output capacitor as close to the connector as possible to lower the impedance and inductance between the port and the capacitor and improve transient performance.
3. Place the input and output capacitors close to the device and connect them to the ground plane to reduce noise coupling.

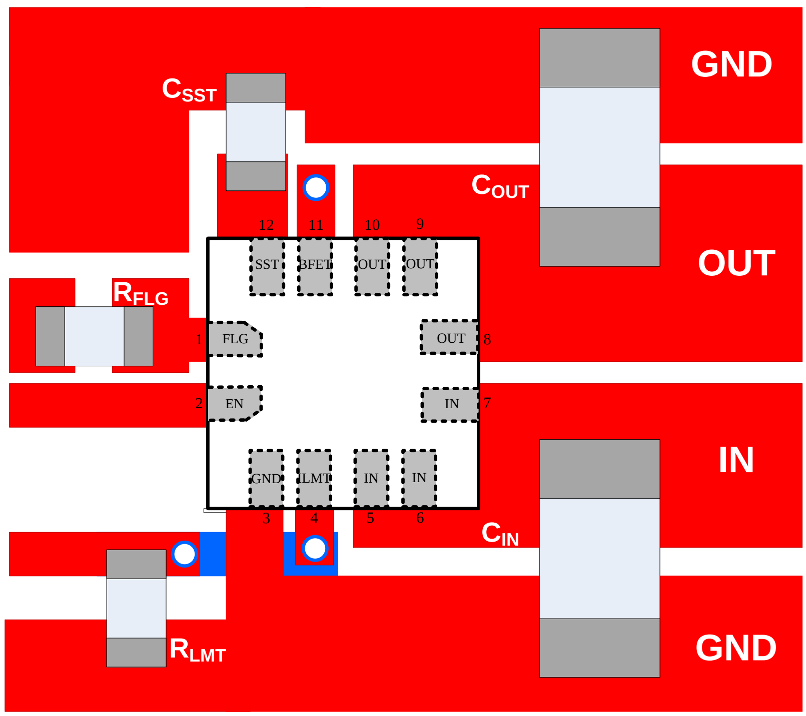


Figure 3. PCB Layout Suggestion

Schematic

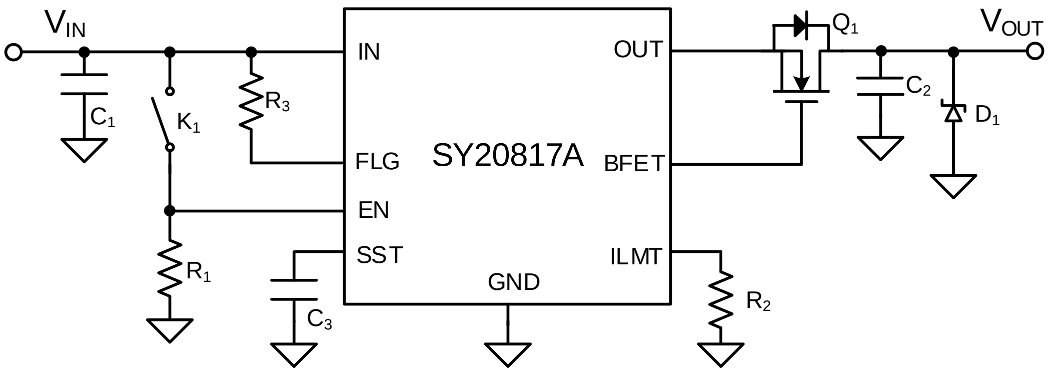
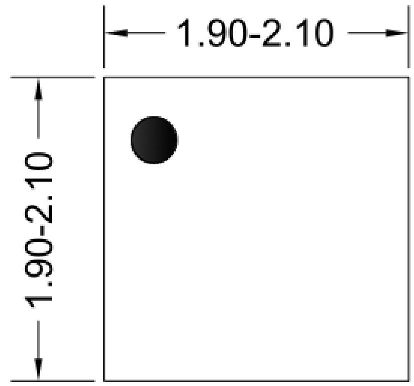


Figure1. Schematic Diagram

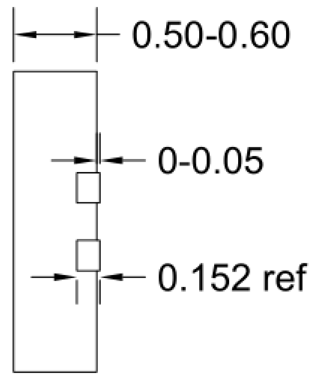
BOM List

Reference Designator	Description	Part Number	Manufacturer
C_1,C_2	10µF/25V, 1206, X5R	C3216X5R1E106KT000N	TDK
C_3	10nF/50V, 0603, X5R	C1608X5R1H103KT000N	TDK
R_1	1MΩ, 0603	RC0603FR-071ML	YAGEO
R_2	1.1kΩ, 0603	RC0603FR-071K1L	YAGEO
R_3	100kΩ, 0603	RC0603FR-07100KL	YAGEO
D_1	40V, 3A Schottky Diode	SS34	
Q_1	Null, Short D-S		

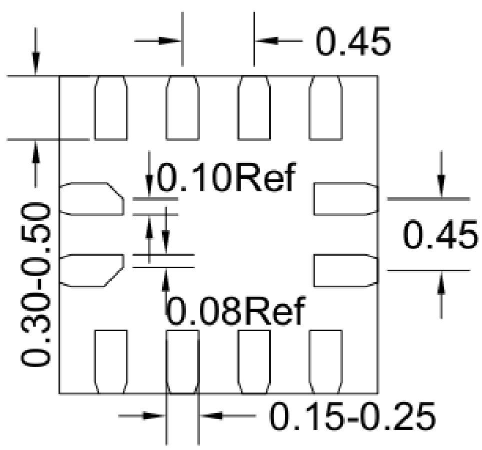
QFN2×2-12 Package Outline Drawing



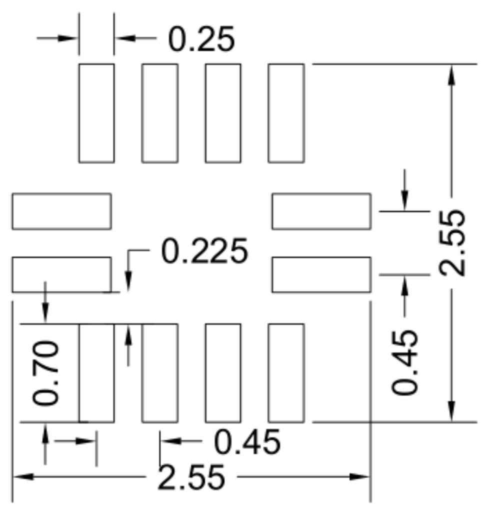
Top View



Side View



Bottom View

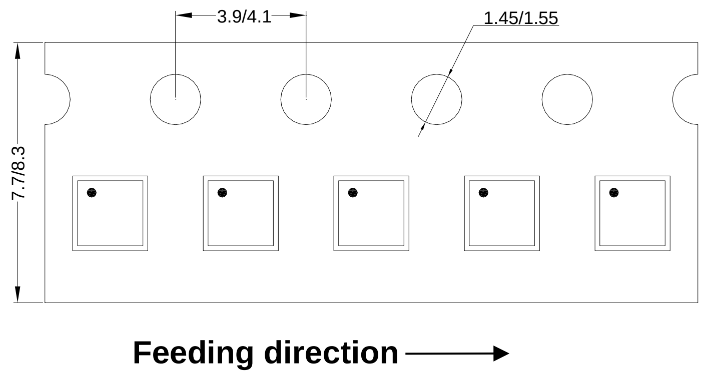


Recommended PCB Layout

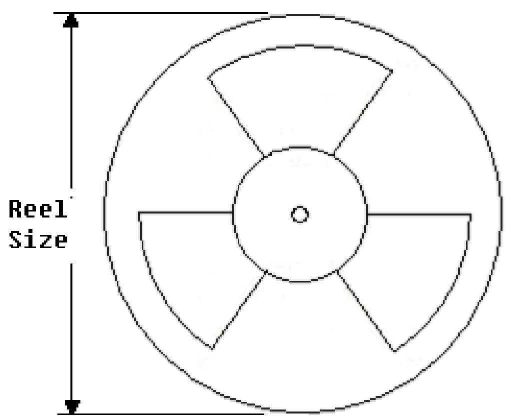
Note: All dimensions are in millimeters and exclude mold flash and metal burr.

Taping & Reel Specification

QFN2×2 Taping Orientation



Carrier Tape & Reel Specification for Packages



Package type	Tape width (mm)	Pocket pitch (mm)	Reel size (Inch)	Trailer length (mm)	Leader length (mm)	Qty per reel
QFN2×2	8	4	7"	400	160	3000

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change
Dec.12, 2023	Revision 1.0	Language improvements for clarity.
Apr.29, 2022	Revision 0.9A	Update the waveforms of OCP Response (Page 9)
Jun. 08, 2018	Revision 0.9	Initial Release

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