SY20681

High Efficiency, 4uA Ultra Low I_Q, 3MHz, 0.6A Inductor Built-in Synchronous Step Down Regulator

General Description

The SY20681 is a 3MHz, 0.6A, 4μA ultra low quiescent current, synchronous step-down converter which integrates an inductor and a control IC in one tiny package (2.0mm×1.5mm, H=1.0mm). It can operate over a wide input voltage range from 1.8V to 5.5V and integrates main switch and synchronous switch with very low $R_{DS\ (ON)}$ to minimize the conduction loss.

Features

- Low $R_{DS(ON)}$ for Internal Switches (Top/Bottom) : 230mΩ/110mΩ
- Integrate an Inductor to Minimizes the External Components and PCB Layout Design
- 1.8~5.5V Input Voltage Range
- 4μA Ultra Low Quiescent Current
- High Switching Frequency 3MHz Minimizes the External Components
- Internal Soft-start Limits the Inrush Current
- 100% Dropout Operation
- RoHS Compliant and Halogen Free
- Compact Package: QFN2x1.5-8

Applications

- Mobile Phone, Smart Phone
- Bluetooth Headsets
- Portable Game Console
- Digital Camera, Camcorder

Typical Applications

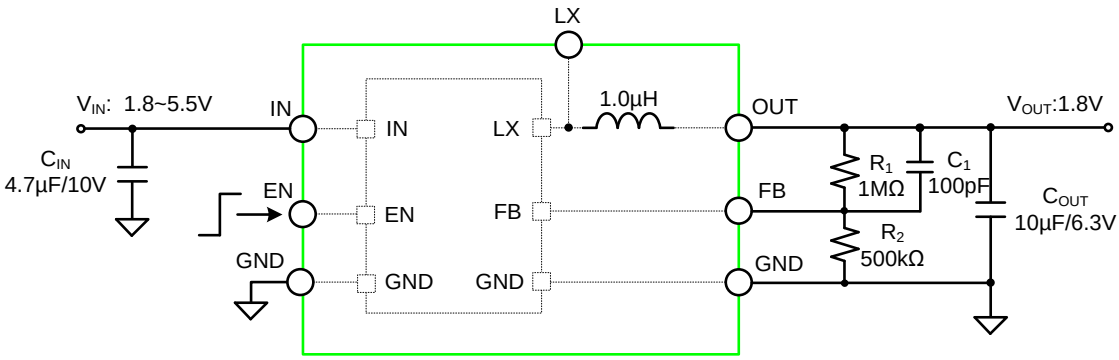


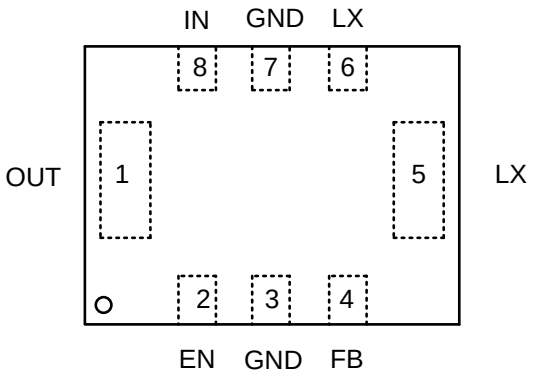
Figure 1. Schematic Diagram

Ordering Information

Ordering Part Number	Package type	Top Mark
SY20681QUC	QFN2×1.5-8 RoHS Compliant and Halogen Free	**Kaxyz**

x=year code, y=week code, z= lot number code

Pinout (top view)



Pin Name	Pin Number	Pin Description
OUT	1	Output Pin. Decouple this pin to ground with at least a 10uF ceramic capacitor.
EN	2	Enable control. Pull high to turn on. Do not leave it floating.
GND	3, 7	Ground pin.
FB	4	Output adjustable version. Connect this pin to the center point of the output resistor divider to program the output voltage: $V_{OUT}=0.6\times(1+R_1/R_2)$.
LX	5,6	Built-in inductor node. Leave it floating.
IN	8	Input pin. Decouple this pin to GND pin with at least a 4.7uF ceramic capacitor.

Absolute Maximum Ratings (1)	Min	Max	Unit
IN,LX,OUT		6	V
FB	-0.3	IN + 0.3	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering,10sec.)		260	
Storage Temperature	-65	150	

Thermal Information (2)	Min	Max	Unit
θ_{JA} Junction-to-ambient Thermal Resistance		60.3	°C/W
θ_{JC} Junction-to-case Thermal Resistance		10	
P_D Power Dissipation T_A=25°C		400	mW

Recommended Operating Conditions (3)	Min	Max	Unit
IN	1.8	5.5	V
Junction Temperature	-40	125	°C
Ambient Temperature	-40	85	°C

Electrical Characteristics

Electrical Characteristics V_{IN} = 4.2V, V_{OUT} = 1.8V, C_{OUT} = 10μF, T_A = 25°C, unless otherwise specified						
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
Input Voltage Range	V_{IN}		1.8		5.5	V
Quiescent Current	I_Q	I_{OUT}=0, V_{FB}=V_{REF}×105%		4		μA
Shutdown Current	I_{SHDN}	EN=0		0.1	1	μA
Feedback Reference Voltage	V_{REF}		0.588	0.6	0.612	V
PFET R_{ON}	$R_{DS(ON),P}$			230		mΩ
NFET R_{ON}	$R_{DS(ON),N}$			110		mΩ
Inductance	L			1.0		μH
PFET Current Limit	I_{LIM}		1.3			A
EN Rising Threshold	V_{ENH}		1.2			V
EN Falling Threshold	V_{ENL}				0.4	V
Input UVLO Threshold	V_{UVLO}				1.8	V
UVLO Hysteresis	V_{HYS}			0.1		V
Oscillator Frequency	f_{OSC}			3		MHz
Min ON Time				80		ns
Max Duty Cycle			100			%
Soft-start Time	t_{SS}			1		ms
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			15		°C
Output discharge resistor	R_{DSC}			70		Ω

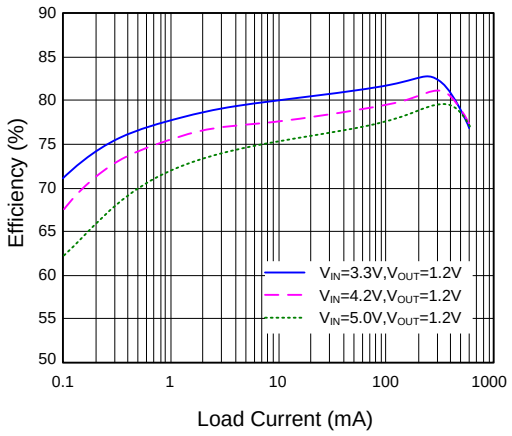
Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection on a two-layer Silergy Evaluation Board.

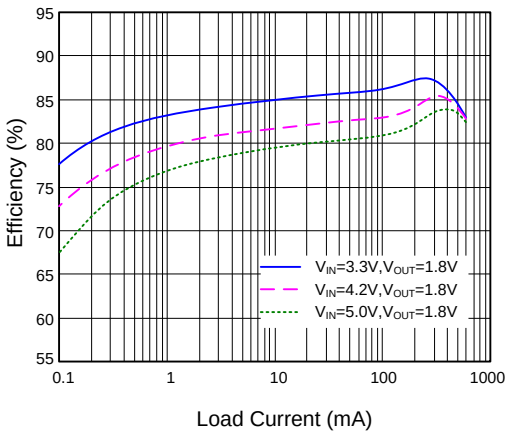
Note 3: The device is not guaranteed to function outside its operating conditions

Typical Performance Characteristics

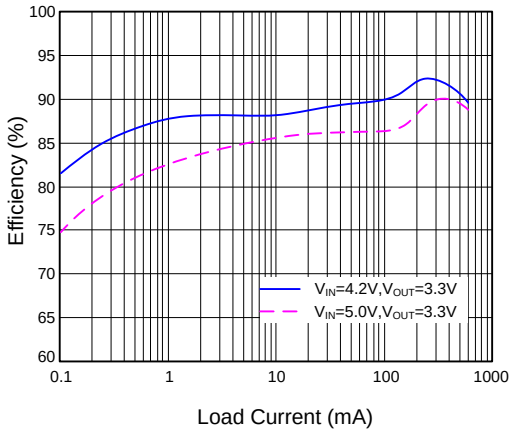
Efficiency vs. Load Current



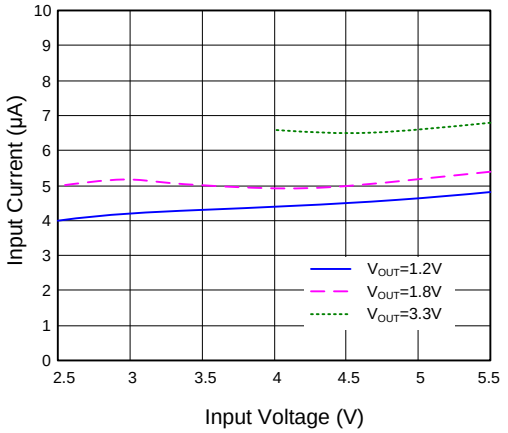
Efficiency vs. Load Current



Efficiency vs. Load Current

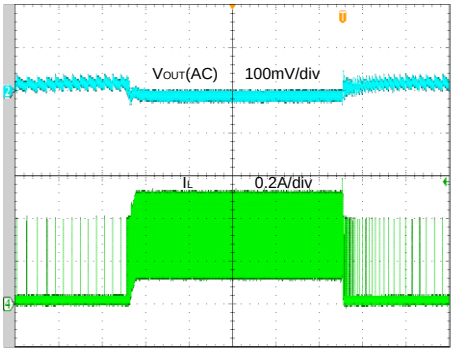


Null Load Input Current vs. Input Voltage



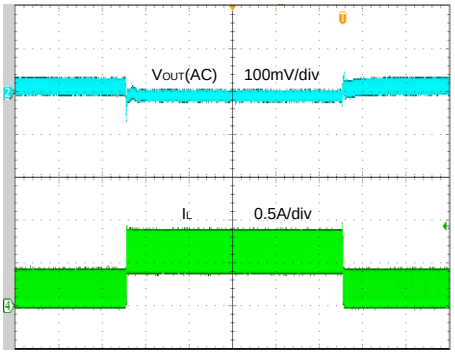
Load Transient

(VIN=5.0V, VOUT=1.8V, ILOAD=0 ~ 0.3A)



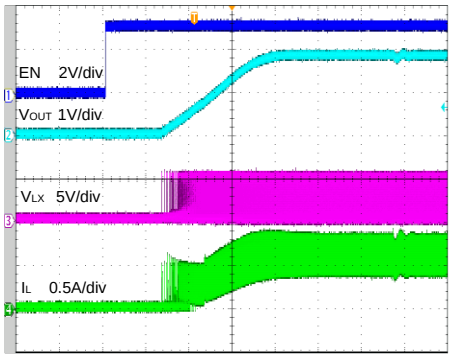
Load Transient

(VIN=5.0V, VOUT=1.8V, ILOAD=0.06 ~ 0.6A)



Startup

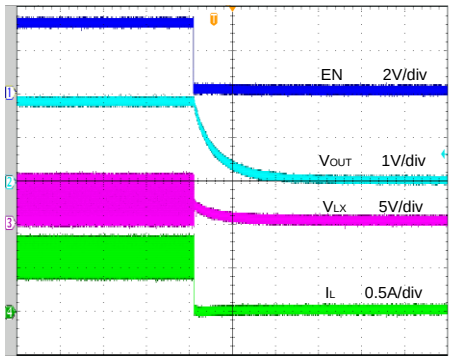
(V_{IN}=5.0V, V_{OUT}=1.8V, I_{LOAD}=0.6A)



Time (400μs/div)

Shutdown

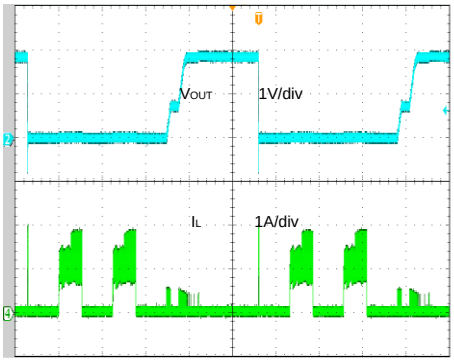
(V_{IN}=5.0V, V_{OUT}=1.8V, I_{LOAD}=0.6A)



Time (100μs/div)

Short Circuit Protection

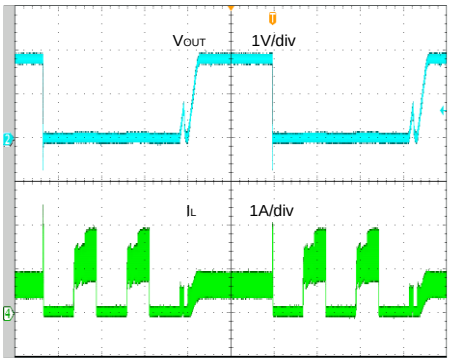
(V_{IN}=5.0V, V_{OUT}=1.8V, 0A to Short)



Time (4ms/div)

Short Circuit Protection

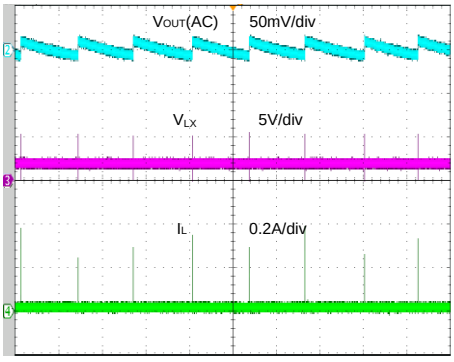
(V_{IN}=5.0V, V_{OUT}=1.8V, 0.6A to Short)



Time (4ms/div)

Output Ripple

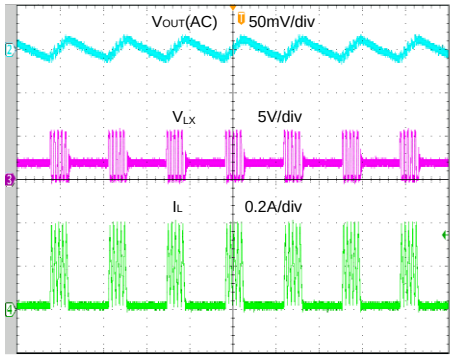
(V_{IN}=5.0V,V_{OUT}=1.8V, I_{LOAD}=0A)



Time (100ms/div)

Output Ripple

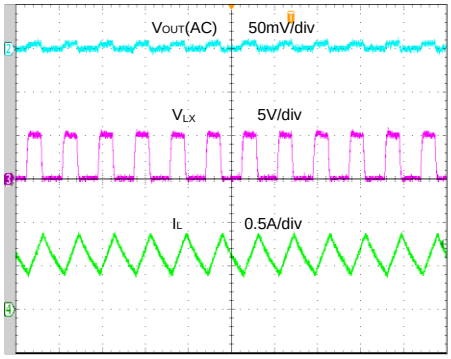
(V_{IN}=5.0V,V_{OUT}=1.8V, I_{LOAD}=0.06A)



Time (4μs/div)

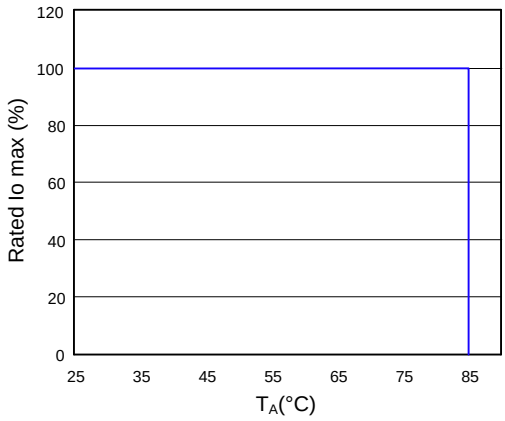
Output Ripple

(V_{IN}=5.0V,V_{OUT}=1.8V, I_{LOAD}=0.6A)



Thermal Derating Curve

(V_{IN}=5V,V_{OUT}=3.3V,0LFM)



Notes:

1) T_A: Air temperature, 0.5 inch above the IC.
2) Based on a four-layer Silergy Evaluation Board in the natural convection.
3) The inductor temperature is not beyond 115℃ under this TD curve.
4) For customer's specific application, the recommended inductor temperature limitation is 115℃.

Operation

SY20681 is a 3MHz, 0.6A, 4μA ultra low quiescent current, synchronous step-down converter which integrates an inductor and a control IC in one tiny package (2.0mm×1.5mm, H=1.0mm). It can operate over a wide input voltage range from 1.8V to 5.5V and integrates main switch and synchronous switch with very low $R_{DS\ (ON)}$ to minimize the conduction loss.

Applications Information

Because of the high integration in SY20681, the application circuit based on this IC is rather simple. Only the input capacitor C_{IN}, the output capacitor C_{OUT} and the feedback resistors (R_1 and R_2) need to be selected for the targeted application specifications.

Feedback Resistor Dividers R1 and R2:

Choose R_1 and R_2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_1 and R_2. A value of greater than 1MΩ is highly recommended for R_1 resistor. If R_1 =1MΩ is chosen, then R_2 can be calculated to be:

$$R_2 = \frac{0.6V}{(V_{OUT} - 0.6V)} \times R_1$$

Input Capacitor CIN:

A typical X7R or better grade ceramic capacitor greater than 4.7μF capacitance is recommended. To minimize the potential noise problem, this ceramic capacitor should be placed really close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and IN/GND pins.

Output Capacitor COUT:

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use an X7R or better grade ceramic capacitor with 6V rating and greater than 10uF capacitance, when V_{OUT} is 1.2V, C_{OUT} is recommended to be greater than 20μF.

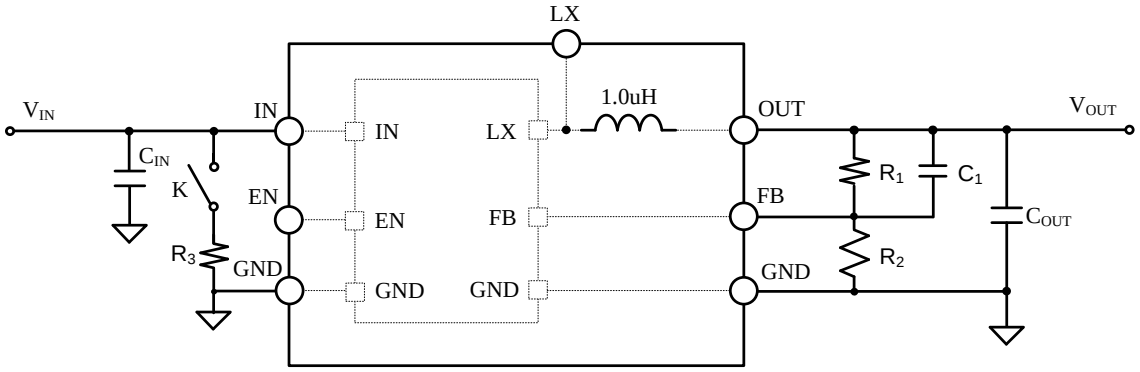
Load Transient Considerations:

SY20681 integrates the compensation components to achieve good stability and fast transient response. In some applications, adding a 22pF~100pF ceramic cap in parallel with R_1 may further speed up the load transient responses and is thus recommended for applications with large load transient step requirements.

Short Circuit Protection:

SY20681 integrates hic-cup mode hard short protection function. If the FB is below 0.2V, the internal soft-start node and the error amplifier output will be reset immediately. The IC works in hic-cup protection mode. The hiccup frequency is about 200Hz, and the hic-cup duty is 50%. If the hard short condition is removed, the IC will go back to normal operation.

Typical Application Schematic



Recommended Table

VOUT(V)	R1(kΩ)	R2(kΩ)
1.2	1000	1000
1.8	1000	500
3.3	1000	221

Bom List

Reference Designator	Description	Part Number	Manufacturer
C_{IN}	4.7μF/10V, 0402, X5R	C1005X5R1A475M	TDK
C_{OUT}	10μF/6.3V, 0603, X5R	C1608X5R0J106M	TDK
C_1	100pF/50V, 0603, C0G	C1608C0G1H101J	TDK
R_1	1MΩ, 1%, 0603		
R_2	500kΩ, 1%, 0603		
R_3	1MΩ, 0603		

Layout Design:

For the minimum noise problems, we should place the following components close to the IC: C_{IN} and C_{OUT}.

1) It is desirable to maximize the PCB copper area connecting to the GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

2) The C_{IN} must be close to the IN and GND pins. The loop area formed by the C_{IN} and GND must be minimized.

3) Connect the LX pins together to reduce the inductor DCR. It is strongly recommended to reduce the LX routing area to avoid the potential noise problem.

4) The trace connecting to the FB pin must NOT be adjacent to the LX node on the PCB layout to minimize the noise coupling to the FB pin.

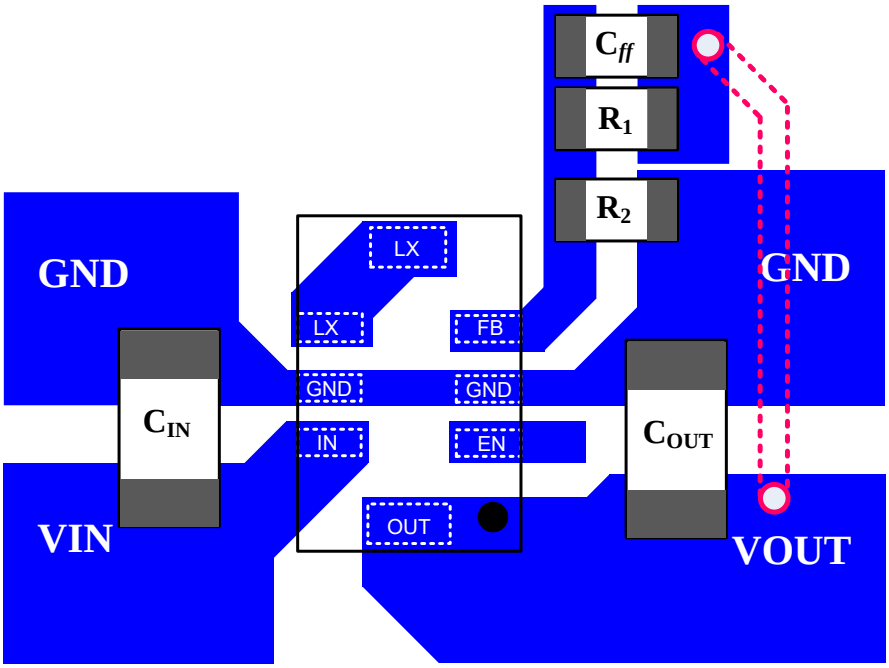
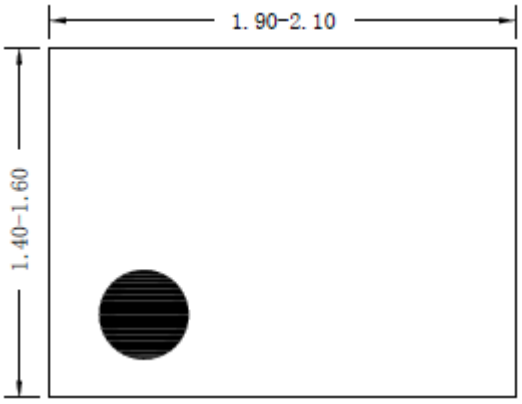
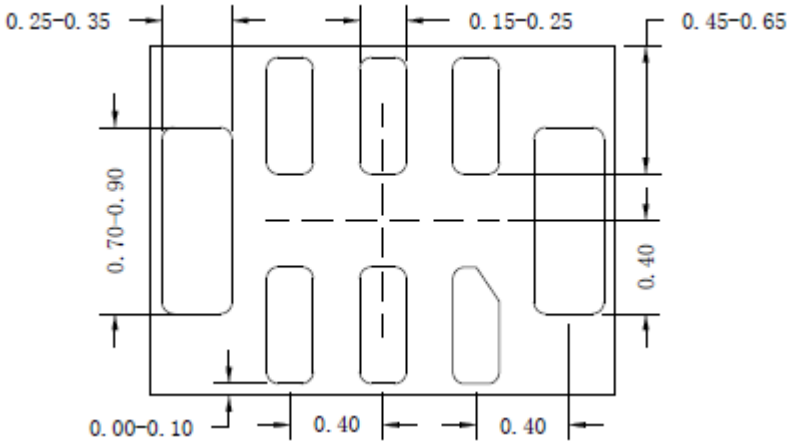


Figure2. PCB Layout Suggestion

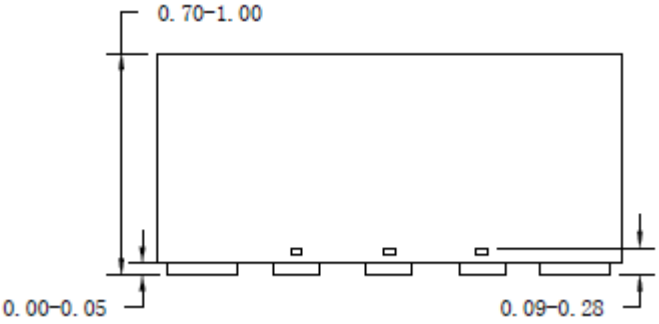
QFN2×1.5-8 Package Outline Drawing



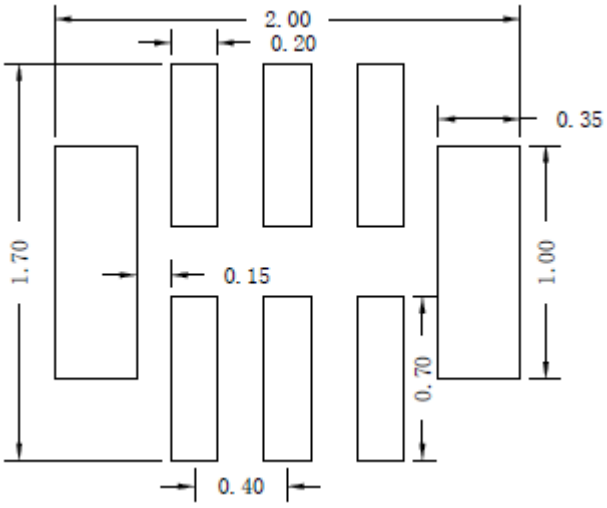
Top View



Bottom View



Side View

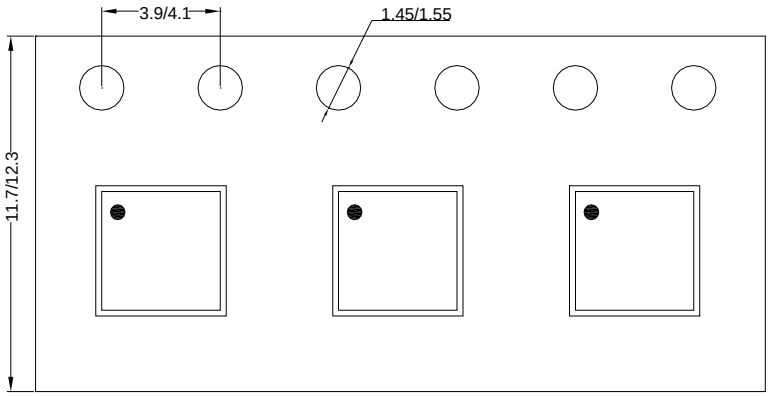


Recommended PCB layout (Reference only)

Notes: All dimension in millimeter and exclude mold flash & metal burr

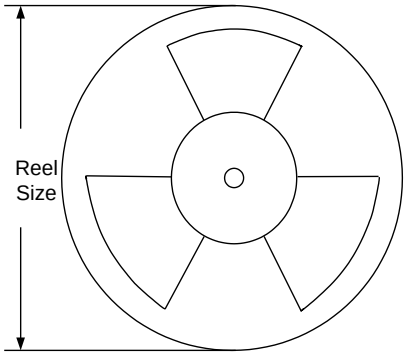
Taping & Reel Specification

1. QFN2×1.5 taping orientation



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN2×1.5	8	4	7	400	160	3000

3. Others: NA

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