SY20616D

High Efficiency 6A, 1.5MHz, I²C Programmable Inductor Built-in Synchronous Step Down Regulator

General Description

The SY20616D is a high efficiency 1.5MHz, 6A synchronous step-down DC/DC regulator which integrates an inductor and a control IC in one tiny package (4.0mm×3.0mm, H=2.0mm). It can operate over a wide input voltage range from 2.7V to 5.5V and integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss. The output voltage can be programmed from 0.6V to 1.5V through the I²C interface.

Applications

- Smart-phone
- Web-tablets

Features

- 2.7V to 5.5V Input Voltage Range
- Pseudo-constant Frequency: 1.5MHz
- Internal Soft-start Limits the Inrush Current
- Typical 95μA Quiescent Current
- Programmable Output Voltage: 0.6V to 1.5V in 10mV Steps
- 6A Continuous Load Current Capability
- Remote Voltage Sense Function to Provide Excellent Output Accuracy
- 1 MHz Fast Mode plus I²C Bus Interface
- Hic-cup Mode Protection for Hard Short Condition
- Power Good Indicator
- RoHS Compliant and Halogen Free
- Compact Package: MQFN3×4-16

Typical Applications

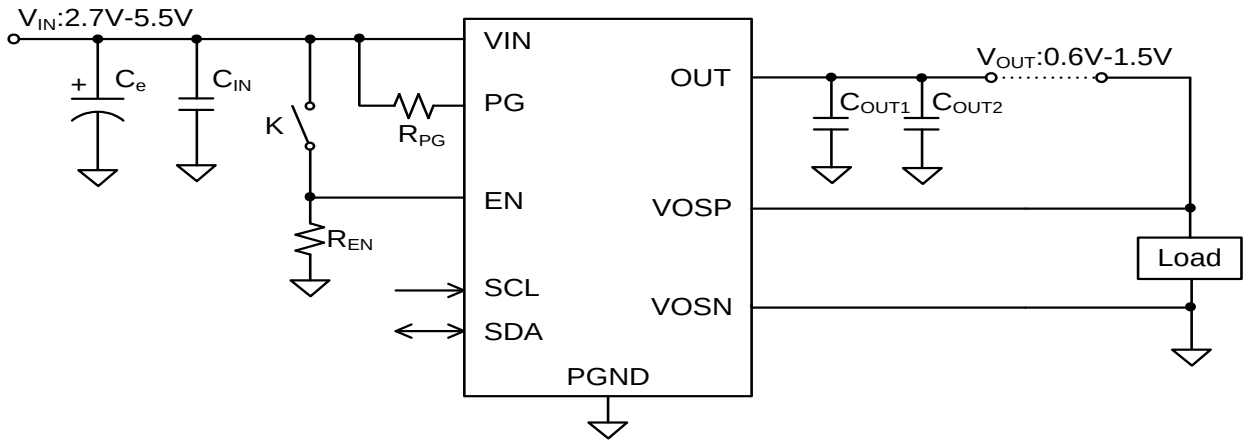


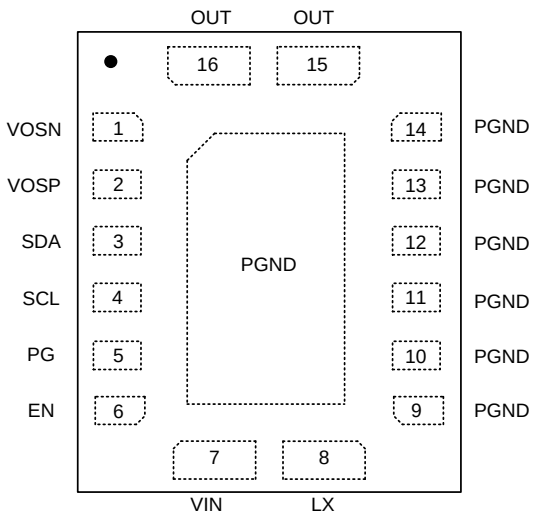
Figure 1. Schematic Diagram

Ordering Information

Ordering Part Number	Package type	Top Mark
SY20616DABM	MQFN3×4-16 RoHS Compliant and Halogen Free	**GWL*xyz***

x=year code, y=week code, z= lot number code

Pinout (top view)



Pin Name	Pin Number	Pin Description
VOSN	1	Negative remote sense pin. Connect to GND of the load side.
VOSP	2	Positive remote sense pin. Connect to VOUT of the load side.
SDA	3	I2C interface Bi-directional data line.
SCL	4	I2C interface clock line.
PG	5	Power good indicator. When the output voltage exceeds 90% of regulation point, it becomes open drain. Low otherwise.
EN	6	Enable control pin. Pull high to turn on. Do not leave it floating. When EN pin is low, the I2C register settings will be set to the default values.
VIN	7	Power input pins. Decouple this pin to PGND with at least one piece 22μF ceramic capacitor.
LX	8	Inductor pins. Leave it floating.
PGND	9-14	Power ground pin. The largest central pad is also power ground.
OUT	15,16	Output pin. Decouple this pin to PGND with at least two pieces 22μF ceramic capacitors.

Block Diagram

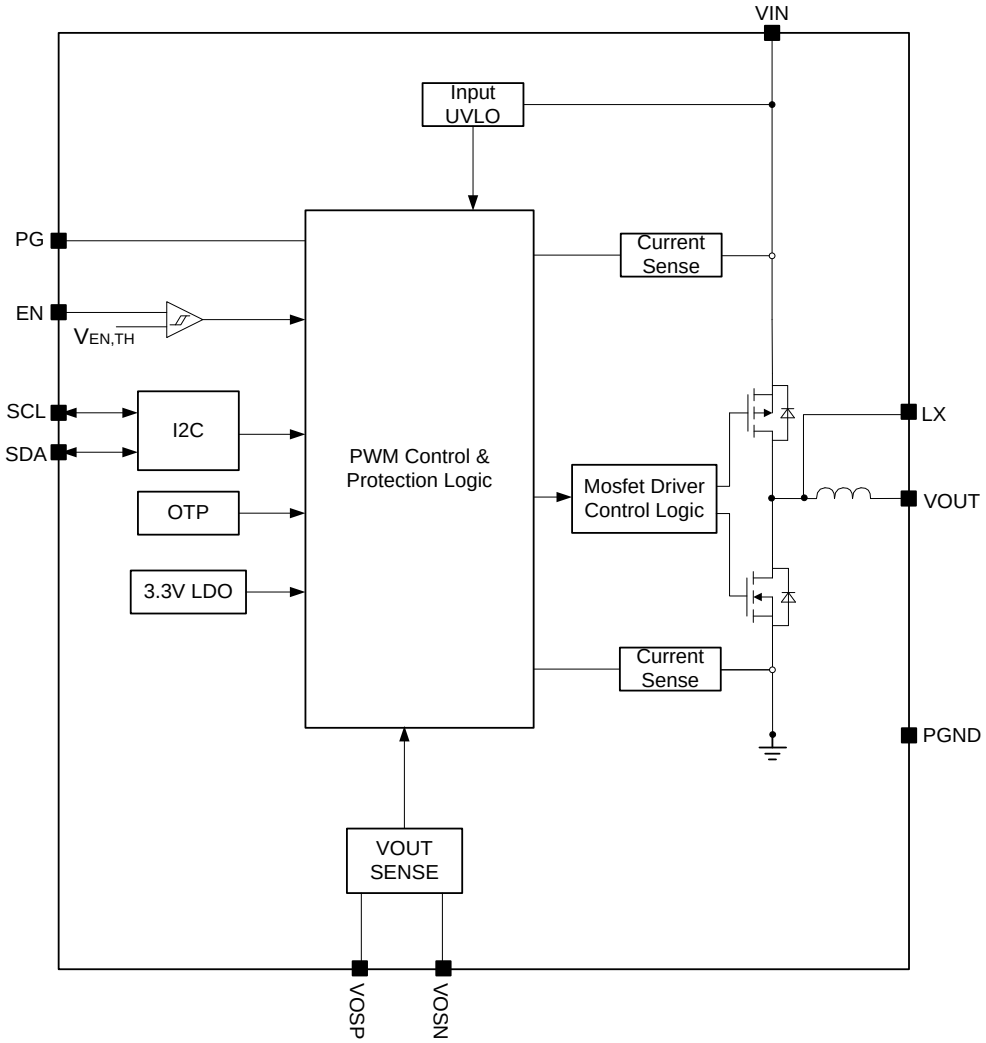


Figure2.Block Diagram

Absolute Maximum Ratings (1)	Min	Max	Unit
IN	-0.3	6	V
EN, PG, SCL, SDA, VOSP, VOSN	-0.3	IN + 0.6	
Junction Temperature, Operating	-40	125	°C
Lead Temperature (Soldering,10sec.)		260	
Storage Temperature	-40	125	

Thermal Information (2)	Min	Max	Unit
θ_{JA} Junction-to-ambient Thermal Resistance		26.4	°C/W
P_D Power Dissipation T_A=25°C		3.8	W

Recommended Operating Conditions (3)	Min	Max	Unit
IN	2.7	5.5	V
Output Voltage	0.6	1.5	
Output Current	0	6	A

Electrical Characteristics

Electrical Characteristics V_{IN} = 5V, V_{OUT} = 1V, C_{OUT} = 2*22µF, T_A = 25°C, unless otherwise specified						
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
Input Voltage Range	V_{IN}		2.7		5.5	V
V_{IN} UVLO	V_{UVLO}	V_{IN} Rising		2.55	2.7	V
V_{IN} UVLO Hysteresis	V_{UVHYST}			150		mV
Quiescent Current	I_Q	I_{OUT}=0, EN=1, Buck_ENx=1,FB=105%*V_{REF}		95		µA
Shutdown Current	$I_{SHDN\_H/W}$	EN=0		0.5	1	µA
	$I_{SHDN\_S/W}$	EN=V_{IN}, Buck_ENx=0		40		
EN Input Voltage High	$V_{EN,H}$		1.1			V
EN Input Voltage Low	$V_{EN,L}$				0.4	V
SDA, SCL						
Logic High	$V_{I2C,H}$		1.5			V
Logic Low	$V_{I2C,L}$				0.4	V
Output Voltage Set-Point	V_{SET}	Forced PWM, V_{OUT}=VSEL0, default value	-1		+1	%
Output Current Limit	$I_{OUT,LIMT}$		6			A
Soft-start Time (Note 4)	t_{SS}	10%-90% VOUT		300		µs
Min on time (Note 4)	$t_{ON, MIN}$			65		ns
Switching Frequency	f_{sw}			1.5		MHz
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			15		°C
Output Discharge Resistance	R_{DIS}			120		Ω
VOSN Compensation Range	V_{VOSN}		120			mV
Input OVP Threshold	V_{OVP}	Rising threshold		6.2		V
		Falling threshold	5.65	5.85		V
Input OVP Blanking Time	$T_{Blanking}$			10		µs

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a four-layer 2-oz 80×80mm (L×W) Silergy Evaluation Board.

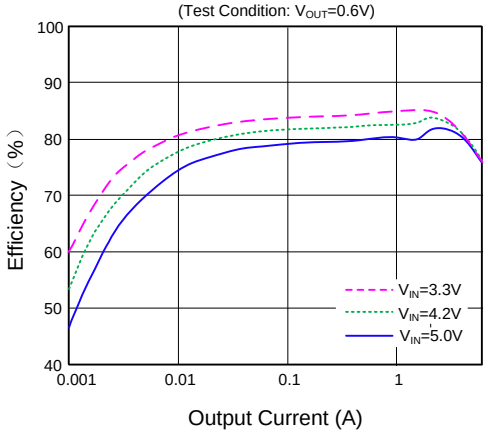
Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: The values are guaranteed by design.

Typical Performance Characteristics

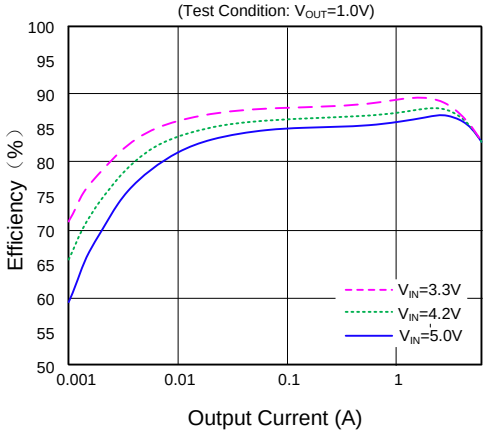
Efficiency vs. Output Current

(Test Condition: V_{OUT}=0.6V)



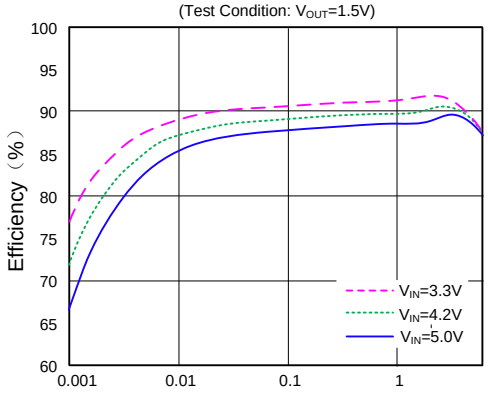
Efficiency vs. Output Current

(Test Condition: V_{OUT}=1.0V)



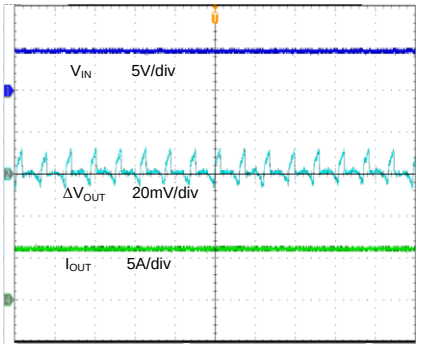
Efficiency vs. Output Current

(Test Condition: V_{OUT}=1.5V)



Output Ripple

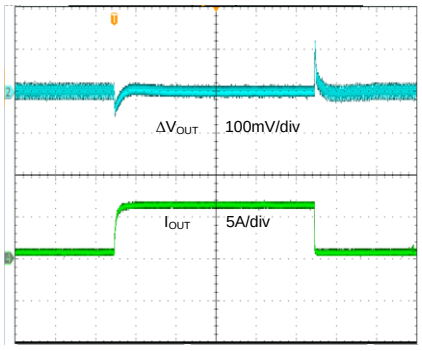
(V_{IN}=5V,V_{OUT}=1V,I_{OUT}=6A)



Time(1μs/div)

Load Transient

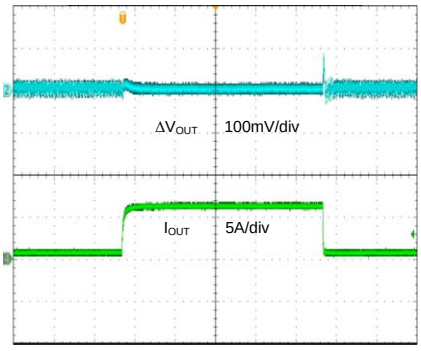
(MODE0=0, V_{IN}=5V, V_{OUT}=1V, I_{OUT}=0.6~6A,
0.5A/μs rise, 9A/μs fall)



Time(100μs/div)

Load Transient

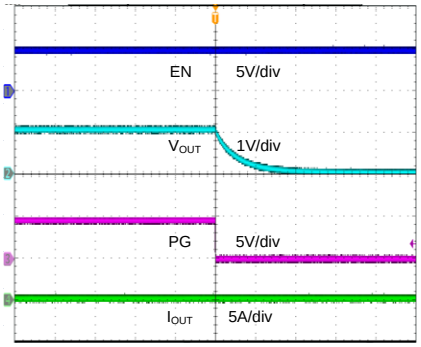
(MODE0=1, V_{IN}=5V, V_{OUT}=1V, I_{OUT}=0.6~6A,
0.5A/μs rise, 9A/μs fall)



Time(100μs/div)

Shutdown From BUCK_EN

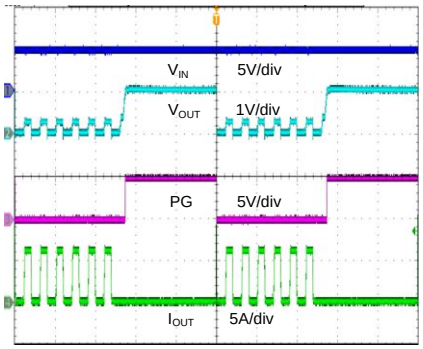
(Output Discharge=1, V_{IN}=5V, V_{OUT}=1V, I_{OUT}=0A, EN pin is high)



Time(10ms/div)

Short Circuit Protection

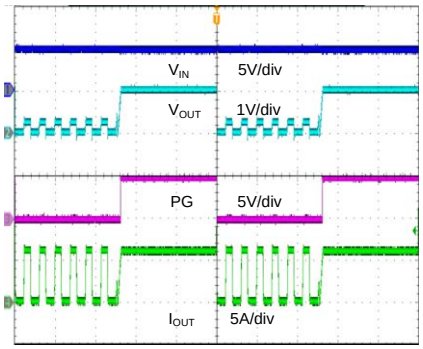
(V_{IN}=5V, V_{OUT}=1V, I_{OUT}=0A)



Time(4ms/div)

Short Circuit Protection

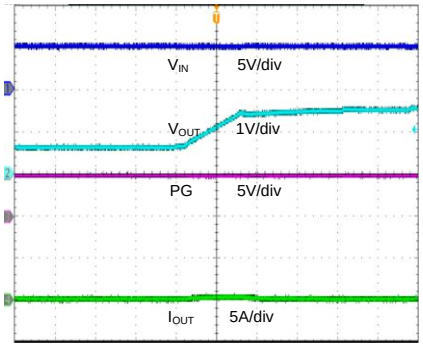
(V_{IN}=5V, V_{OUT}=1V, I_{OUT}=6A)



Time(4ms/div)

Dynamic Voltage Scale

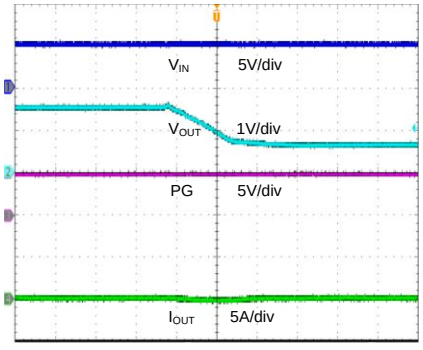
(Slew Rate=000, V_{IN}=5V, V_{OUT}=0.6-1.5V, I_{OUT}=0A)



Time(10μs/div)

Dynamic Voltage Scale

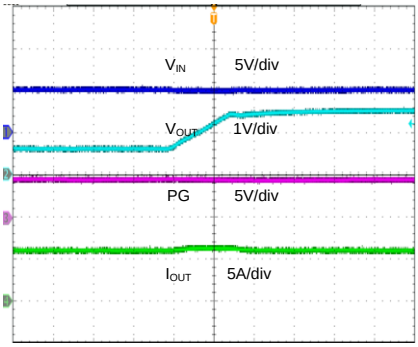
(Slew Rate=000, V_{IN}=5V, V_{OUT}=1.5-0.6V, I_{OUT}=0A)



Time(10μs/div)

Dynamic Voltage Scale

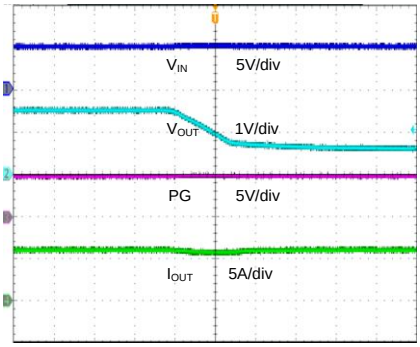
(Slew Rate=000, V_{IN}=5V, V_{OUT}=0.6-1.5V, I_{OUT}=6A)



Time(10μs/div)

Dynamic Voltage Scale

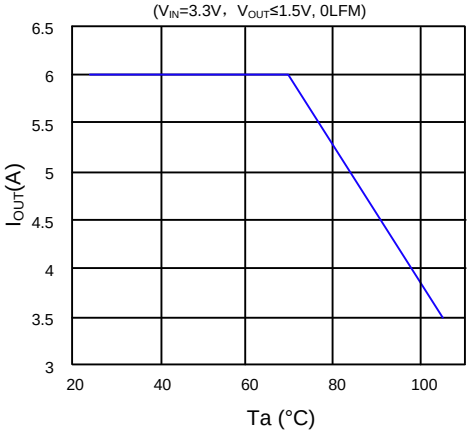
(Slew Rate=000, V_{IN}=5V, V_{OUT}=1.5-0.6V, I_{OUT}=6A)



Time(10μs/div)

Thermal Derating Curve

(V_{IN}=3.3V，V_{OUT}≤1.5V, 0LFM)



Note:

1) TA: Air temperature, 0.5 inch above the IC.

2) Based on a Two-layer Silergy evaluation board in the natural convection.

3) The IC case temperature is not beyond 115°C under this TD curve.

4) For customer's specific application, the recommended the IC case temperature limitation is 115°C.

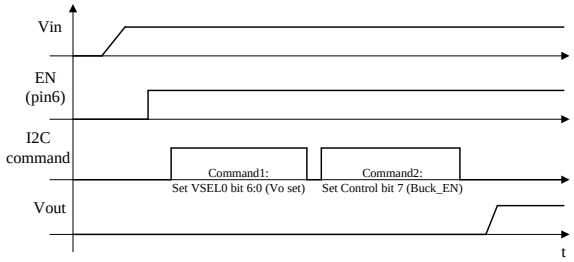
Enabling Function

The EN pin controls the SY20616D's start-up. EN pin low to high transition starts the power-up sequencer. If EN pin is low, the DC/DC converter will be turned off, and all I²C registers will be reset to default values, and the I²C command will not be supported at this state.

When the EN pin is HIGH, the SY20616D's output can be controlled by the I²C register BUCK_EN bit.

Hardware and Software Enable control table.

Pin	I²C register	OUTPUT
EN	BUCK_EN	
0	x	OFF
1	0	OFF
1	1	ON



Input Over Voltage Protection Function

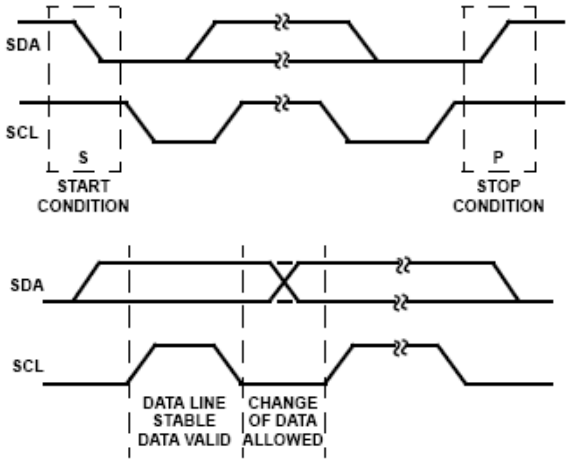
When the V_{IN} exceeds over voltage protection threshold, SY20616D will stop switching to protect the circuitry. An internal 10us blanking time filter helps to prevent the circuit from shutting down due to noise spikes.

I²C Interface

The SY20616D features an I²C interface that allows the HOST processor to control the output voltage to achieve the DVS function. The I²C interface supports clock speeds up to 1.0MHz and uses standard I²C commands. The SY20616D always operates as a slave device, and is addressed using a 7-bit slave address followed by an 8-bit, which indicates whether the transaction is a read-operation or a write-operation.

START and STOP Conditions

The SY20616D is controlled via an I²C compatible interface. The START condition is a HIGH to LOW transition on the SDA line while the SCL is HIGH. The STOP condition is a LOW to HIGH transition on the SDA line while the SCL is HIGH. A STOP condition must be sent before each START condition. The I²C master always generates the START and STOP conditions.

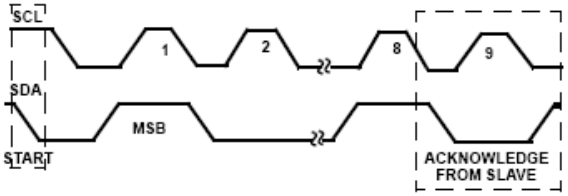


Data Validity

The data on the SDA line must be stable during the HIGH period of the SCL, unless generating a START or STOP condition. The HIGH or LOW state of the data line can only be changed when the clock signal on the SCL line is LOW.

Acknowledge

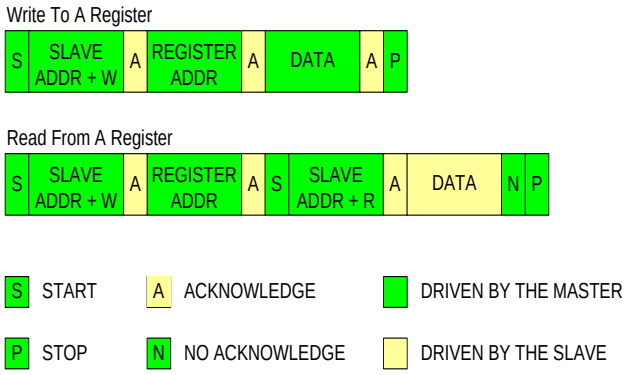
Each address and data transmission uses 9-clock pulses. The ninth pulse is the acknowledge bit (ACK). After the START condition, the master sends 7-slave address bits and an R/W bit during the next 8-clock pulses. During the ninth clock pulse, the device that recognizes its own address holds the data line low to acknowledge. The acknowledge bit is also used by both the master and the slave to acknowledge receipt of register addresses and data.



Data Transactions

All transactions start with a control byte sent from the I²C master device. The control byte begins with a START condition, followed by 7-bit of slave address (1100000x) for the SY20616D (this address can be changed if necessary), and followed by the 8th bit, R/W bit. The R/W bit is 0 for a write or 1 for a read. If any slave devices on the I²C bus recognize their address, they will be acknowledged by pulling the SDA line low for the last clock cycle in the control byte. If no

slaves exist at that address or are not ready to communicate, the data line will be 1, indicating a Not Acknowledge condition. Once the control byte is sent, and the SY20616D acknowledges it, the 2nd byte sent by the master must be a register address byte. The register address byte tells the SY20616D which register the master will write or read. The SY20616D will response once it receives a register.



Register Settings:

1. VSEL0 (0×00)

Register Name				VSEL0
Address				0×00
Field	**Bit**	**R/W**	**Default**	**Description**
Reserved	7	R/W	0	Always reads back 0.
NSEL	6:0	R/W	0101000 (V_{OUT}=1.00V)	0000000 = 0.60V …… 0011111= 0.91V …… 1011010=1.50V …… 1111111=1.50V

2. Control Register (0×01)

Register Name				Control Register
Address				0×01
Field	**Bit**	**R/W**	**Default**	**Description**
BUCK_EN	7	R/W	0	Software buck enable. When EN pin is low, the regulator is off. When EN pin is high, Buck EN bit must be written as 1 to enable SY20616D.
MODE0	6	R/W	0	0=Allow auto-PFM mode during light load. 1=Forced PWM mode
Output Discharge	5	R/W	0	0 = discharge resistor is disabled. 1 = discharge resistor is enabled.
Slew Rate	4:2	R/W	000=10mV/0.15μs	Set the slew rate for positive voltage transitions. 000 = 10mV/0.15μs 001 = 10mV/0.3μs 010 = 10mV/0.6μs

				011 = 10mV/1.2μs 100 = 10mV/2.4μs 101 = 10mV/4.8μs 110 = 10mV/9.6μs 111 = 10mV/19.2μs
RESET	1	R/W	0	Setting to 1 resets all registers to default values.
Reserved	0	R/W	0	Always reads back 0.

3. Power Good Register (0×02)

Register Name				PGOOD Register
Address				0×02
Field	**Bit**	**R/W**	**Default**	**Description**
PGOOD	7	R	0	1: Buck is enabled and soft-start is completed.
Reserved	6:0	R	000 0000	Always reads back 0.

Application Information

Because of the high integration in the SY20616B, the application circuit based on this regulator is rather simple. Only the input capacitor C_{IN} and the output capacitor C_{OUT} need to be selected for the targeted applications specifications. And X7R or better grade ceramic capacitors with low ESR are recommended for reliable operation.

External capacitor recommendation

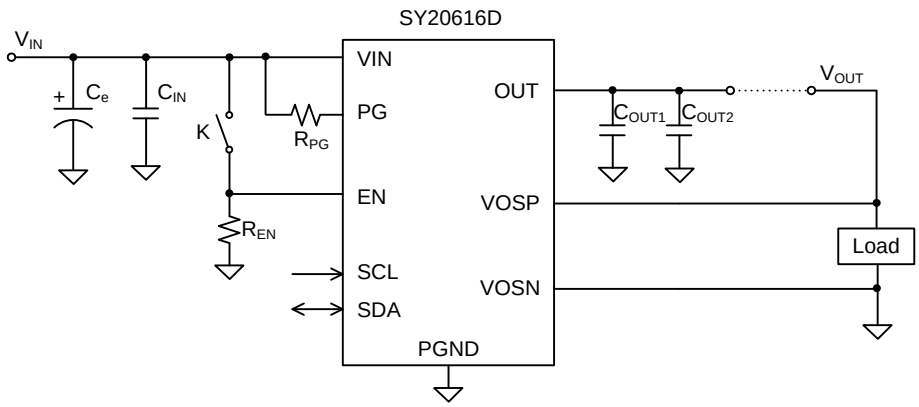
	Capacitance	Vendor	PN
C_{IN}	22μF	muRata	GRM31CC71C226 ME11
C_{OUT}	2×22μF	muRata	GRM31CC71C226 ME11

Layout Design

To achieve a higher efficiency and better noise immunity, following components should be placed close to the IC: C_{IN}, C_{OUT}.

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. Reasonable vias are suggested to be placed underneath the ground pad to enhance the soldering quality and thermal performance.
2) The decoupling capacitor of VIN/VOUT and GND must be placed close enough to the pins. The loop area formed by the capacitors and GND must be minimized.
3) The PCB copper area associated with LX pin must be minimized to improve the noise immunity.

Typical Application Circuit



BOM List

Reference Designator	Description	Part Number	Manufacturer
C_e	470μF/16V Electrolytic Capacitor		
C_{IN}	22μF/16V/X7S, 1206	GRM31CC71C226ME11	muRata
C_{OUT1},C_{OUT2}	22μF/16V/X7S, 1206	GRM31CC71C226ME11	muRata
R_{PG}	1MΩ, 1%, 0603		
R_{EN}	1MΩ, 1%, 0603		

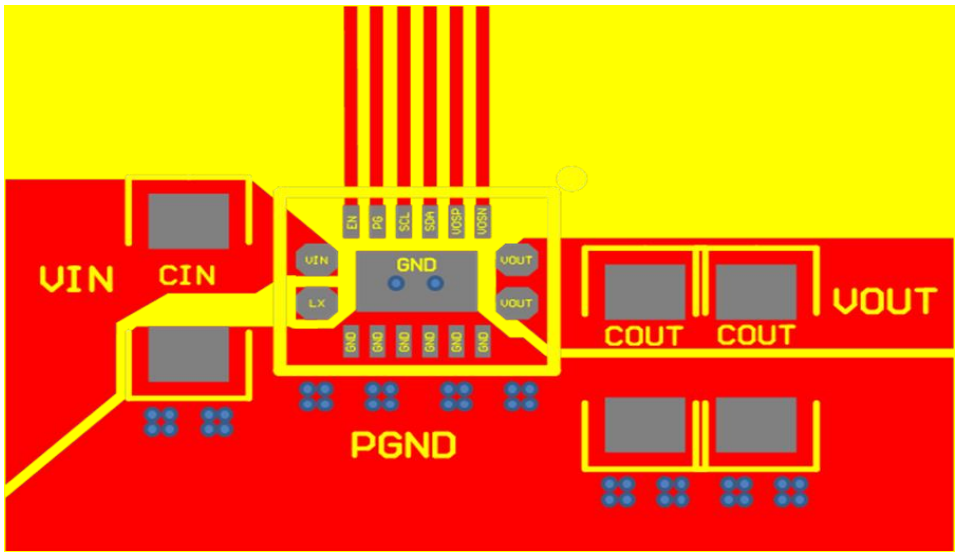
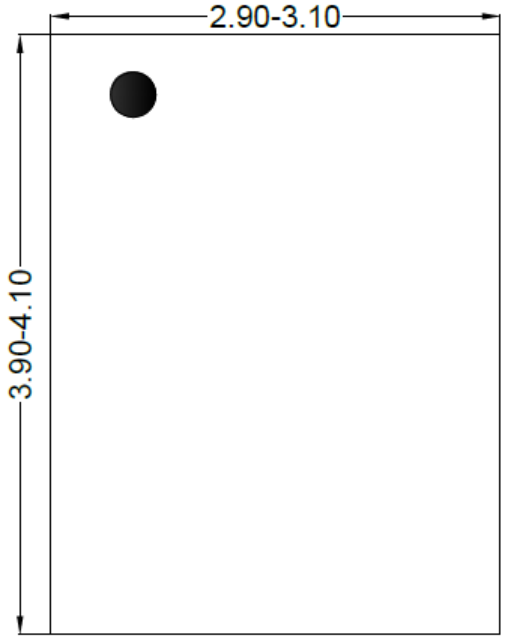
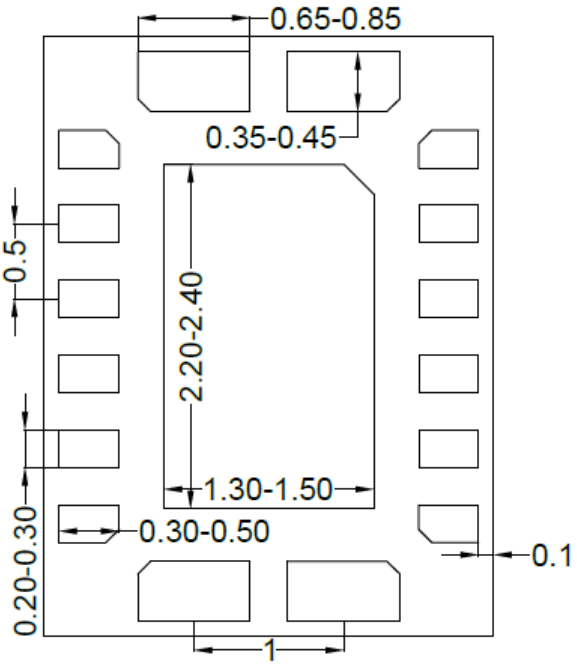


Figure3.PCB Layout Suggestion

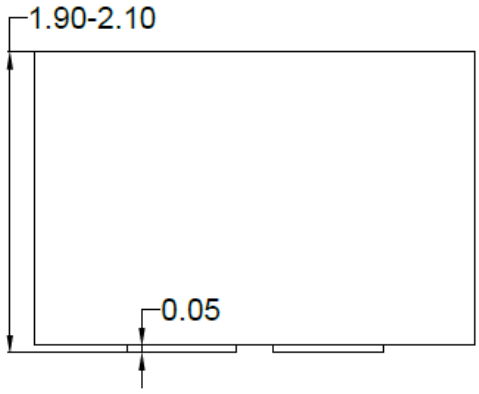
MQFN3×4-16 Package Outline Drawing



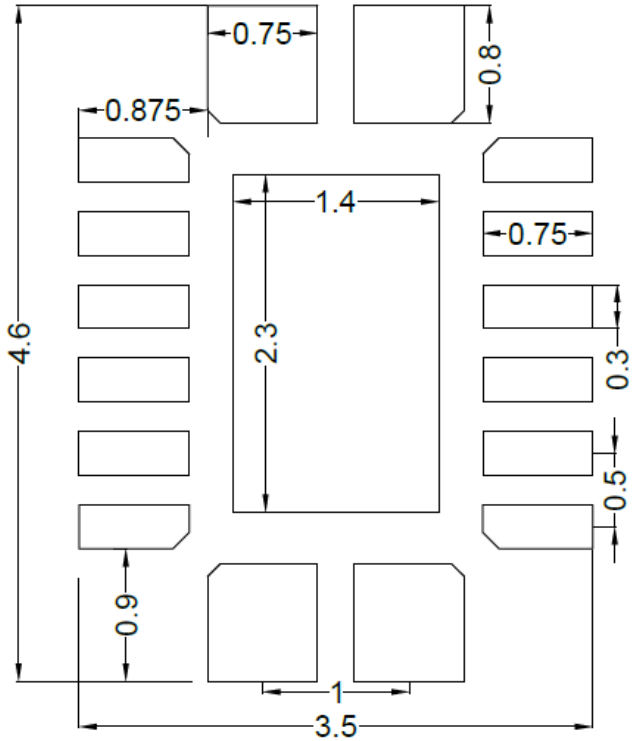
Top view



Bottom view



Side view

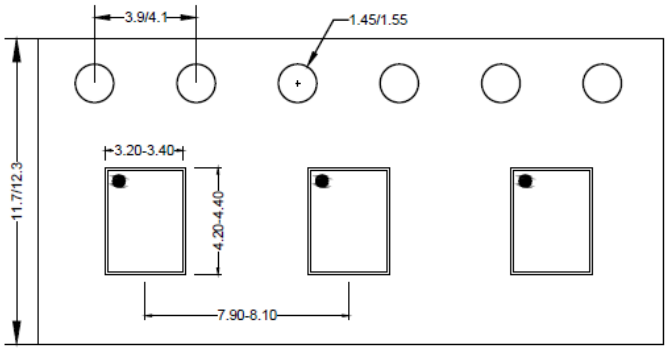


Recommended PCB layout
(Reference only)

Taping & Reel Specification

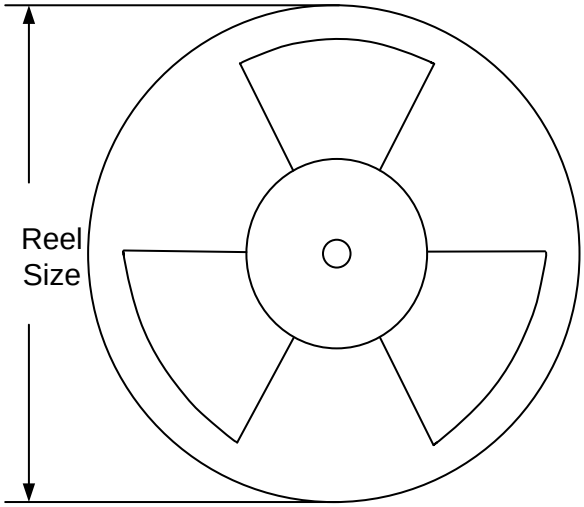
1. Taping orientation

MQFN3×4



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
MQFN3×4	12	8	13"	400	400	2500

3. Others: NA

IMPORTANT NOTICE

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