SY28902

IEEE 802.3bt PD Interface Controller

General Description

The SY28902 is a power device (PD) controller with all the features needed to implement the IEEE802.3at/at/bt protocol. It integrates a multi-state $\overline{T2P}$ output indicator to indicate the number of classification events received during IEEE 802.3bt-compliant identification and negotiation of available power.

An internal charge-pump is used for enabling the use of external low $R_{DS(ON)}$ N-channel MOSFETs and increase the end-to-end power transmission efficiency. The SY28902 includes an integrated signature resistor, under-voltage lockout, a power-good output and thermal protection. The start-up inrush current can be adjusted using an external capacitor. Auxiliary power override is supported for voltages higher than 9V applied to the AUX pin.

802.3bt, 802.3at, and 802.3af power levels are all supported by configuring external components.

The SY28902 is available in a 3mm x 3mm MSOP10 package.

Features

- IEEE 802.3af/at/bt Powered Device (PD) Solution for Type 1-4 PoE Applications
- Supports up to 71.3W PDs
- Supports up to 5-Event Classification Sensing
- 100V Robust Surge Protection (Abs. Max.)
- Integrated Signature Resistor
- Thermal Shutdown Protection
- External Hot-swap N-Channel MOSFET for Lowest Power Dissipation and Highest System Efficiency
- Configurable AUX Power Support as Low as 9V
- –40℃ to 125℃Junction Temperature Range

Applications

- Security Cameras
- Base Stations
- IEEE 802.3bt Compliant Devices
- Video and VoIP Telephones
- Industrial Applications

Typical Application

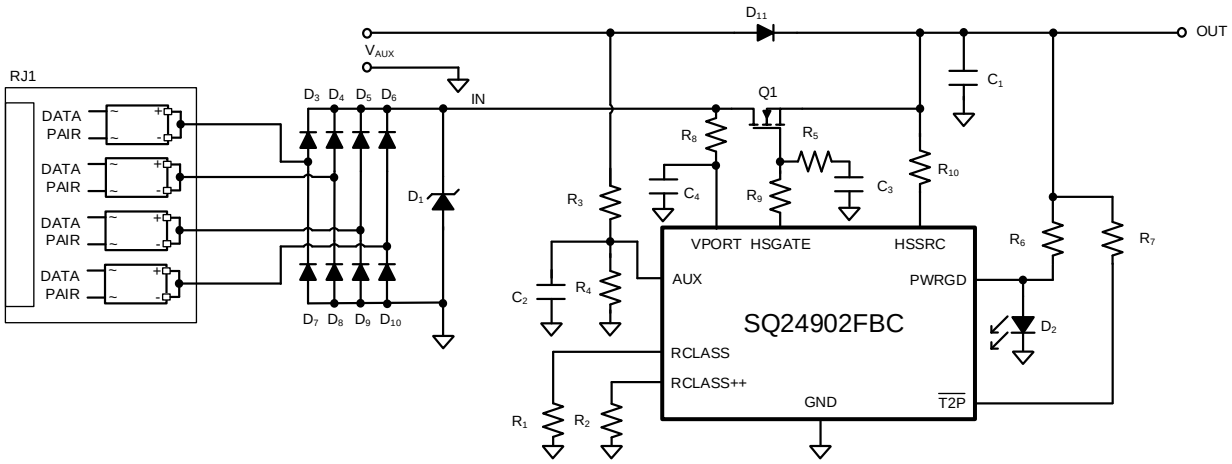

Figure 1. Schematic Diagram

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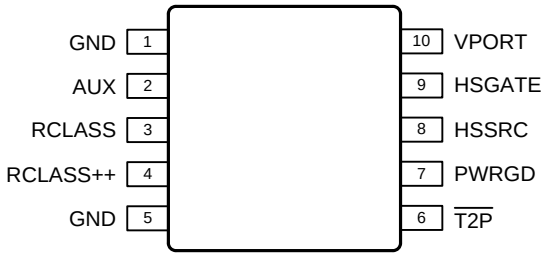
Ordering Information

Ordering Part Number	Package Type	Top Mark
SY28902FBC	MSOP10 RoHS Compliant and Halogen Free	**CXW*xyz***

x=year code, y=week code, z= lot number code

Pinout (top view)



Pinout Description

Pin Name	NO.	TYPE	Pin Description
GND	1,5	-	Device ground.
AUX	2	I	Auxiliary sense pin. Connect a resistive divider from the auxiliary power input to AUX to configure the voltage at which the auxiliary supply takes over. In auxiliary power operation, HSGATE is pulled down, the signature resistor disconnects, classification is disabled, the PWRGD pin is high impedance and $\overline{T2P}$ indicates the maximum available power. Connect to GND when not used.
RCLASS	3	O	Configurable PoE classification resistor.
RCLASS++	4	O	Configurable PoE classification resistor.
$\overline{T2P}$	6	O	PSE type indicator: Open-drain output.
PWRGD	7	O	Power good indicator: Open-drain output. Pulled to GND during V_{CLASS} and inrush stages.
HSSRC	8	I	External hot-swap MOSFET source. Connect to the source of the external MOSFET.
HSGATE	9	O	External hot-swap MOSFET gate control output. Connect to the gate of the external MOSFET.
VPORT	10	I	PD interface upper power rail and external hot-swap MOSFET drain connection.

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Block Diagram

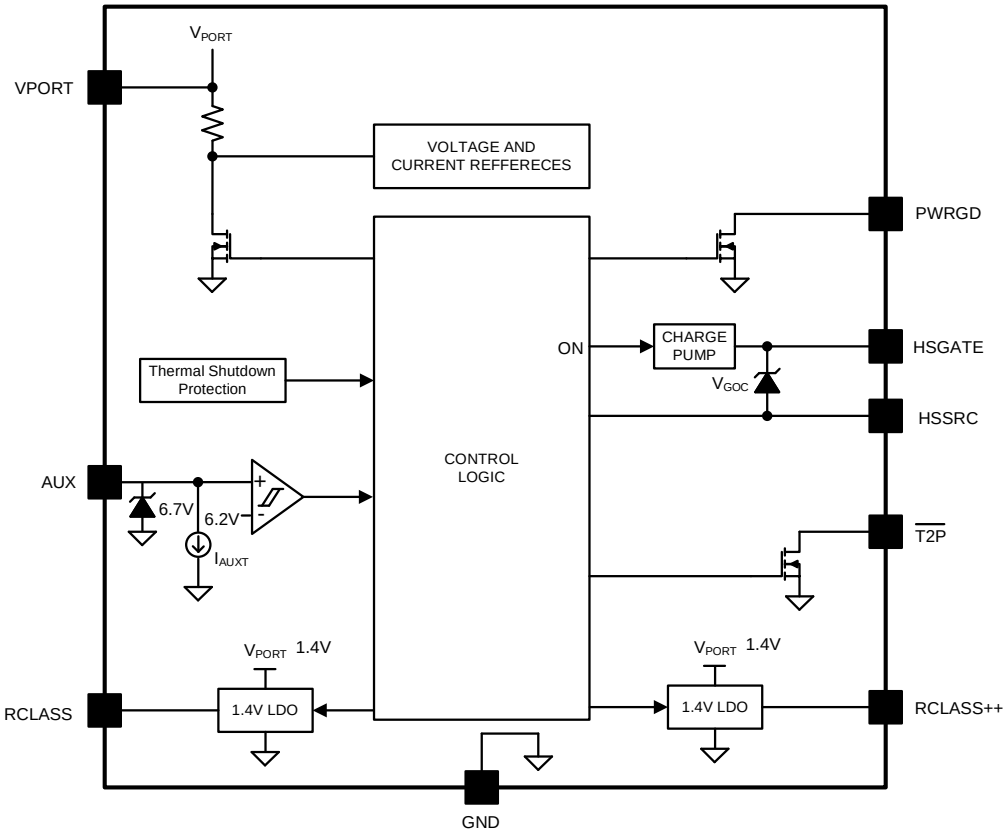

Figure 2. Block Diagram

Absolute Maximum Ratings

Parameter (Note1) (Note4)	Min	Max	Unit
VPORT, HSSRC, HSGATE, $\overline{T2P}$, PWRGD	-0.3	100	V
HSGATE to HSSRC	V_{HSSRC}-0.2	V_{HSSRC} +14	
RCLASS, RCLASS++	-0.3	6 (and ≤ VPORT)	
HSGATE Current	-20	20	mA
AUX Current	-1.4	1.4	
$\overline{T2P}$, PWRGD Current		5	
Junction Temperature, Operating	-40	125	°C
Lead Temperature (Soldering, 10sec.)		300	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note2)	Typ	Unit
θ_{JA} Junction-to-ambient Thermal Resistance	135.2	°C/W
θ_{JC} Junction-to-case Thermal Resistance	25	
P_D Power Dissipation T_A=25°C	0.74	W

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Recommended Operating Conditions

Parameter (Note5)	Min	Max	Unit
VPORT, HSSRC	0	60	V
HSGATE to HSSRC	V_{HSSRC}	V_{HSSRC} +14	
RCLASS, RCLASS++	0	5 (and ≤ VPORT)	
Ambient Temperature	-40	125	°C

Electrical Characteristics

Unless otherwise noted: –40℃≤ T_J ≤125℃. (Note4)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VPORT Operating Input Voltage		At VPORT pin			60	V
VPORT Signature Range	V_{SIG}	At VPORT pin	1.5		10	V
VPORT Classification Range	V_{CLASS}	At VPORT pin	12.5		21	V
VPORT Mark Range	V_{MARK}	At VPORT pin, preceded by V_{CLASS}	5.6		10	V
VPORT AUX Mode Range		At VPORT pin, AUX > V_{AUXT}	8		60	V
Signature/Class Hysteresis Window			1.0			V
Reset Threshold	V_{RESET}	At VPORT pin, preceded by V_{CLASS}	2.6		5.6	V
Power Good Threshold	V_{PG_TH}		7.1	8	8.9	V
Hot-swap Turn-on Voltage	V_{HSON}			35	37	V
Hot-swap Turn-off Voltage	V_{HSOFF}		30	31		V
Hot-swap On/Off Hysteresis Window			3			V
Supply Current						
Supply Current		V_{VPORT}=V_{HSSRC}=57V			1	mA
Supply Current During Classification		V_{VPORT} = 17.5 V, RCLASS and RCLASS++ open	0.1	0.2	0.5	mA
Supply Current During Mark Event		V_{VPORT}=V_{MARK} after 1st classification event	0.5		1.8	mA
Detection and Classification Signature						
Detection Signature Resistance		V_{SIG} (Note 3)	23.7	24.4	25.2	kΩ
Resistance During Mark Event		V_{MARK} (Note 3)	5.8	8.3	11	kΩ
RCLASS/RCLASS++ Operating Voltage		–10mA ≥ I_{RCLASS} ≥ –36mA, V_{CLASS}	1.32	1.40	1.43	V
Classification Signature Stability Time		V_{VPORT} Step to 17.5V, 34.8Ω from RCLASS or RCLASS++ to GND			2	ms
Analog/Digital Interface						
AUX Threshold	V_{AUXT}		6	6.2	6.4	V
AUX Hysteresis	$V_{AUX,HYS}$			0.4		V
AUX Pin Hysteresis Current	I_{AUXT}	V_{AUX} = 6.1V	0.8	2.1	4	µA
$\overline{T2P}$ Output Low		1mA Load			0.8	V
PWRGD Output Low		1mA Load			0.8	V
PWRGD Leakage Current		V_{PWRGD} = 60V			5	µA
$\overline{T2P}$ Leakage Current		$\overline{T2P}$ = 60V			5	µA
Hot-swap Control						
HSGATE Pull-up Current	I_{GPU}	V_{HSGATE} - V_{HSSRC} = 5V (Note 7)	-27	-22	-18	µA
HSGATE Open Circuit Voltage	V_{GOC}	-10µA Load, with Respect to HSSRC	10		17	V

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
HSGATE Pull-down Current		V_{HSGATE} - V_{HSSRC} = 5V	200			μA
Timing						
$\overline{T2P}$ Frequency	f_{T2P}	After PWRGD valid, if IEEE802.3bt PSE is mutually identified	690	840	990	Hz
$\overline{T2P}$ Duty Cycle in PoE Operation (Note 6)		After 4-event Classification		50		%
		After 5-event Classification (RCLASS++ has resistor to GND) at T_A = 25°C.		25		%
$\overline{T2P}$ Duty Cycle in Auxiliary Supply Operation (Note 6)		V_{AUX} > V_{AUXT}, and RCLASS++ has resistor to GND at T_A = 25°C.		25		%

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on the Silergy EVB test board of JEDEC 51-3 thermal measurement standard.

Note 3: Signature resistance specifications do not include resistance added by the external diode bridge, which can add as much as 1.1k to the port resistance.

Note 4: All voltages with respect to GND unless otherwise noted. Positive currents are into pins; negative currents are out of pins unless otherwise noted.

Note 5: This IC includes over-temperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 150°C when over-temperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 6: Specified as the percentage of the period which $\overline{T2P}$ is low impedance with respect to GND.

Note 7: I_{GPU} available in PoE-powered operation. That is, available after V_{VPORT} > V_{HSON} and V_{AUX} < V_{AUXT}, over the range where V_{VPORT} is between V_{HSOFF} and 60V.

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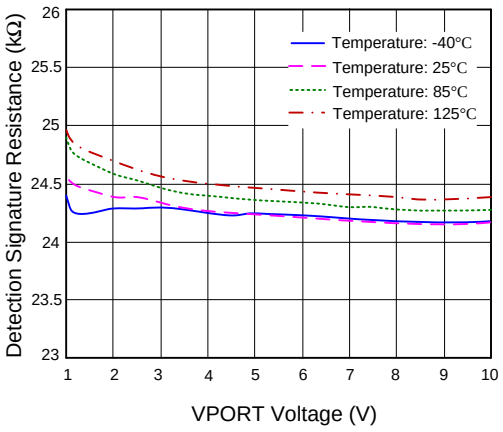
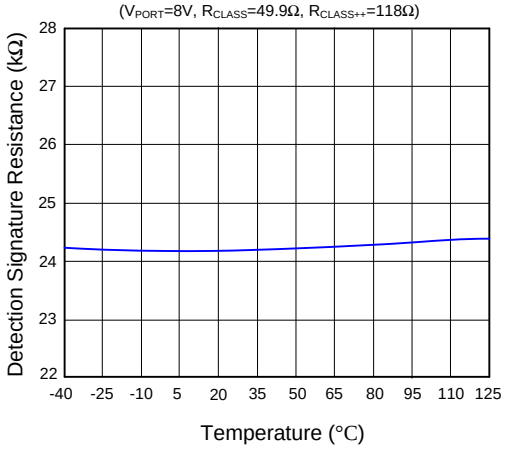
Typical Performance Characteristics

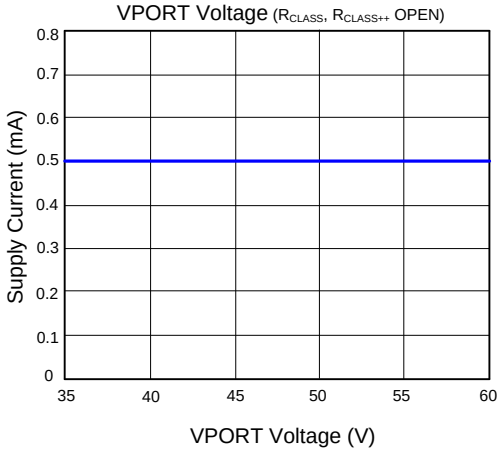
Detection Signature Resistance vs. VPORT Voltage



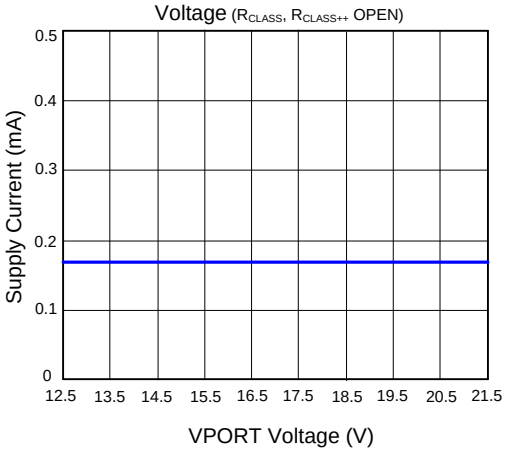
Detection Signature Resistance vs. Temperature
(V_{PORT}=8V, R_{CLASS}=49.9Ω, $R_{CLASS++}$=118Ω)



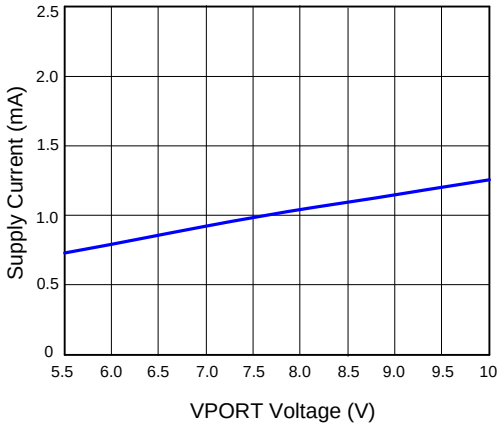
Supply Current during PWRFET Turn on vs. VPORT Voltage (R_{CLASS}, $R_{CLASS++}$ OPEN)



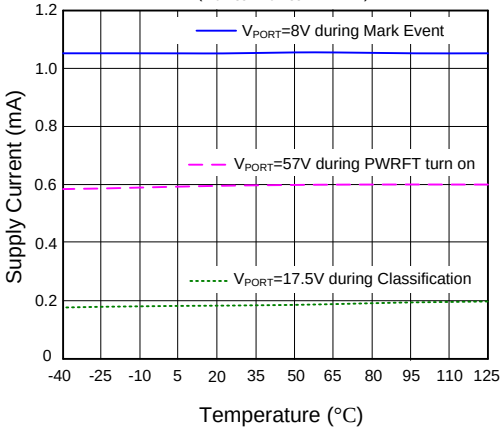
Supply Current during Classification vs. VPORT Voltage (R_{CLASS}, $R_{CLASS++}$ OPEN)



Supply Current during Mark Event vs. VPORT Voltage (R_{CLASS}, $R_{CLASS++}$ OPEN)



Supply Current vs. Temperature
(R_{CLASS}, $R_{CLASS++}$ OPEN)



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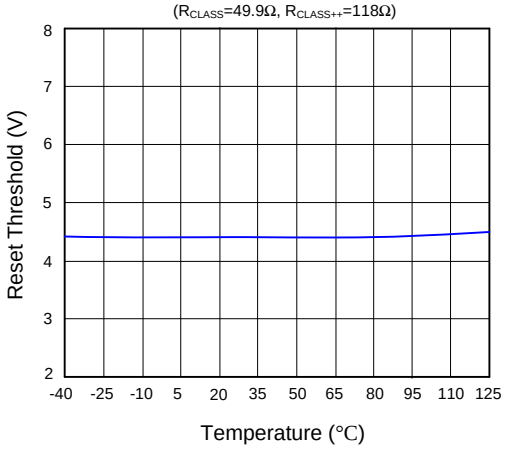
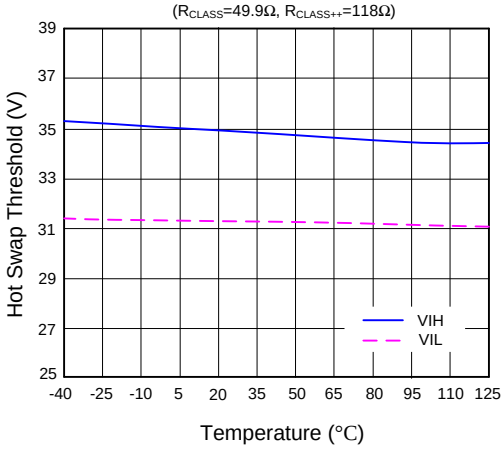
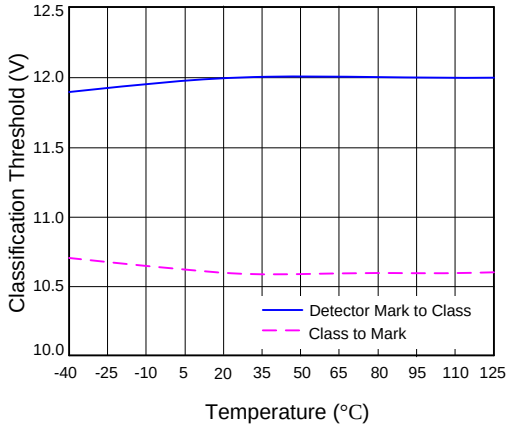
Reset Threshold vs. Temperature
(R_{CLASS}=49.9Ω, $R_{CLASS++}$=118Ω)



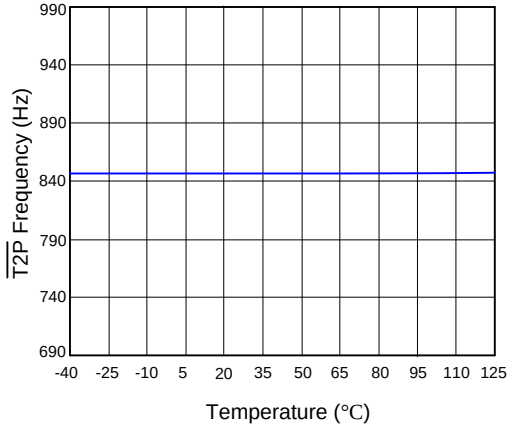
Hot Swap Threshold vs. Temperature
(R_{CLASS}=49.9Ω, $R_{CLASS++}$=118Ω)



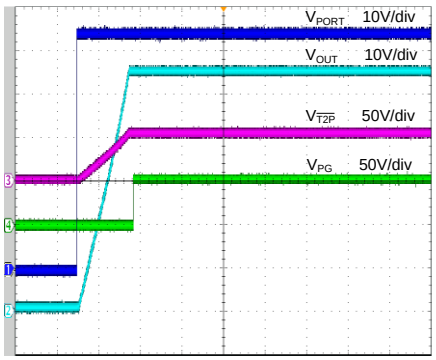
Classification Threshold vs. Temperature
(R_{CLASS}=49.9Ω, $R_{CLASS++}$=118Ω)



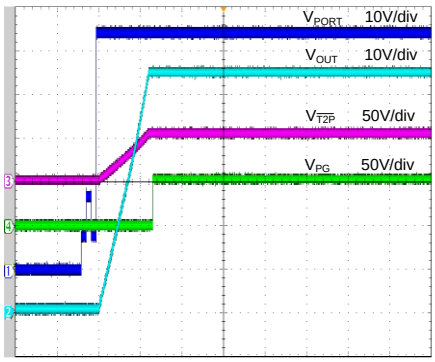
$\overline{T2P}$ Frequency vs. Temperature



Event 0 Operation Test
(V_{PORT}=0→54V, V_{AUX}=0V, R_{CLASS}=49.9Ω, $R_{CLASS++}$=118Ω)



Event 1 Operation Test
(V_{PORT}=0→8V→17.5V→8V→54V, V_{AUX}=0V, R_{CLASS}=49.9Ω, $R_{CLASS++}$=118Ω)



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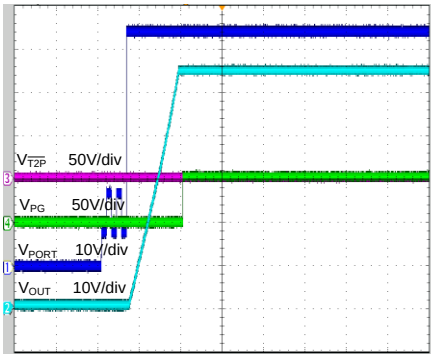
Event 2 Operation Test

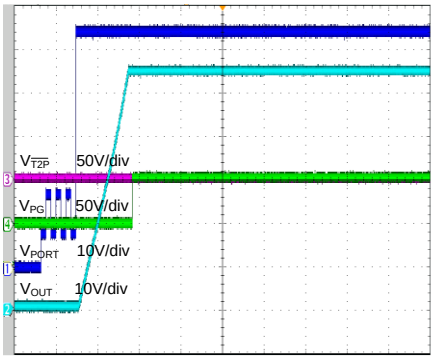
(V_{PORT}=0→8V→(17.5V→8V)$_2$→54V, V_{AUX}=0V, R_{CLASS}=49.9Ω, $R_{CLASS++}$=118Ω)



Time (100ms/div)

Event 3 Operation Test

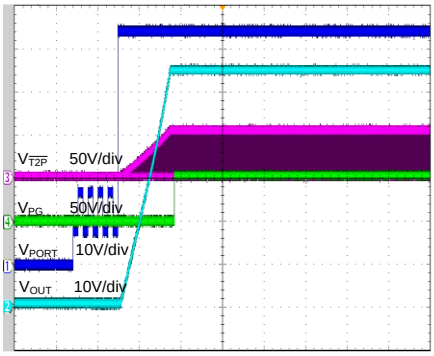
(V_{PORT}=0→8V→(17.5V→8V)$_3$→54V, V_{AUX}=0V, R_{CLASS}=49.9Ω, $R_{CLASS++}$=118Ω)



Time (100ms/div)

Event 4 Operation Test

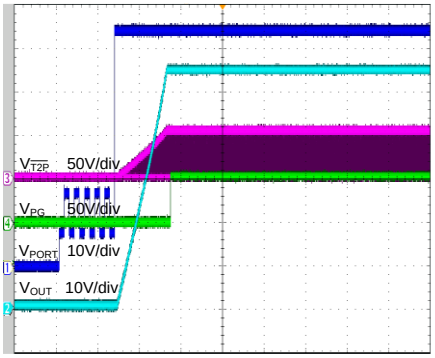
(V_{PORT}=0→8V→(17.5V→8V)$_4$→54V, V_{AUX}=0V, R_{CLASS}=49.9Ω, $R_{CLASS++}$=118Ω)



Time (100ms/div)

Event 5 Operation Test

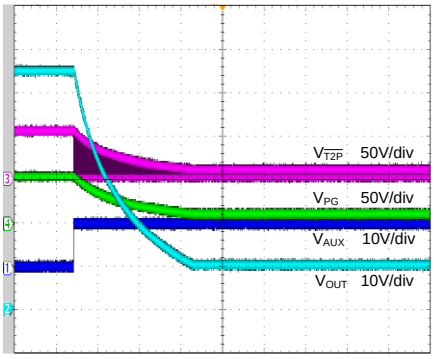
(V_{PORT}=0→8V→(17.5V→8V)$_5$→54V, V_{AUX}=0V, R_{CLASS}=49.9Ω, $R_{CLASS++}$=118Ω)



Time (100ms/div)

AUX ON

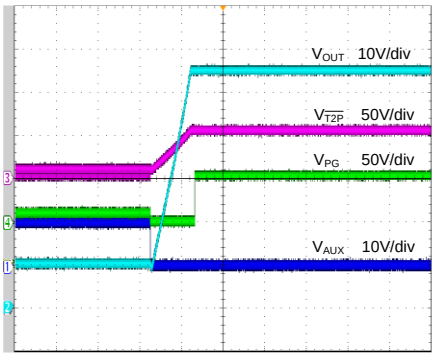
(V_{PORT}=54V, V_{AUX}=0→10V, R_{CLASS}=49.9Ω, $R_{CLASS++}$=118Ω)



Time (100ms/div)

AUX OFF

(V_{PORT}=54V, V_{AUX}=10→0V, R_{CLASS}=49.9Ω, $R_{CLASS++}$=118Ω)



Time (100ms/div)

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Application Information

Overview

The IEEE 802.3af/at/bt specification defines a process for safely powering a PD over a cable and removing power if a PD is disconnected. The process proceeds through three operational states: detection, classification, and operation.

The SY28902 is a power device controller containing all the features needed to implement an IEEE802.3at/at/bt protocol. It integrates the $\overline{T2P}$ output indicator to show the number of classification events received during IEEE 802.3bt-compliant mutual identification and negotiation of available power. To eliminate expensive heat sinks, the SY28902 uses external low $R_{DS(ON)}$ N-channel hot-swap MOSFET to extend end-to-end power transmission efficiency.

Modes of Operation

Detection Signature

When a voltage in the range of 2.7V to 10.1V is applied to the PI, a signature resistance of 25 kΩ signals the Power Supply Equipment (PSE) that the PD is capable of accepting power. Figure 3 shows the detection voltages of the PSE. The PSE calculates the signature resistance using a ΔV/ΔI measurement technique.

The SY28902 integrates a temperature-compensated, precision 24.4k signature resistor between the VPORT and GND pins. The PSE requests power to be applied if a valid PD is recognized. Typically, the SY28902 signature resistor is smaller than 25k to compensate for the additional series resistance on the line.

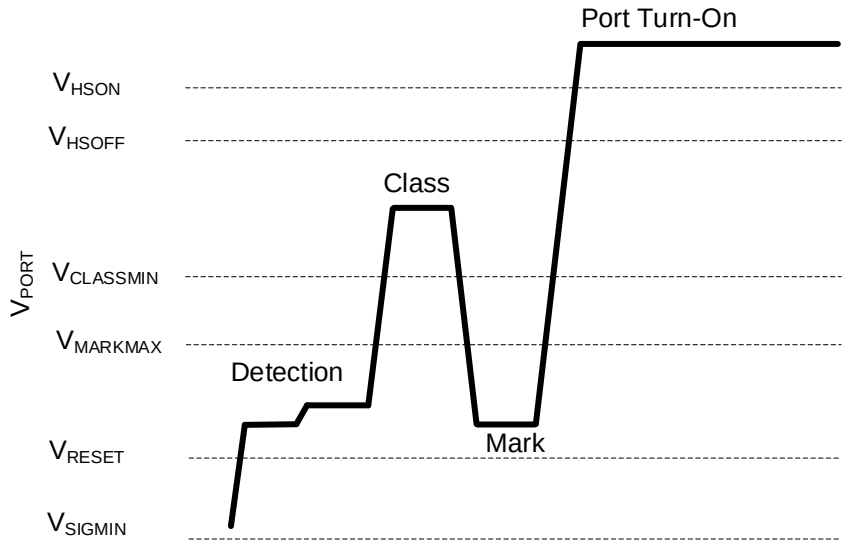

Figure 3. Type 1 PSE, 1-Event Class Sequence

IEEE 802.3bt Single-Signature vs. Dual-Signature PDs

Although PD signature configuration is not defined for Type 1 and Type 2 PDs, a Type 3 or Type 4 PSE may identify such a PD as single-signature or dual-signature. The SY28902 is a single-signature PD that may receive 4-pair power regardless of the PD type, eliminating the additional cost of the second PD controller.

Classification Signature and Mark

The SY28902 may optionally provide a classification signature to the PSE, indicating the maximum power it will draw during operation. The IEEE specification defines this signature as a constant current draw when the PSE port voltage is in the V_{CLASS} range (between 14.5V and 20.5V). If the PSE applies a classification probe voltage, the PSE returns the PD voltage to the mark voltage range before applying another classification probe voltage or powering up the PD.

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An example of 1-Event classification is shown in Figure 3. In 2-Event classification, a PSE probes for power classification twice as shown in Figure 4. An IEEE 802.3bt PSE may apply as many as five events before powering up the PD.

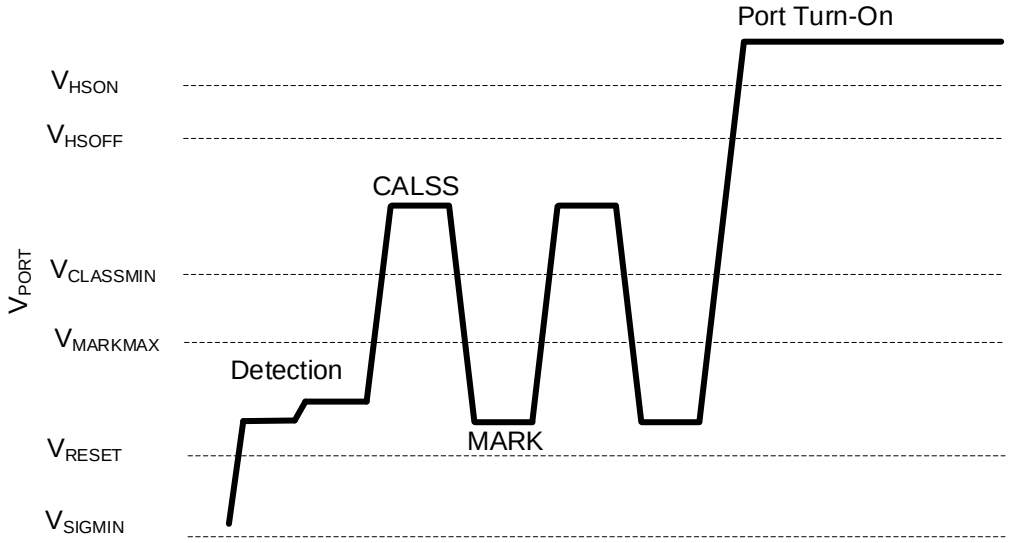

Figure 4. Type 2 PSE, 2-Event Class Sequence

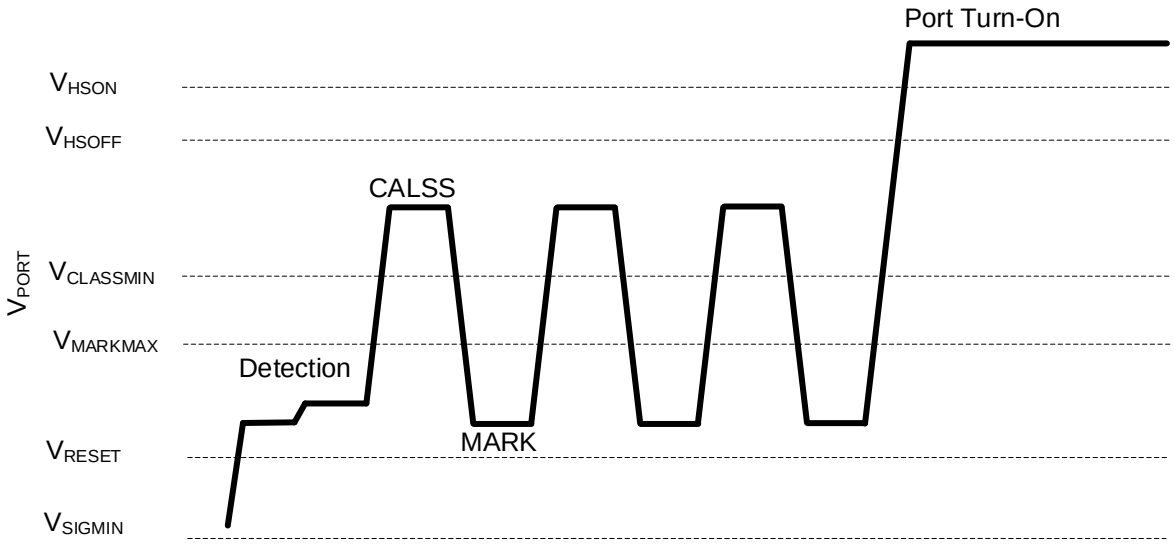

Figure 5. Type 3 or 4 PSE, 3-Event Class Sequence

IEEE 802.3bt Demotion and Physical Classification

IEEE 802.3 PSEs may demote PDs to a lower power state when PD requested power exceeds the PSE available power. IEEE 802.3bt defines physical classification to allow a PD to request a power allocation from the connected PSE and to allow the PSE to inform the PD of the PSE's available power.

As shown in Table 1, the number of class/mark events issued by the PSE directly indicates the power allocated to the PD.

IEEE 802.3bt provides nine PD classes and four PD types as shown in tables 1 and 2. The class of the SY28902 is configured by setting the R_{CLS} and R_{CLS++} resistor values.

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Table 1. PSE Allocated Class Power

PD REQUESTED CLASS	NUMBER OF PSE CLASS/MARK EVENTS				
	1	2	3	4	5
0	13W				
1	3.84W				
2	6.49W				
3	13W				
4	**13W**	25.5W			
5	**13W**	**25.5W**		40W	
6	**13W**	**25.5W**		51W	
7	**13W**	**25.5W**		**51W**	62W
8	**13W**	**25.5W**		**51W**	71.3W

Note: Bold indicates the PD has been demoted.

Table 2. Single-Signature Classification Codes, Power Levels and Resistor Selection

PD REQUESTED CLASS	PD POWER AVAILABLE	PD TYPES	NOMINAL CLASS CURRENT	RESISTOR(1%)	
				R_{CLS}	R_{CLS++}
0	13W	Type 1	2.5mA	1.00kΩ	Open
1	3.84W	Type 1 or 3	10.5mA	140Ω	Open
2	6.49W	Type 1 or 3	18.5mA	76.8Ω	Open
3	13W	Type 1 or 3	28mA	49.9Ω	Open
4	25.5W	Type 2 or 3	40mA	34.8Ω	Open
5	40W	Type 3	40mA/2.5mA	1.00kΩ	37.4Ω
6	51W	Type 3	40mA/10.5mA	140Ω	46.4Ω
7	62W	Type 4	40mA/18.5mA	76.8Ω	64.9Ω
8	71.3W	Type 4	40mA/28mA	49.9Ω	118Ω

IEEE 802.3bt PSEs present 1-Event classification as shown in Figure 3 to Class 0 through 3 PDs. The PSE receives the class signature of a class 0-3 PD and then powers on if sufficient power is available. Power-limited IEEE 802.3bt PSEs may present 1-Event to Class 4 and higher PDs to demote those PDs to Class 3 (13W).

IEEE 802.3bt PSEs present up to 3-Events classification, according to PSE Type, to Class 4 PDs, as shown in Figure 5. Class 4 PDs present a class signature of 4 on all events. The third event distinguishes a Class 4 PD from a higher-class PD. Power-limited IEEE 802.3bt PSEs may issue 3-Events to Class 5 and higher PDs to demote those PDs to Class 4 (25.5W).

IEEE 802.3bt PSEs present up to 4-Events classification as shown in Figure 6 to Class 5 and 6 PDs. Class 5 and 6 PDs present a class signature of 4 on the first two events and then a class signature of 0 or 1, respectively, on the remaining events. Power-limited IEEE 802.3bt PSEs may issue 4-Events classification to Class 7 and higher PDs to demote those PDs to Class 6 (51W).

IEEE 802.3bt PSEs present up to 5-Events classification as shown in Figure 7 to Class 7 and 8 PDs. Class 7 and 8 PDs present a class signature of 4 on the first two events and then a class signature of 2 or 3, respectively, on the remaining events. The SY28902 communicates the PSE allocated power to the PD application via the $\overline{T2P}$ pin. Refer to the $\overline{T2P}$ Output section of the datasheet for more details.

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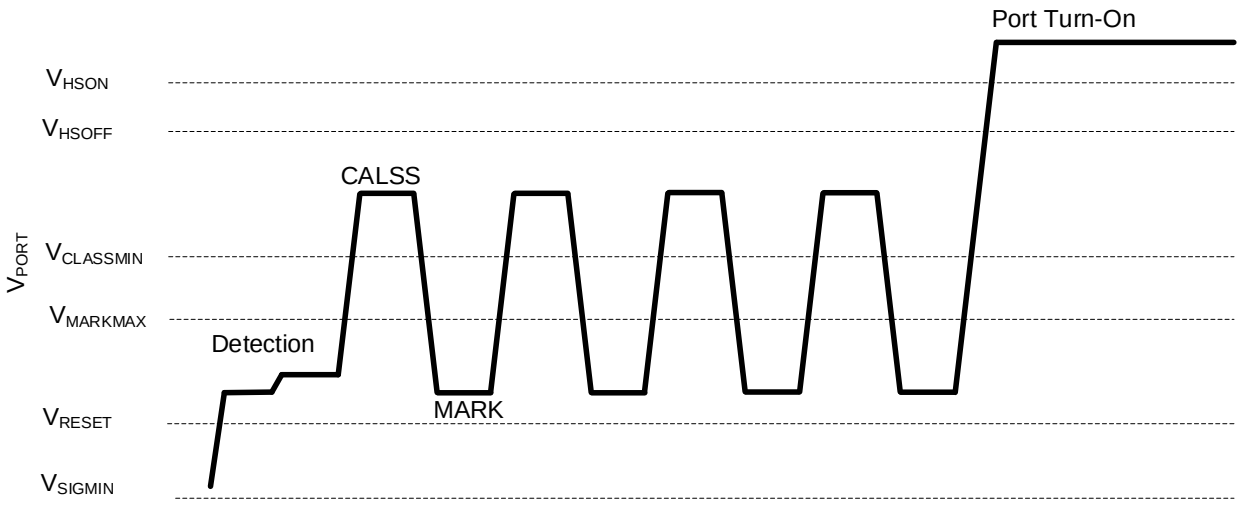

Figure 6. Type 3 or 4 PSE, 4-Event Class Sequence

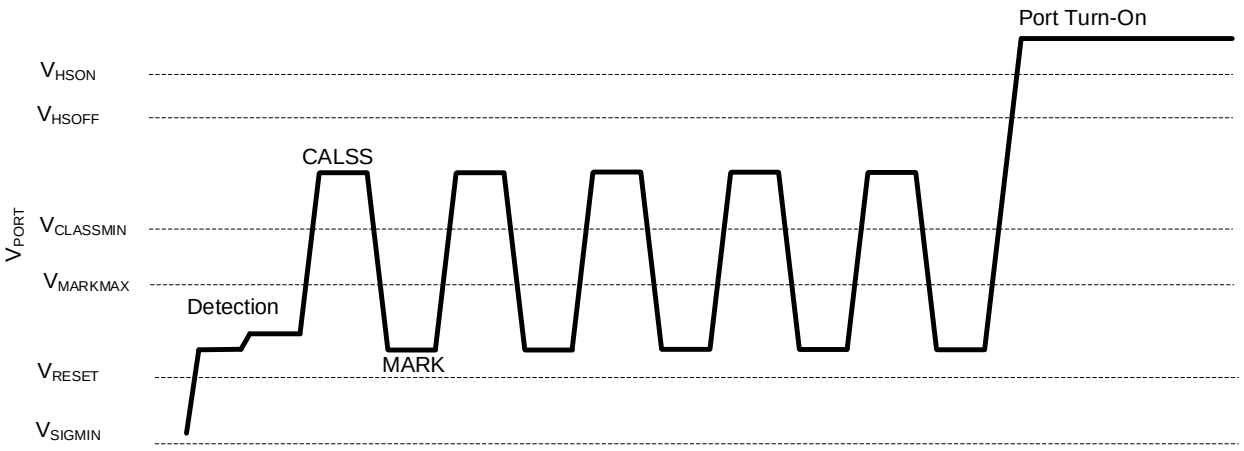

Figure 7. Type 4 PSE, 5-Event Class Sequence

Selection of Classification Resistors (R_{CLS} and R_{CLS++})

Select the value R_{CLS} and R_{CLS++} resistors to configure the corresponding classification currents according to Table 2 to select the PD power classification. Connect each 1% resistor between the R_{CLASS}, $R_{CLASS++}$ pins, and GND.

Detection Signature Corrupt During Mark Event

The SY28902 presents a resistance < 11kΩ to the port according to the requirements of the IEEE 802.3 specification.

Inrush Current and Power On

The PSE turns on the power to the PD once the PSE detects and classifies the PD. The SY28902 begins to source I_{GPU} out of the HSGATE pin when the port voltage rises above the V_{HSON} threshold. This current flows into an external capacitor C_{GATE}, shown in Figure 8, which causes the gate of the external MOSFET to rise. The external N-channel MOSFET acts as a source follower and causes the voltage ramp on the output bulk capacitor C_{OUT}, thereby determining the inrush current (I_{INRUSH}). A typical design target for I_{INRUSH} is approximately 100mA. The value for C_{GATE} can be calculated using the following equation:

$$I_{INRUSH} = I_{GPU} \frac{C_{OUT}}{C_{GATE}}$$

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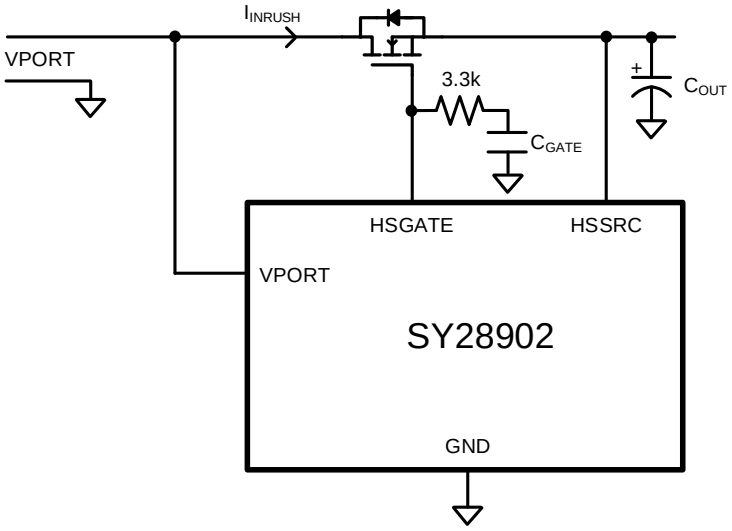

Figure 8. Configuring I_{INRUSH}

The SY28902 internal charge pump enables the use of N-channel MOSETs due to their lower cost and $R_{DS(ON)}$. Using a low $R_{DS(ON)}$ MOSFET maximizes power transmission efficiency, reduces power and heat dissipation, and simplifies thermal design.

Power Good Indicator

The PWRGD pin can be used for disabling the downstream circuits until the external MOSFET is fully biased and inrush time is complete. The PWRGD pin remains low until HSGATE is charged to approximately 8V above HSSRC. The HSGATE pin remains high, and the PWRGD pin is in high-impedance until the port voltage falls below V_{HSOFF}.

Auxiliary Supply Override

The SY28902 enters auxiliary power supply override mode if the AUX pin is held above V_{AUXT}. In this mode of operation, the signature resistor disconnects, HSGATE pulls down, classification is turned off, the PWRGD pin is high-impedance, and the $\overline{T2P}$ pin indicates maximum available power.

The AUX pin allows for setting the auxiliary supply turn on and turn off voltage thresholds, V_{AUXON}, and V_{AUXOFF}, respectively. Use the following equations to set V_{AUXON} and V_{AUXOFF} using the resistors R_1 and R_2 in (figure 9). Note that an internal 6.7V Zener limits the voltage on the AUX pin.

A capacitor of up to 1000pF may be placed between the AUX pin and the GND to improve noise immunity. V_{AUXON} must be lower than V_{HSOFF}.

$$V_{AUXON} = (\frac{R_1}{R_2} + 1)V_{AUXT} + I_{AUXT}R_1$$

$$V_{AUXOFF} = V_{AUXON} - (\frac{R_1}{R_2} + 1)V_{AUX\_HY}$$

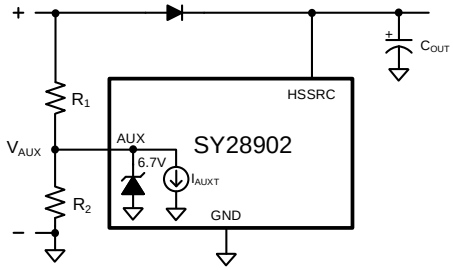

Figure 9. AUX Threshold and Hysteresis Calculation

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AUX Voltage Limit

If the AUX pin is driven above the internal Zener voltage threshold of 6.7V**,** the SY28902 will clamp the voltage to this level. For safe operation, the maximum current flowing into the AUX pin has to be lower than 1.4mA. Use a R_1 value higher than the resistance value calculated using the following equation:

$$R_1 \geq \frac{V_{AUX(MAX)} - 6.7V}{1.4mA}$$

PD Start Delay

The PD application should not exceed 350 mA within 80ms to meet the requirements of IEEE 802.3 standards when the PSE powers up the port.

$\overline{\text{T2P}}$ Output Indicator

The $\overline{\text{T2P}}$ pin state is determined by the number of classification events, the RCLASS++ pin, and the AUX pin and also depends on the PSE allocated power. The SY28902 uses a 5-state encoding for the $\overline{\text{T2P}}$ output by changing the pin level and/or the duty cycle. Table 3 lists the $\overline{\text{T2P}}$ state based on the above input conditions:

Table 3. $\overline{\text{T2P}}$ Response based on the PSE Allocated Power, Number of classification events and allocated power

AUX STATE	PD REQUESTED CLASS(RCLASS/RCLASS++)	NUMBER OF CLASSIFICATION EVENTS	$\overline{\text{T2P}}$ WITH RESPECT TO GND	PSE ALLOCATED POWER
AUXILIARY	0-4	NA	Low-Z	AUX Power
	5-8	NA	25% Low-Z 75% HI-Z	AUX Power
PoE	0-4	1	HI-Z	13W
		≥2	Low-Z	25.5W
	5-8	1	HI-Z	13W
		2 or 3	Low-Z	25.5W
		4	50% Low-Z 50% HI-Z	Min(PD Requested Class, 51W)
		5	25% Low-Z 75% HI-Z	Min(PD Requested Class, 71.3W)

The AUX pin is the highest priority input. When AUX is de-asserted, the device can enter the PoE state, but it exits the PoE state as soon as the auxiliary power is detected. Based on the PD requested class, the $\overline{\text{T2P}}$ pin indicates the highest available power in the auxiliary power state. The auxiliary power supply must be sized to provide at least the level of power required by the PD.

As shown in Table 2, the RCLASS and RCLASS++ pins configure the PD-requested class. The RCLASS++ pin can be used to determine if the PD Class is 0-4 or 5-8.

As shown in Table 1, the amount of power allocated by the PSE is determined by the number of classification events.

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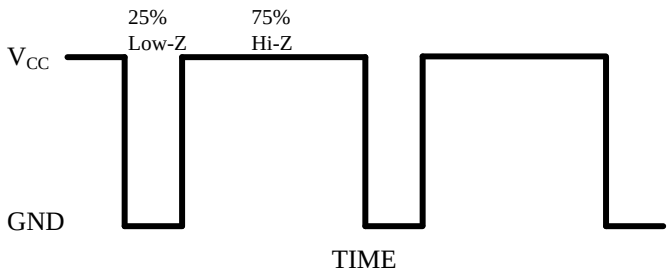

Figure 10. Example of a 25% Low-Z, 75% Hi-Z Response

Thermal Shutdown Protection

A PD must meet the IEEE 802.3 specification to indefinitely withstand any applied voltage from 0V to 57V.

However, during the classification process, the power dissipation of the SY28902 may be as high as 1.5W. The SY28902 easily tolerates this during the maximum IEEE classification timing but can overheat if this condition persists abnormally. The SY28902 includes a thermal shutdown protection function to protect itself and the downstream equipment under abnormal load conditions. If the junction temperature exceeds the over-temperature threshold, the SY28902 pulls down the HSGATE pin and disables classification.

External Interface and Component Selection

PoE Input Bridge

A PD needs to perform polarity correction of its input voltage. There are several options for bridge rectifiers: ideal diodes, silicon diodes, and Schottky diodes. When using Schottky or silicon diode bridges, the voltage at the VPORT pin will be reduced due to the forward voltage across the diodes. The SY28902 is designed to tolerate these voltage drops.

Silicon diode bridges perform poorly, are unbalanced from wiring pair to pair, and consume up to 4% of the available power. In addition, thermal runaways can cause significant, non-compliant current unbalance between pair sets. Although using Schottky diodes can help reduce power loss and offer lower forward voltages, Schottky bridges may not be suitable for high-temperature PD applications, due to the increase of leakage currents at high temperature and a dependance of the leakage with voltage, as this can lead to an invalid detection signature.

The increased leakage currents can also back-feed through the unpowered branch and the unused bridge, violating the IEEE 802.3 specifications.

Auxiliary Input Diode Bridge

Some PDs require an auxiliary power source to receive AC or DC power. A diode bridge is typically required to handle the polarity correction and voltage rectification.

Input Capacitor

Add a 0.1μF capacitor between VPORT and GND to meet the input impedance requirement of IEEE 802.3 and appropriately bypass the SY28902.

Transient Voltage Suppressor

The SY28902 is specified to withstand an absolute maximum input voltage of 100V, and it can tolerate brief over-voltage events due to Ethernet cable surges. To protect the SY28902 from an over-voltage event, a unidirectional transient voltage suppressor (TVS), such as an SMAJ60A, should be used between the VPORT and GND pins.

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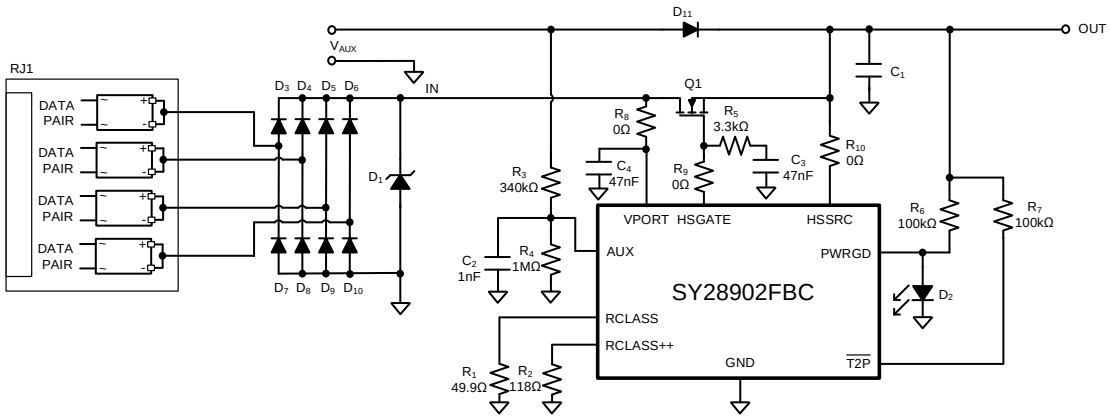
Application Schematic



BOM List

Designator	Description	Part Number	Manufacturer
C_1	/	/	/
C_2	1nF/50V, 0603	GRM1885C1H102GA01D	Murata
C_3	47nF/100V, 0805	GRM21BR72A4473KA01L	Murata
C_4	47nF/100V, 0805	GRM21BR72A4473KA01L	Murata
R_1	49.9Ω, 0603	RC0603FR-0749R9L	YAGEO
R_2	118Ω, 0603	RC0603FR-07118RL	YAGEO
R_3	340kΩ, 0603	RC0603FR-07340KL	YAGEO
R_4	1MΩ, 0603	RC0603FR-071ML	YAGEO
R_5	3.3kΩ, 0603	RC0603FR-073K3L	YAGEO
R_6	100kΩ, 0603	RC0603FR-07100KL	YAGEO
R_7	100kΩ, 0603	RC0603FR-07100KL	YAGEO
R_8, R_9,R_{10}	0	/	/
D_1	TVS/60V, SMA	SMAJ60A	Littelfuse
D_2	LED	/	/
D_3-D_{11}	Schottky/100V	SS3100	TOSHIBA
RJ1	RJ45	RJ45-B-1*1	BOOMELE
Q_1	NMOS/100V	FDMS86150	Fairchild

Layout Considerations

Place resistors R_1 and R_2 close to the SY28902 to avoid excessive parasitic capacitance on the RCLASS and RCLASS++ pins.

Place the transient voltage suppressor (TVS) as close to SY28902 as possible. Place the 0.1μF input capacitor with appropriate voltage rating close to the device input pins.

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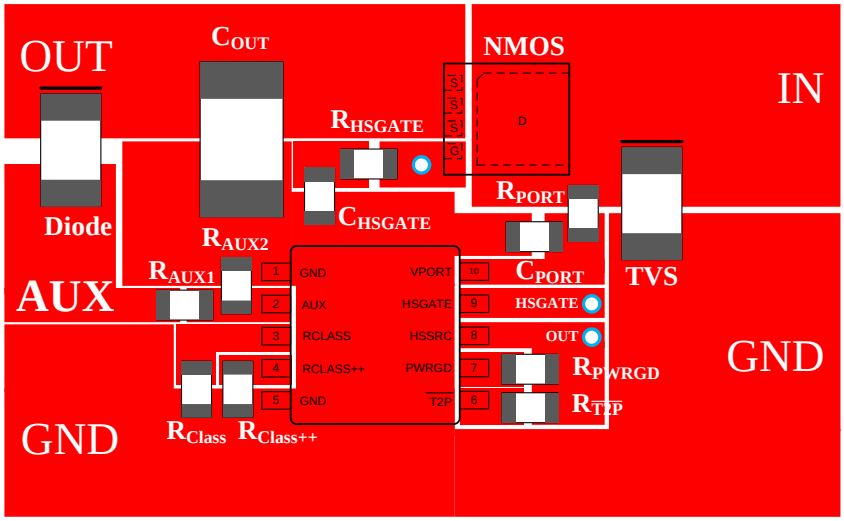

Figure 11. PCB Layout Suggestion

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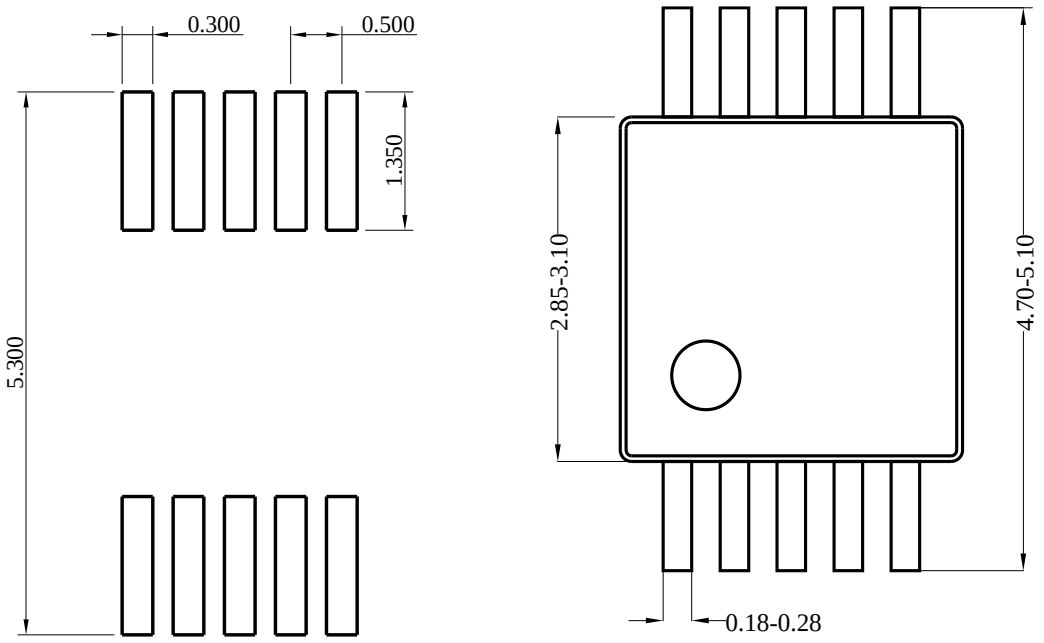
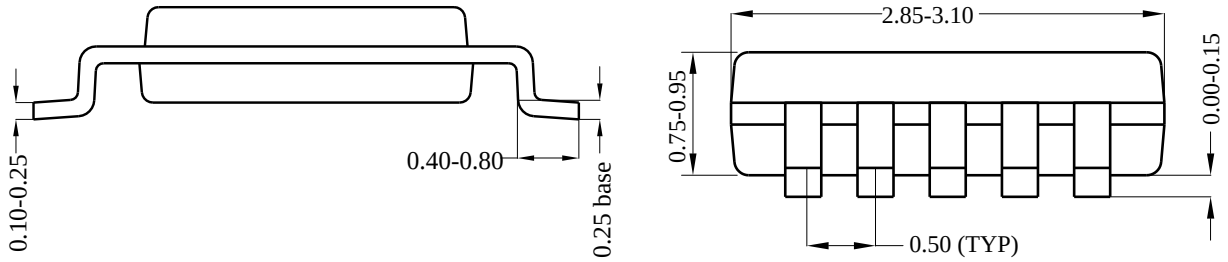
MSOP10 Package Outline & PCB Layout



Recommended Pad Layout



Notes: All dimensions are in millimeters and exclude mold flash and metal burr.

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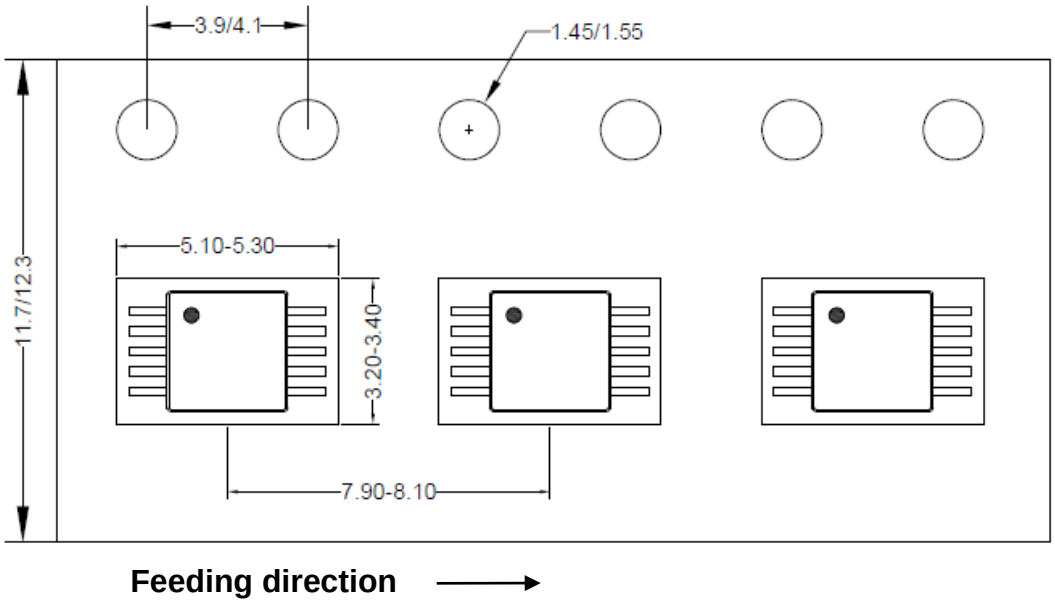
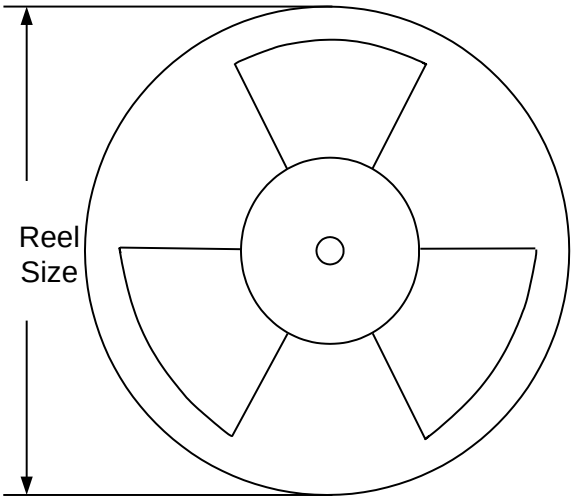
Taping & Reel Specification

MSOP10 Taping Orientation



Carrier Tape & Reel Specification for Packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
MSOP10	12	8	13"	400	400	3000

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Revision History

Date	Revision	Change
Oct.18, 2023	Revision 1.0	Language improvements for clarity.
Jan. 20, 2022	Revision 0.9	Initial Release

The revision history provided is for informational purposes only and is believed to be accurate; however, it is not warranted. Please make sure that you have the latest revision.

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