SY26056

Continuous Source- or Sink-Current, 6A, 6V Input High-Efficiency Synchronous Step-Down Regulator

General Description

The SY26056 high-efficiency synchronous step-down DC/DC regulator is capable of delivering 6A of continuous source or sink output current over a wide input voltage range of 0.8V to 6V.The output voltage is adjustable from 0.4V to 1.2V

Silergy's proprietary Instant-PWM™ fast-response, constant-on-time (COT) PWM control method supports high input/output voltage ratios (low duty cycles) and responds to load transients within approximately 100ns, while maintaining a near-constant operating frequency over line, load, and output voltage ranges. This control method provides stable operation without complex compensation, even with low-ESR ceramic output capacitors.

Internal 18mΩ power and 10mΩ synchronous rectifier switches provide excellent efficiency for a wide range of applications, especially for low output voltages and low duty cycles. The SY26056 offers cycle-by-cycle current limit, input undervoltage lock-out, internal soft-start, output undervoltage and overvoltage protection, and thermal shutdown to provide safe operation in all operating conditions.

The SY26056 is available in a compact QFN3.5mm×4mm package.

Features

- 0.8V to 6V Input Voltage Range
- 6A Continuous Output Source or Sink Current
- Internal 18mΩ Power Switch and 10mΩ Synchronous Rectifier
- Accurate ±1% Output Voltage
- Fast Transient Response
- 600kHz and 1000kHz Operating Frequency
- Adjustable 0.4 to 1.2V Output Voltage
- Selectable Peak-, Valley-, and Reverse-Current Limit
- Selectable Automatic High-Efficiency Discontinuous Operating Mode at Light Loads
- Output Voltage Tracking Using an External Voltage Reference
- Internal Soft-Start Limits Inrush Current
- Smooth Pre-Biased Startup
- Power-Good Indicator
- Auto-Recovery for Input Undervoltage (UVLO), Output Undervoltage (UVP), Output Overvoltage (OVP) and Overtemperature (OTP) Conditions
- MSL-3 Compliant
- Package: QFN3.5mm×4mm

Applications

- Memory Termination Regulator for DDR/DDR2/DDR3/DDR3L/DDR4
- V_{TT} Termination

Typical Application

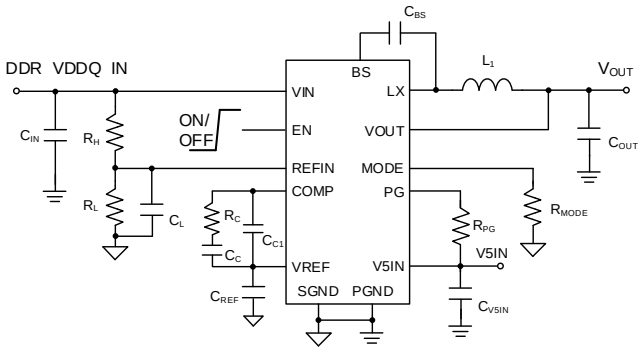

Figure 1. Application Circuit

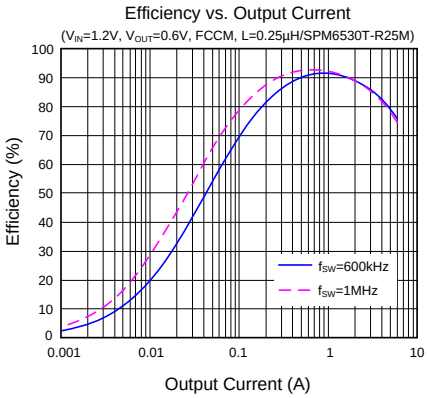

Figure 2. Efficiency vs. Output Current

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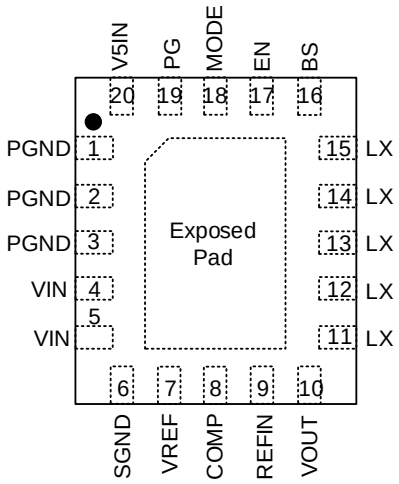
Ordering Information

Ordering Part Number	Package Type	Top Mark
SY26056WEQ	QFN3.5×4-20 RoHS-Compliant and Halogen-Free	**ECR***xyz*

x = year code, y = week code, z = lot number code

Pinout (top view)



Pin No	Pin Name	Pin Description
1, 2, 3	PGND	Power ground.
4, 5	V_{IN}	Power input. Decouple this pin to PGND pin with at least a 20µF ceramic capacitor.
6	SGND	Signal ground.
7	V_{REF}	Internal 1.2V reference pin. Decouple this pin to the SGND pin with at least a 0.22µF ceramic capacitor.
8	COMP	Loop compensation pin. Connect an R-C-C network between this pin and the V_{REF} pin.
9	REFIN	External tracking reference input. Tracking reference range is 0.4V to 1.2V. Connect the REFIN pin and the V_{REF} pin using a resistor-divider for non-tracking mode.
10	V_{OUT}	Output voltage feedback pin.
11, 12, 13, 14, 15	LX	Inductor pin. Connect this pin to the switching node of the inductor.
16	BS	Bootstrap supply for the high-side gate driver. Connect a 0.1µF ceramic capacitor between the BS and the LX pin.
17	EN	Enable input. Pull low to disable the device, high to enable. Do not leave this pin floating.
18	MODE	Operation mode selection. See Table 1.
19	PG	Power-good indicator. Open-drain output when the output voltage is within 93.5% to 120% of the regulation setpoint.
20	V_{5IN}	External 5V power supply for analog circuits and gate driver.

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Block Diagram

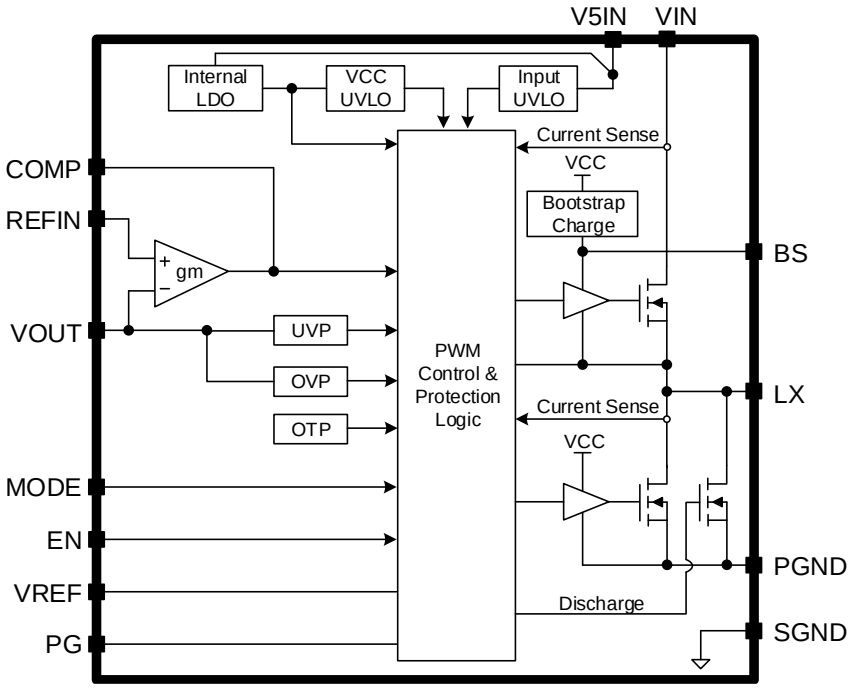

Figure 3. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
V_{IN}, V_{5IN}, LX	-0.3	7	V+
EN, PG, MODE	-0.3	V5IN + 0.3	
LX, 20ns duration	-3	10	
BS	LX - 0.3	LX + 4	
V_{REF}, REFIN, COMP	-0.3	4	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering,10sec.)		260	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	30.5	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	4	
P_D Power Dissipation T_A = 25°C	3.2	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
V_{IN}	-0.1	6.5	V
V_{5IN}	4.5	6.5	
Output Current	-6	6	A
Junction Temperature	-40	125	°C

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Electrical Characteristics

(V_{V5IN} = 5V, T_J = -40°C to +125°C, typical values are at T_J = 25°C, unless otherwise specified (Note 4))

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
V_{IN} Shutdown Current		I_{VIN_SD}	V_{EN} = 0V, T_J = 25°C		1.8	5	μA
V_{5IN}	Voltage	V_{V5IN}		4.5	5	6.5	V
	UVLO, rising	$V_{V5IN,UVLO}$	V_{V5IN} rising	4.1	4.37	4.5	
	UVLO, Hysteresis	$V_{V5IN,HYS}$	V_{V5IN} falling		500		mV
	Supply Current	I_{V5IN}	EN high, V_{5IN} supply current, f_{SW} = 600kHz		1.1		mA
	Shutdown Current	$I_{V5IN,SD}$	EN low, V_{5IN} shutdown current		3	6	μA
	POR Reset Threshold	$V_{POR,V5IN}$	OVP latch is reset by V_{5IN} falling below the reset threshold	2.5	3	3.5	V
V_{REF}	UVLO, Rising	$V_{VREF,UVLO}$	V_{VREF} rising		1.1		V
	UVLO, Hysteresis	$V_{VREF,HYS}$	V_{VREF} falling		100		mV
	Accuracy	V_{VREF}	I_{VREF} = 0μA	1.188	1.2	1.212	V
			I_{VREF} = 50μA	1.185	1.2	1.215	
	Sink Current	I_{VREF}	V_{VREF} = 1.25V		1		mA
Power Switch	On-Resistance	$R_{DS(ON)HS}$	V_{BS-LX} = 3.3V, T_J = 25°C		18		mΩ
	Peak-Current Limit	$I_{LMT,TOP1}$	See Table 1		10.5		A
		$I_{LMT,TOP2}$			8.5		
Synchronous Rectifier	On-Resistance	$R_{DS(ON)LS}$	V_{CC} = 3.3V, T_J = 25°C		10		mΩ
	Valley-Current Limit	$I_{LMT,BOT1}$	See Table 1	6.8	9.5	11	A
		$I_{LMT,BOT2}$		4.2	6.5	9	
	Reverse-Current Limit	$I_{LMT,RVS1}$			-10.3		
		$I_{LMT,RVS2}$			-7		
Internal-Current Sense Gain		A_{CSINT}	Gain from the current of the low-side FET to PWM comparator when PWM = OFF	43	53	67	mV/A
Output Voltage Accuracy		$V_{OUT,ACC}$	V_{REFIN} = 0.6V	-1		+1	$\%V_{REFIN}$
Discharge FET Resistance		R_{DIS}			36		Ω
Enable (EN)	Input Voltage High	$V_{EN,H}$		2			V
	Input Voltage Low	$V_{EN,L}$				0.5	
	Leakage Current	$I_{EN,LKG}$	EN high			1	μA
Soft-Start (SS)	Time	$t_{INT,SS}$	V_{OUT} ramps up from 0 to 95%		1.6		ms
	Delay Time	$t_{INT,SSDLY}$	From V_{VREF} = 1.1V to V_{OUT} ready to ramp up		260		μs
Zero-Crossing Comp Internal Offset		V_{ZXOS}			0		mV
Overvoltage Protection	Threshold	V_{OVP}	Measure V_{OUT}, V_{REFIN} = 1V		120		$\%V_{REFIN}$
	Delay	$t_{OVP,DLY}$	Time from V_{OUT} exceeds 120% of V_{REFIN} to OVP fault		10		μs
Undervoltage Protection	Threshold	V_{UVP}	Measure V_{OUT}, device latches off, begins soft-stop, V_{REFIN} = 1V	64	68	72	$\%V_{REFIN}$
	Delay	$t_{UVP,DLY}$	Time from V_{OUT} less than 68% of V_{REFIN} to UVP fault		256		μs
UVP Hiccup On-Time		$t_{HICCUP,ON}$			2		ms
UVP Hiccup Off-Time		$t_{HICCUP,OFF}$			18		
Min Off-Time		$t_{OFF,MIN}$	V_{VIN} = 5V, V_{VOUT} = 1.05V, f_{SW} = 1MHz, V_{VOUT} < V_{REFIN}		260		ns

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Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Undervoltage Fault-Enable Delay		$t_{UVP,DLY,EN}$	Time from EN_INT going high to undervoltage fault is ready		2		ms
			External tracking from V_{OUT} ramp starts		8		
Power-Good	Thresholds	V_{PG}	V_{OUT} falling, fault		84		%V_{REFIN}
			V_{OUT} rising, good		92		
			V_{OUT} rising, fault		116		
			V_{OUT} falling, good		108		
	Startup Delay	$t_{PG,ST}$	At external tracking, time from V_{OUT} ready to ramp-up		8		ms
	Delay	$t_{PG,R}$	V_{OUT} rising, good	0.5	1	1.3	
		$t_{PG,F}$	V_{OUT} falling, fault		10		µs
	Output Low	$I_{PG,LKG}$	I_{PG} = 4mA, V_{V5IN} = 4.5V			0.3	V
	Leakage Current	$V_{PG,L}$	V_{PG} = 5.5V	-1	0	1	µA
Minimum V_{IN} Voltage for Valid PG		$V_{INMINPG}$	Measured at V_{IN} pin with a 2mA sink current on PG pin. V_{5IN} is grounded here.	0.7	1	1.6	V
Transconductance		gm			1		mS
Common-Mode Input Voltage Range		V_{CM}		0		1.2	V
Different-Mode Input Voltage Range		V_{DM}		0		60	mV
COMP	Maximum Source Current	$I_{COMP,SRC}$	V_{COMP} = 1.2V, V_{REFIN} - V_{OUT} = 60mV		60		µA
	Maximum Sink Current	$I_{COMP,SNK}$	V_{COMP} = 1.2V, V_{REFIN} - V_{OUT} = -60mV		-60		
Input Offset Voltage of Error Amplifier		V_{OFFSET}	T_J = 25ºC		0		mV
Thermal Shutdown	Threshold	T_{SD}			145		˚C
	Hysteresis	T_{HYS}			10		

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Package thermal resistance is measured in the natural convection at T_A = 25˚C on an 8.5cm×8.5cm size four-layer Silergy Evaluation Board.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Production testing is performed at 25˚C; limits at -40°C to +125°C are guaranteed by design, test or statistical correlation.

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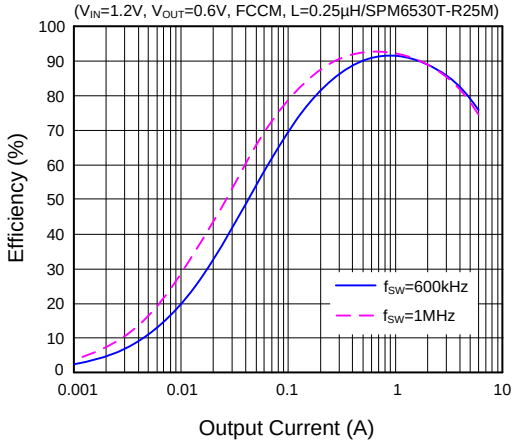
Typical Performance Characteristics

(T_A = 25 ˚C, V_{V5IN} = 5V, V_{IN} = 1.2V, V_{OUT} = 0.6V, L = 0.25μH, C_{OUT} = 12 × 22μF, f_{SW} = 600kHz, unless otherwise noted.)

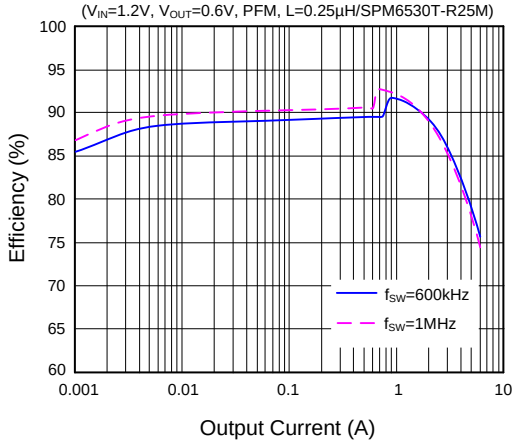
Efficiency vs. Output Current

(V_{IN}=1.2V, V_{OUT}=0.6V, FCCM, L=0.25μH/SPM6530T-R25M)



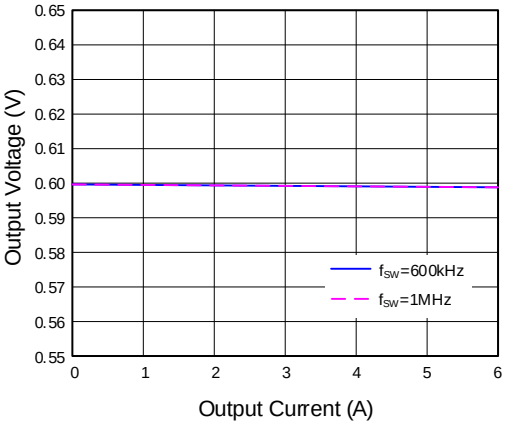
Efficiency vs. Output Current

(V_{IN}=1.2V, V_{OUT}=0.6V, PFM, L=0.25μH/SPM6530T-R25M)



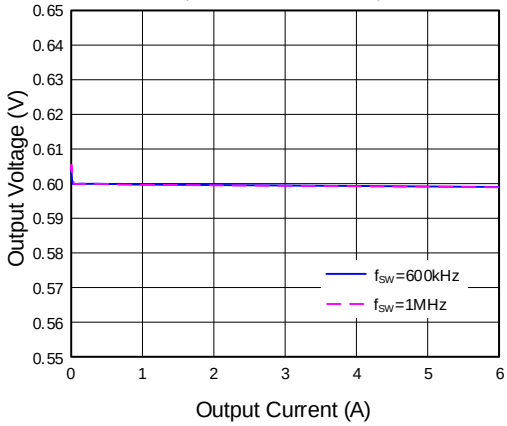
Load Regulation

(V_{IN}=1.2V, V_{OUT}=0.6V, FCCM)



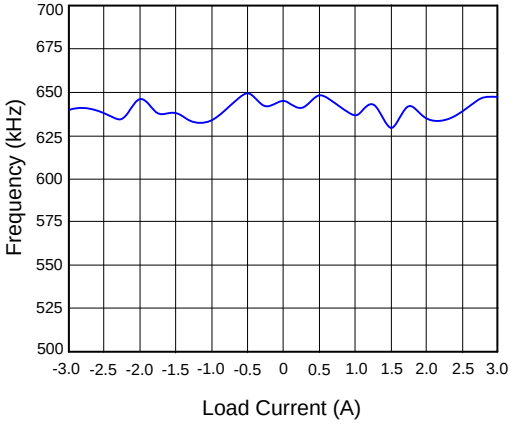
Load Regulation

(V_{IN}=1.2V, V_{OUT}=0.6V, PFM)



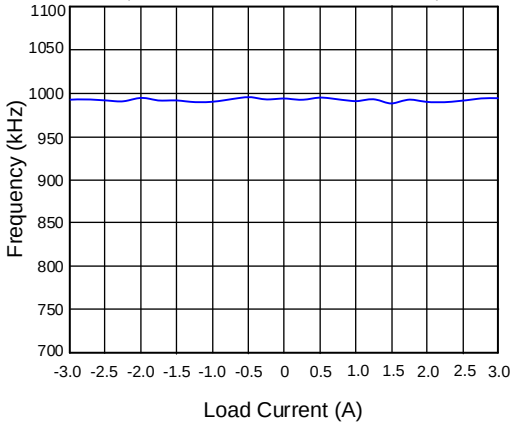
Frequency vs. Load Current

(V_{IN}=1.2V, V_{OUT}=0.6V, f_{SW}=600kHz, FCCM)



Frequency vs. Load Current

(V_{IN}=1.2V, V_{OUT}=0.6V, f_{SW}=1000kHz, FCCM)



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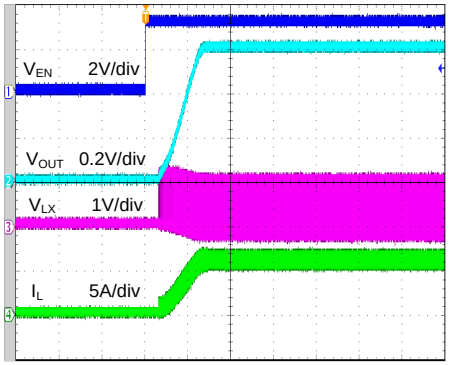
Startup from Enable

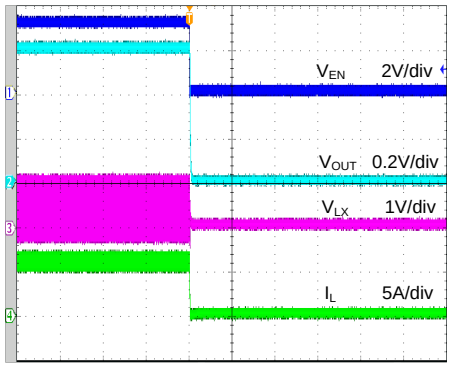
(V_{IN}=1.2V, V_{OUT}=0.6V, I_{OUT}=6A)



Time (2ms/div)

Shutdown from Enable

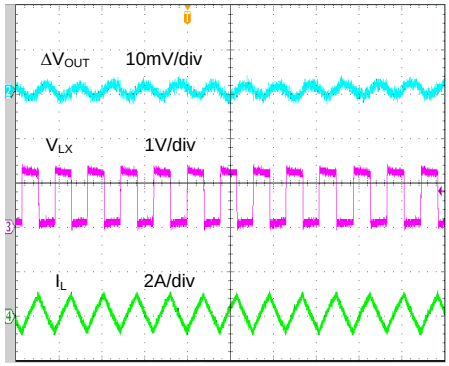
(V_{IN}=1.2V, V_{OUT}=0.6V, I_{OUT}=6A)



Time (2ms/div)

Output Ripple

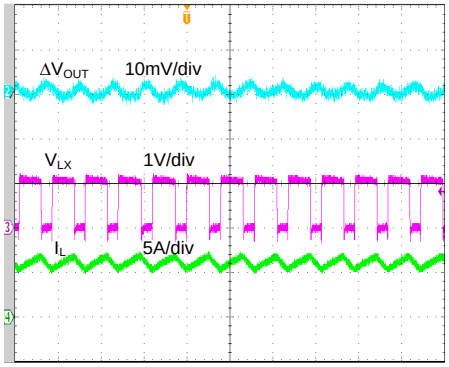
(V_{IN}=1.2V, V_{OUT}=0.6V, I_{OUT}=0A)



Time (2µs/div)

Output Ripple

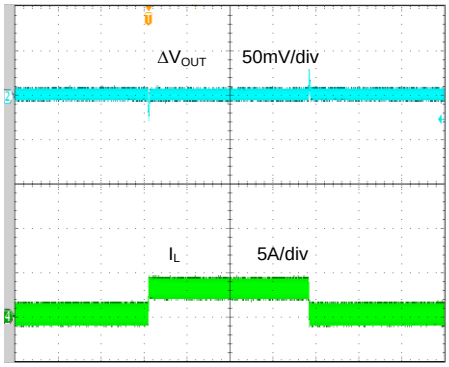
(V_{IN}=1.2V, V_{OUT}=0.6V, I_{OUT}=6A)



Time (2µs/div)

Load Transient

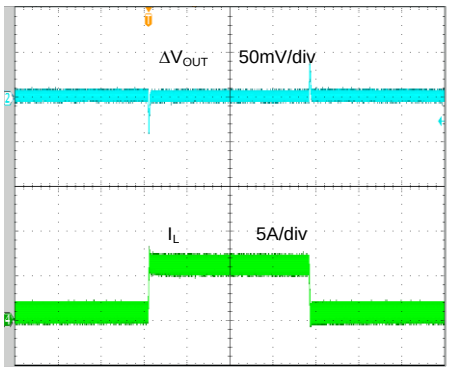
(V_{IN}=1.2V, V_{OUT}=0.6V, I_{OUT}=0A~3A~0A)



Time (800µs/div)

Load Transient

(V_{IN}=1.2V, V_{OUT}=0.6V, I_{OUT}=0.6A~6A~0.6A)



Time (800µs/div)

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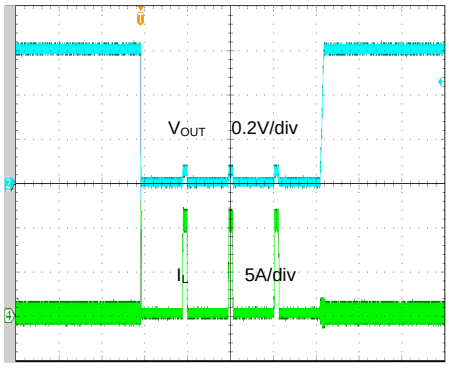
Short Circuit Protection

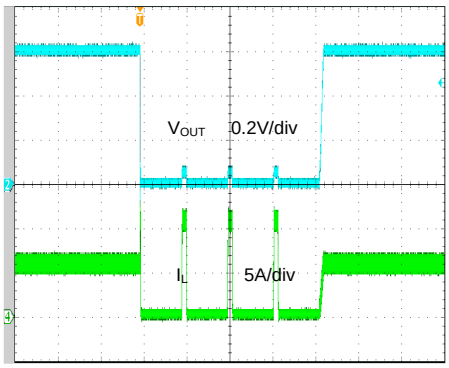
(V_{IN}=1.2V, V_{OUT}=0.6V, 0A Short)



Time (20ms/div)

Short Circuit Protection

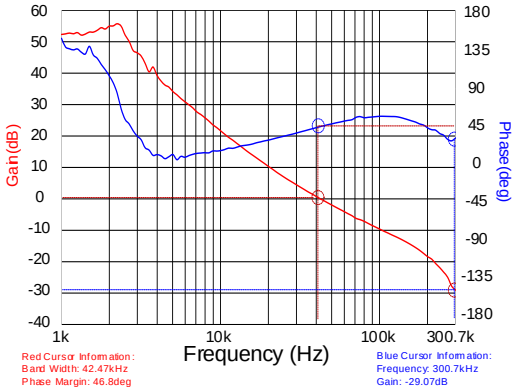
(V_{IN}=1.2V, V_{OUT}=0.6V, 6A Short)



Time (20ms/div)

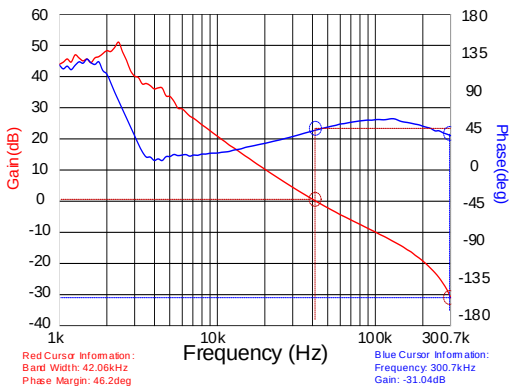
Bode Plot

(V_{IN}=1.2V, V_{OUT}=0.6V, I_{OUT}=3A, f_{sw}=600kHz)



Bode Plot

(V_{IN}=1.2V, V_{OUT}=0.6V, I_{OUT}=3A, f_{sw}=1000kHz)



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Detailed Description

The SY26056 high-efficiency synchronous step-down DC/DC regulator is capable of delivering 6A of continuous source or sink output current over a wide input voltage range of 0.8V to 6V.The output voltage is adjustable from 0.4V to 1.2V

The SY26056 uses a constant on-time and valley current control architecture to enable fast transient response.

Internal 18mΩ power and 10mΩ synchronous rectifier switches provide excellent efficiency for a wide range of applications, especially for low output voltages and low duty cycles. The SY26056 offers cycle-by-cycle current limit, input undervoltage lock-out, internal soft-start, output undervoltage and overvoltage protection, and thermal shutdown to provide safe operation in all operating conditions.

Constant-On-Time Architecture

The one-shot circuit or on-time generator, which determines how long to turn on the high-side power switch, is fundamental to any constant-on-time (COT) architecture. Each on-time (t_{ON}) is a fixed period internally calculated to operate the step-down regulator at the desired switching frequency, considering the input and output voltage ratio, $t_{ON} = (V_{OUT}/V_{IN}) \times (1/f_{SW})$. For example, consider a hypothetical converter that targets 0.6V output from a 1.2V input at 600kHz. The target on-time is (0.6V/1.2V) × (1/600kHz) = 833ns. Each t_{ON} pulse is generated at the beginning of a new switching cycle. After one t_{ON} period, a minimum off-time ($t_{OFF,MIN}$) is imposed before any further switching is initiated. This approach avoids making any switching decisions during the noisy periods immediately after switching events, or while the switching node (LX) is rapidly rising or falling.

There is no fixed clock in the COT control loop, so the high-side power switch can turn on almost immediately after a load transient. Subsequent switching pulses can be quickly initiated, ramping the inductor current up to meet load requirements with minimal delays.

Valley Current Mode Operation

During normal, steady-state operation, the output voltage is compared with a fraction of the V_{REF} voltage and the amplified error signal is generated by the transconductance amplifier. A new switching cycle starts with turning on the main switch for the constant on-time period, followed by the off-time when the main switch is turned off and the synchronous switch is turned on. It keeps the on-time constant while only adjusting the off-time as required to maintain the regulated voltage. The SY26056 control loop monitors the current going through the synchronous rectifier MOSFET during the off time. The decision to start the next switching cycle is based on comparing the current sense signal with the output of the error signal amplifier. The minimum t_{OFF} time is used to avoid making any incorrect switching decisions during the noisy periods. The minimum t_{OFF} is relatively short so that during sudden load current increases, t_{ON} can be retriggered with minimal delay, allowing the inductor current to ramp up quickly, in order to provide sufficient energy to the output capacitor.

Frequency-Locked Loop (FLL)

Although COT provides a relatively constant operating frequency over variations in line and load conditions, Silergy's FLL improves the operating frequency performance by comparing the actual operating frequency with an internal reference frequency. The signal that results is used to adjust t_{ON}, resulting in a stable and predictable operating frequency. Note that the FLL is disabled during soft-start and during discontinuous inductor current mode (DCM) conditions. In these cases, the operating frequency will be lower than the target.

Light-Load Operating Modes

The SY26056 supports two user-selectable light-load operating modes, set with the MODE input (see Table 1). Light load occurs at approximately $I_{OUT} < 0.5 \times \Delta I_L$, when the current through the low-side synchronous rectifier will ramp to near zero before the next t_{ON} time.

In forced continuous inductor current mode (FCCM), the low-side synchronous rectifier remains on until the next t_{ON} cycle, allowing continuous current flow in the inductor. The inductor current ramps below zero, recirculating current from the output to the input. This allows the device to maintain a relatively constant switching frequency over the output current range. This also reduces efficiency at light loads, but is often desirable in equipment that is sensitive to low-frequency operations, such as audio or RF systems.

In discontinuous inductor current mode (DCM), the low-side synchronous rectifier is turned off and remains off when the inductor current reaches zero, preventing recirculation current that can significantly reduce efficiency under these light-load conditions. As load current is further reduced and the V_{OUT} voltage remains greater than the REFIN voltage, the Instant-PWM control loop will not trigger another t_{ON} until needed, so the apparent operating switching frequency will drop, further enhancing efficiency. Continuous inductor current mode (CCM) resumes smoothly as soon as the load current increases sufficiently for the inductor current to remain

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above zero at the time of the next t_{ON} cycle. This threshold of load current may be determined as follows:

$$I_{OUT\_CTL} = \frac{\Delta I_L}{2} = \frac{V_{OUT} \times (1 - D)}{2 \times f_{SW} \times L_1}$$

Note that the operating frequency of the device in DCM can be very low, and may not be desirable in equipment that is sensitive to low-frequency operations such as audio or RF systems.

MODE Input

The MODE pin is an input that provides user-selectable operating frequency, light-load operating modes, and current-limit value. See Table 1 for configuration details. Note that this input is evaluated during startup of the device, and changes to the configuration after startup will not change the device operation. Any change in the configuration requires a restart of the device.

Table 1. MODE Configuration

MODE	MODE Resistance to GND	Light-Load Mode	Switching Frequency	Valley-Current Limit	Peak-Current Limit	Reverse-Current Limit
1	0Ω	DCM	600kHz	$I_{LMT,BOT1}$	$I_{LMT,TOP1}$	$I_{LMT,RVS1}$
2	12kΩ (±5%)		600kHz	$I_{LMT,BOT2}$	$I_{LMT,TOP2}$	$I_{LMT,RVS2}$
3	22kΩ (±5%)		1000kHz	$I_{LMT,BOT2}$	$I_{LMT,TOP2}$	$I_{LMT,RVS2}$
4	33kΩ (±5%)		1000kHz	$I_{LMT,BOT1}$	$I_{LMT,TOP1}$	$I_{LMT,RVS1}$
5	47kΩ (±5%)	FCCM	600kHz	$I_{LMT,BOT1}$	$I_{LMT,TOP1}$	$I_{LMT,RVS1}$
6	68kΩ (±5%)		600kHz	$I_{LMT,BOT2}$	$I_{LMT,TOP2}$	$I_{LMT,RVS2}$
7	100kΩ (±5%)		1000kHz	$I_{LMT,BOT2}$	$I_{LMT,TOP2}$	$I_{LMT,RVS2}$
8	Floating		1000kHz	$I_{LMT,BOT1}$	$I_{LMT,TOP1}$	$I_{LMT,RVS1}$

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Non-Tracking Startup

When the SY26056 is configured for non-tracking applications, output voltage is regulated to the REFIN voltage, which taps off the voltage dividers from the 1.2V reference voltage. Either the EN pin or the V_{5IN} pin can be used to start up the device. The soft-start time is 1.6ms in this application (see Figure 5).

In a non-tracking application, the output voltage is determined by the resistive divider between the V_{REF} pin and the REFIN pin as follows:

$$V_{OUT} = \frac{R_2}{R_1 + R_2} \times V_{REF}$$

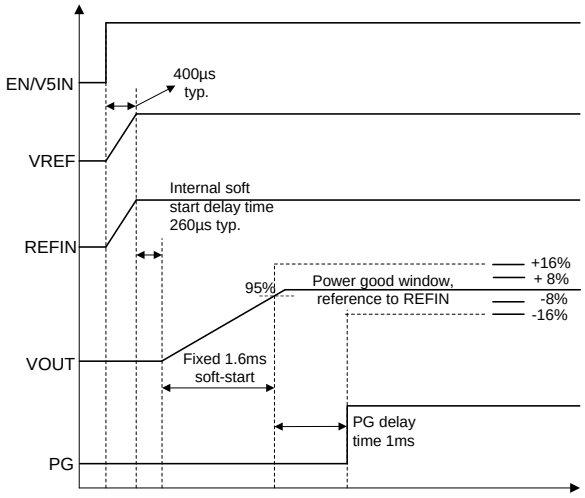

Figure 5. Non-Tracking Startup

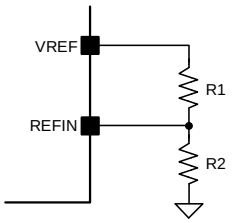

Figure 6. Non-Tracking Configuration

Tracking Startup

When the SY26056 is configured for tracking applications, output voltage is regulated to the REFIN voltage, which comes from an external power source. In order for the device to differentiate between a non-tracking configuration and a tracking configuration, there is a minimum delay time of 260µs required between the time when V_{REF} reaches 1.2V to the time when the REFIN pin voltage can be applied (see Figure 9). The valid REFIN voltage range is between 0.4V and 1.2V.

In a DDR Memory power tracking application, the output voltage should be one half of the V_{DDQ} voltage. V_{DDQ} can be V_{IN}, or it can be an additional power rail. Therefore, R1 = R2 in both Figure 7 and Figure 8.

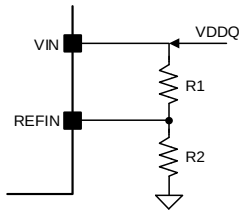

Figure 7. Tracking Configuration I

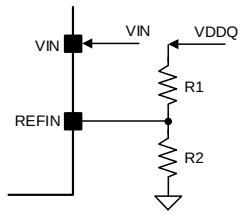

Figure 8. Tracking Configuration II

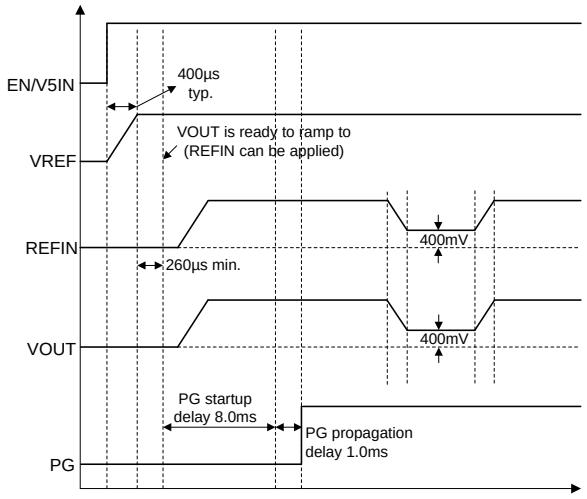

Figure 9. Tracking Startup Timing

DROOP Application

Compared to non-DROOP applications, DROOP applications have the advantage of reducing the output capacitors (with the same dynamic peak-to-peak output-volage ripple specification) and reducing power

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consumption. The comparison of load-transient performance between non-DROOP and DROOP configurations is shown in Figure 10.

As Figure 11 shows, the compensation between COMP and V_{REF} is a purely proportional component (R instead of RC), which will cause the amplifier's gain to be finite. The equation for DROOP voltage is as follows:

$$V_{DROOP} = \frac{I_{OUT} \times A_{CSINT}}{g_m \times R_{DROOP}}$$

where I_{OUT} is the output current, A_{CSINT} is 53mV/A (typ), g_m is the transconductance of the amplifier, which is 1mS (typ), R_{DROOP} is the value of the resistor connected between the V_{REF} pin and the COMP pin.

The following equation can be used for selecting proper R_{DROOP} for a target load-line:

$$R_{DROOP} = \frac{A_{CSINT}}{g_m \times R_{LOAD-LINE}}$$

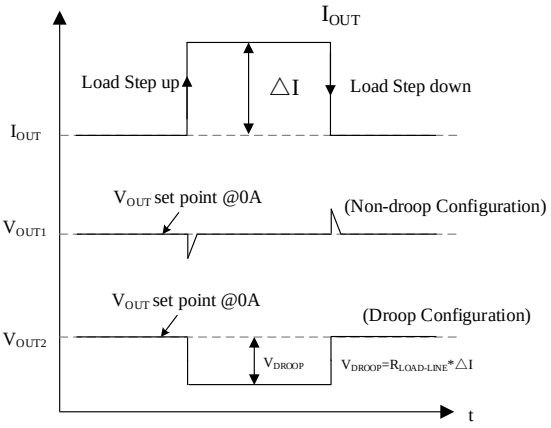

Figure 10. Non-DROOP and DROOP Comparison

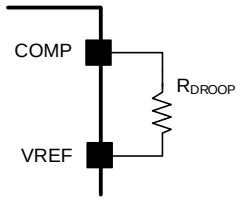

Figure 11. DROOP Configuration

External Bootstrap Capacitor Connection

This device integrates a floating power supply for the gate driver that operates the high-side power switch. Proper operation requires a 0.1µF low-ESR ceramic capacitor to be connected between the BS and LX pins. This bootstrap capacitor provides the gate driver supply voltage for the high-side N-channel MOSFET power switch.

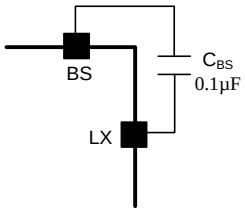

Figure 12. External Bootstrap Capacitor

Power-Good Indicator (PG)

PG is an open-drain output controlled by a window comparator connected to the feedback signal. PG allows system monitoring of the device. If V_{OUT} is greater than $V_{PG,R}$ and less than V_{OVP} for at least $t_{PG,R}$, PG will be high-impedance.

Connect PG to V_{5IN}, or another desirable voltage rail, with a resistor in the range of 10kΩ to100kΩ. During startup, there is a 1ms power-good high-propagation delay. The PG pin is pulled low as soon as the EN pin is pulled low, or an undervoltage condition on V_{5IN} (or any other fault) is detected.

Bias Capacitor C_{V5IN}

It is recommended to use a X7R or better grade ceramic capacitor with 10V rating and no less than 2.2µF capacitance. This ceramic capacitor is recommended to be placed close to the V5IN and GND pins.

V_{REF} Output Capacitor C_{VREF}

It is recommended to use a X7R or better grade ceramic capacitor with 6.3V rating and no less than 0.22µF capacitance. This ceramic capacitor is recommended to be placed close to the VREF and SGND pins.

Output Discharge Function

An internal 36Ω discharge FET is turned on whenever the shutdown logic is triggered, discharging the output through the inductor. The circuit is only active during the shutdown process, when it brings the output to a low-voltage state until the device is once again enabled.

V_{5IN} Undervoltage Protection

The SY26056 continuously monitors the voltage on the V_{5IN} pin to ensure that the voltage level is high enough to bias the device properly and to provide sufficient gate drive to maintain high efficiency. The converter starts when the voltage rises above 4.37V (typ.) and has a

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nominal 500mV of hysteresis. If the V_{5IN} voltage limit is reached, the converter latches off until the device is reset by cycling V_{5IN} voltage until the POR is reached (3V nominal). The power input does not have a UVLO function.

Fault-Protection Modes

Overcurrent Protections (OCP)

Three cycle-by-cycle overcurrent protections are integrated in this device to prevent excessive current flow. Although current-limit protections will not force a shutdown of the device, continuous operation in these conditions is expected to result in the output voltage dropping below the undervoltage protection threshold, or in the case of the junction temperature rising above the thermal protection limit, which will shut down the device. See UVP and OTP sections for more information.

Peak-Current Limit

During t_{ON}, and after $t_{ON,MIN,}$ if the high-side power-switch current exceeds $I_{LMT,TOP}$, the switch is turned off, the low-side synchronous rectifier is turned on, and t_{ON} is inhibited until the low-side synchronous rectifier current is below $I_{LMT,BOT}$. Peak-current limit is disabled during initial t_{ON} at startup. $I_{LMT,TOP}$ is selectable. See Table 1.

Valley-Current Limit

The iInductor current is measured in the low-side synchronous rectifier when it turns on, and as the inductor current ramps down. If the current exceeds $I_{LMT,BOT}$, the synchronous rectifier is turned off and t_{ON} is inhibited until the current is less than $I_{LMT,BOT}$. $I_{LMT,BOT}$ is selectable. See Table 1 for details.

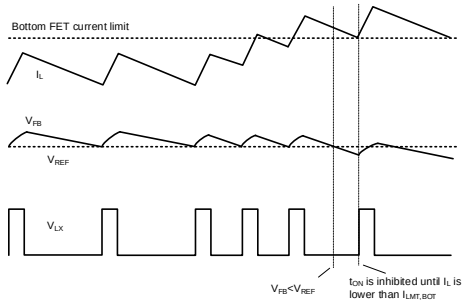

Figure 13. Valley-Current Limit

Reverse-Current Limit

In FCCM mode, if the low-side synchronous rectifier current exceeds $I_{LMT,RVS}$, the low-side synchronous rectifier is turned off and the high-side power switch is turned on for the constant on-time, which is determined by the COT generator. $I_{LMT,RVS}$ is selectable. See Table 1 for details.

Output Undervoltage Protection (UVP)

After startup, if V_{OUT} drops below V_{UVP} for more than $t_{UVP,DLY}$ UVP will be triggered, and the device will shut down for $t_{HICCUP,OFF}$, after which the device will restart with a complete soft-start cycle. If the fault condition remains after $t_{HICCUP,ON}$, this 'hiccup' cycle of startup and shutdown will continue unless the junction temperature exceeds T_{SD}. If the fault condition is resolved, the device will resume normal operation.

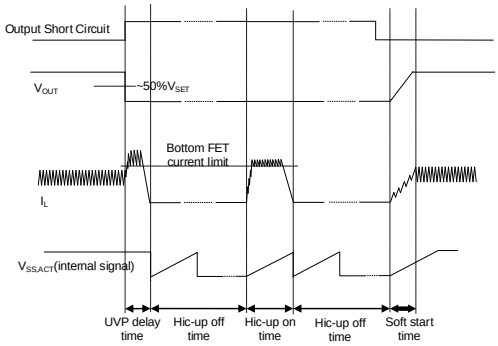

Figure 14. Reverse-Current Limit

Output Overvoltage Protection (OVP)

An OVP condition is detected when the output voltage is approximately 120% × V_{REFIN}. In this case, the converter pulls low the PG pin and performs the overvoltage protection function. During OVP, the low-side FET is always on before triggering the reverse-current limit. After triggering the reverse-current limit, the low-side FET is no longer continuously on, and pulsed signals are generated to limit the negative inductor current. When the output voltage drops below 250mV, the COMP pin voltage will be clamped to approximately 1V. After 10µs delay time, the converter latches off. The converter remains in the off state until the device is reset by cycling V_{5IN} voltage until the POR is reached (2.3V nominal) or when the EN pin is toggled off and on.

Overtemperature Protection (OTP)

The overtemperature protection (OTP) circuitry prevents overheating due to excessive power dissipation. This will shut down the device when the junction temperature exceeds T_{SD}. Once the junction temperature cools down by approximately 10°C, the device will resume normal operation after a complete soft-start cycle. For continuous operation, provide adequate cooling so that the junction temperature does not exceed the T_{SD}.

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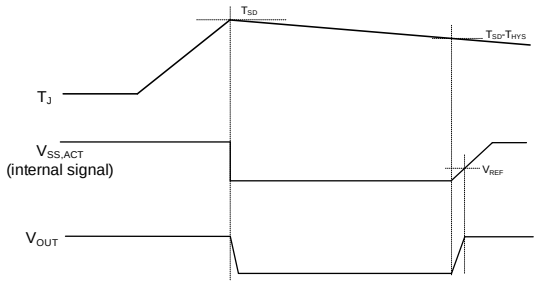

Figure 15. Overtemperature Protection

Design Procedure

Input Capacitor Selection

Input filter capacitors are needed to reduce the ripple voltage on the input, to filter the switched current drawn from the input supply and to reduce potential EMI. When selecting an input capacitor, be sure to select a voltage rating at least 20% greater than the maximum voltage of the input supply and a temperature rating above the system requirements. X5R or X7R series ceramic capacitors are most often selected due to their small size, low cost, surge current capability and high RMS current ratings over a wide temperature and voltage range. Systems that are powered by a wall adapter or other long and therefore inductive cabling may be susceptible to significant inductive ringing at the input to the device. In these cases, consider adding some bulk capacitance like electrolytic, tantalum or polymer type capacitors. Using a combination of bulk capacitors (to reduce overshoot or ringing) in parallel with ceramic capacitors (to meet the RMS current requirements) is helpful in these cases.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required, to meet the calculated RMS ripple current,

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1-D)}$$

The worst-case condition occurs at D = 0.5, then

$$I_{CIN\_RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification.

Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated by

$$V_{CIN\_RIPPLE,CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1\text{-}D)$$

The worst-case condition occurs at D = 0.5, then

$$V_{CIN\_RIPPLE,CAP,MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. In most applications two 10µF and one 100nF X7R capacitors are sufficient. Place the ceramic input capacitors as close to the device VIN and PGND pin as possible, with the 100nF capacitor being the closest.

Inductor Selection

The inductor is necessary to supply constant current to the output load while being driven by the switched input voltage.

Instant-PWM™ operates well over a wide range of inductor values. This flexibility allows for optimization to find the best trade-off of efficiency, cost, and size for a particular application. Selecting a low inductor value will help reduce size and cost, and enhance transient response, but will increase peak inductor ripple current, reducing efficiency and increasing output voltage ripple. The low DC resistance (DCR) of these low-value inductors may help reduce DC losses and increase efficiency. Higher inductor values tend to have higher DCR and will slow transient response.

A reasonable compromise between size, efficiency, and transient response can be determined by selecting a ripple current (ΔI_L) approximately 20–50% of the desired full output load current. Start calculating the approximate inductor value by selecting the input and output voltages, the operating frequency (f_{SW}), the maximum output current ($I_{OUT,MAX}$), and estimated ΔI_L as a percentage of that current:

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Use this inductance value to determine the actual inductor ripple current (ΔI_L) and required peak-current inductor current $I_{L,PEAK}$.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L_1}$$

$$I_{L,PEAK} = I_{OUT,MAX} \times \frac{\Delta I_L}{2}$$

Select an inductor with a saturation current and thermal rating in excess of $I_{L,PEAK}$. If FCCM light-load operation is selected, make sure the inductor value is high enough to avoid the reverse-current limit being triggered during a steady state if the load current is zero.

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For maximum efficiency, select an inductor with a low DCR that meets the inductance, size, and cost targets. Low-loss ferrite materials should be considered.

Inductor Design Example

Consider a typical design for a device providing $0.6V_{OUT}$ at 6A from $1.2V_{IN}$, operating at 600kHz and using a target inductor ripple current (ΔI_L) of 50%, or 3A. Determine the approximate inductance value at first:

$$L_1 = \frac{0.6V \times (1.2V - 0.6V)}{1.2V \times 600kHz \times 3A} = 0.17\mu H$$

Next, select the nearest standard inductance value, in this case 0.25µH, and calculate the resulting inductor ripple current (ΔI_L):

$$\Delta I_L = \frac{0.6V \times (1.2V - 0.6V)}{1.2V \times 600kHz \times 0.25\mu H} = 2A$$

$$I_{L,PEAK} = 6A + 2A/2 = 7A$$

The resulting 2A ripple current is approximately 33.3% (2A/6A), well within the 20%–50% target.

$$I_{L,PEAK,RVS} = 2A/2 = 1A < I_{LIM,RVS}$$

Finally, select an available inductor with a saturation current higher than the resulting $I_{L,PEAK}$ of 7A.

Output Capacitor Selection

Instant-PWM provides excellent performance with a wide variety of output capacitor types. Ceramic and POS types are most often selected due to their small size and low cost. Total capacitance is determined by the transient response and output voltage ripple requirements of the system.

Output Ripple

Output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔI_L) on the output capacitor's ESR (ESR ripple) as well as the stored charge (capacitive ripple). When considering total ripple, both should be considered.

$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

Consider a typical application with ΔI_L = 2A using six 47µF ceramic capacitors, each with an ESR of approximately 5mΩ for a parallel total of 282µF and 0.8mΩ ESR.

$$V_{RIPPLE,ESR} = 2A \times 0.8m\Omega = 1.6mV$$

$$V_{RIPPLE,CAP} = \frac{2A}{8 \times 282\mu F \times 600kHz} = 1.5mV$$

Total ripple = 3.1mV. The actual capacitive ripple may be higher than the calculated value because the capacitance decreases with the voltage on the capacitor.

Output Transient Undershoot/Overshoot

If very fast load transients must be supported, consider the effect of the output capacitor on the output transient undershoot and overshoot. Instant-PWM responds quickly to changing load conditions, but some considerations are still required, especially when using small ceramic capacitors. These capacitors have low capacitance, which results in insufficient stored energy for load transients. Output-transient undershoot and overshoot have two causes: voltage changes caused by the ESR of the output capacitors and voltage changes caused by the output capacitance and inductor current slew rate.

ESR undershoot or overshoot may be calculated as $V_{ESR} = \Delta I_{OUT} \times ESR$. Using the ceramic capacitor example above and a fast load transient of ±3A, V_{ESR} = ±3A × 0.8mΩ = ±2.4mV.

Capacitive undershoot (load increasing) is a function of the output capacitance, load step, inductor value, input-output voltage difference, and maximum duty factor. During a fast load transient, the maximum duty factor of Instant-PWM is a function of t_{ON} and the minimum t_{OFF} as the control scheme is designed to rapidly ramp the inductor current by grouping together many t_{ON} pulses in this case. The maximum duty factor D_{MAX} may be calculated as follows:

$$D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF,MIN}}$$

Given this, the capacitive undershoot may be calculated as follows:

$$V_{UNDERSHOOT,CAP} = -\frac{L_1 \times \Delta I_{OUT}^2}{2 \times C_{OUT} \times (V_{IN,MIN} \times D_{MAX} - V_{OUT})}$$

Consider a 3A load increase using the ceramic capacitors selected above when V_{IN} = 1.2V. At V_{OUT} = 0.6V, the result is t_{ON} = 830ns, $t_{OFF,MIN}$ = 260ns, D_{MAX} = 830 / (830 + 260) = 0.76 and

$$V_{UNDERSHOOT,CAP} = \frac{0.25\mu H \times (3A)^2}{2 \times 282\mu F \times (1.2V \times 0.76 - 0.6V)} = 12.8mV$$

Capacitive overshoot (load decreasing) is a function of the output capacitance, the inductor value and the output voltage.

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$$V_{OVERSHOOT,CAP} = \frac{L_1 \times \Delta I_{OUT}^2}{2 \times C_{OUT} \times V_{OUT}}$$

Consider a 3A load decrease using the ceramic capacitors specified above. At V_{OUT} = 0.6V the result is

$$V_{OVERSHOOT,CAP} = \frac{0.25\mu H \times (3A)^2}{2 \times 282\mu F \times 0.6V} = 6.6mV$$

Combine the ESR and capacitive undershoot and overshoot to calculate the total overshoot and undershoot for a given application.

Loop Compensation Considerations:

The SY26056 uses a transconductance amplifier for the error amplifier and supports a commonly used frequency compensation circuit. The compensation circuit is shown in Figure 16. The Type 2 circuit is normally implemented in high-bandwidth power supply designs using low-ESR output capacitors.

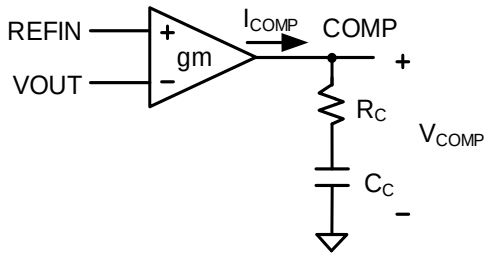

Figure 16. Loop Compensation Circuit

The design guidelines for the SY26056 loop compensation are as follows:

$$\frac{V_{COMP}}{I_{COMP}} = \frac{(1 + s \times R_C \times C_C)}{s \times C_C}$$

The R_C and C_C introduce a zero to the loop compensation. Increasing R_C will increase the bandwidth, while increasing C_C will decrease the bandwidth. With higher bandwidth, the IC will achieve faster dynamic response speed. However, the higher bandwidth will bring a lower stability margin. It is therefore a tradeoff for dynamic response and stability margin when selecting R_C and C_C. In addition, placing a capacitor (C_{C1}, with a much lower capacitance compared to C_C) between COMP and GND is recommended to reject high-frequency noise.

Thermal Design Considerations

The maximum power dissipation depends on multiple factors: PCB layout, IC package thermal resistance, local airflow, and the junction temperature relative to ambient. The maximum power dissipation may be calculated as:

$$P_{D,MAX} = \frac{(T_{J,MAX} - T_A)}{\theta_{JA}}$$

Where, $T_{J,MAX}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

To comply with the recommended operating conditions, the maximum junction temperature is 125℃. The junction to ambient thermal resistance θ_{JA} is layout dependent. For the QFN3.5×4-20 package the thermal resistance θ_{JA} is 30.5°C /W when measured on a standard Silergy four-layer thermal test board. These standard thermal test layouts have a very large area with long 2oz. copper traces connected to each IC pin and large, unbroken 1oz. internal power and ground planes.

To meet the performance of the standard thermal test board in a typical evaluation board area, wide copper traces are required well-connected to the IC's backside pads leading to exposed copper areas on the component side of the board as well as good thermal vias from the exposed pad connecting to a wide middle-layer ground plane, and perhaps, to an exposed copper area on the board's solder side.

The maximum power dissipation at T_A = 25°C may be calculated using the following formula:

$$P_{D,MAX} = \frac{(125℃ - 25℃)}{(30.5℃/W)} = 3.2W$$

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J,MAX}$ and thermal resistance θ_{JA}. Use the derating curve in Figure 12 below to calculate the effect of rising ambient temperature on the maximum power dissipation.

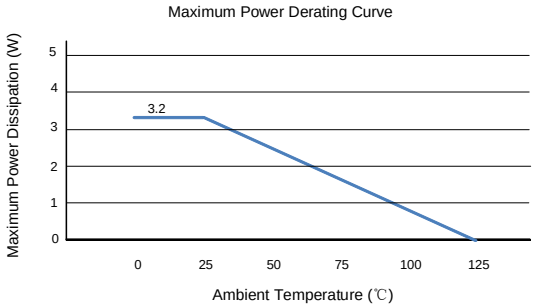

Figure 17. Maximum Power Derating Curve

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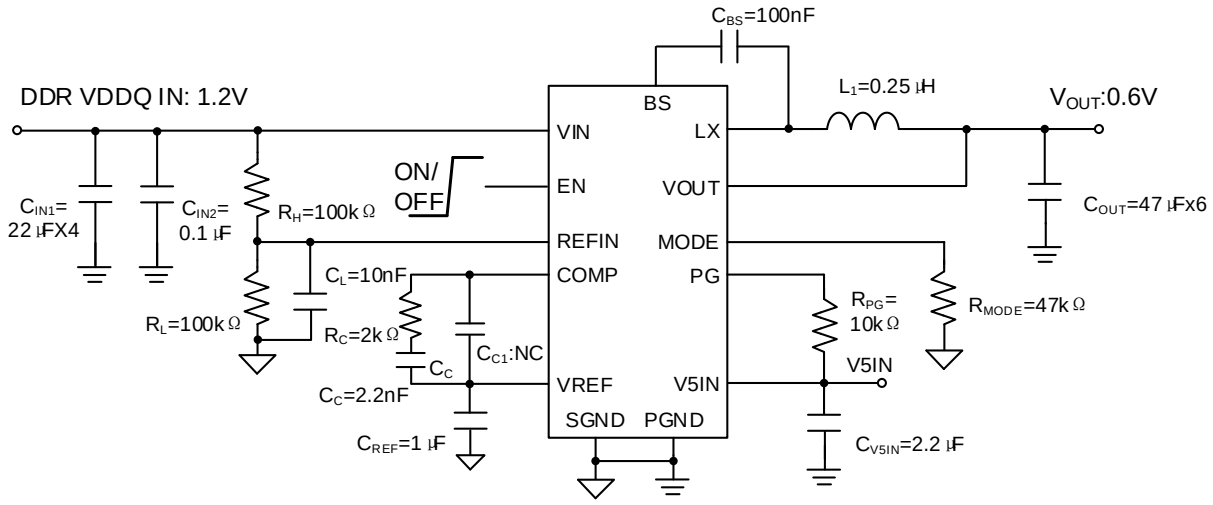
Application Schematic (V_{OUT} = 0.6V)



BOM List

Designator	Description	Part Number	Manufacturer
C_{IN1}	22μF/16V, X5R,1206	C3216X5R1C226K	TDK
C_{IN2}	0.1μF/50V, X7R, 0603	C1608X7R1H104K	TDK
C_{OUT}	47μF/6.3V, X5R,1206	C3216X5R0J476M	TDK
C_{REF}	1μF/16V, X7R,0603	C1608X7R1C105K	TDK
C_{BS}	100nF/50V, X7R,0603	C1608X7R1H104K	TDK
C_{V5IN}	2.2μF/16V, Y5V,0805	C1608Y5V1C225Z	TDK
C_C	2.2nF/50V, C0G,0603	C1608C0G1H222J	TDK
C_L	10nF/50V, X7R,0603	C1608X7R1H103K	TDK
L_1	0.25μH	SPM6530T-R25	TDK
R_H	100kΩ, 1%, 0603		
R_L	100kΩ, 1%, 0603		
R_{PG}	10kΩ, 1%, 0603		
R_{MODE}	47kΩ, 1%, 0603		
R_C	2kΩ, 1%, 0603		
C_{C1}	NC		

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Layout Design

Follow these PCB layout guidelines for optimal performance and thermal dissipation.

- Place the major MLCC capacitors (C_{IN}, C_{OUT}) on the same layer as the device.
- Place the input capacitors as close as possible to the V_{IN} and GND pins, minimizing the loop formed by these connections. Avoid using direct vias in the power trace between the input capacitors and V_{IN}, PGND to reduce parasitic inductance.
- Use a Kelvin connection between SGND and PGND.
- Use a Kelvin connection between the feedback sampling point and C_{OUT} (rather than connecting it to the inductor output terminal).
- Guarantee the C_{OUT} negative sides are connected with PGND pin by wide copper traces instead of vias, in order to achieve better accuracy and stability of output voltage.
- The LX connection has large voltage swings and fast edges, and can easily radiate noise to adjacent components. Keep its area small to prevent excessive EMI, while providing wide copper traces to minimize parasitic resistance and inductance. Keep sensitive components away from the switching node or provide ground traces between them for shielding, to prevent stray capacitive noise pickup.
- Place the BS capacitor on the same layer as the device; keep the BS voltage path (BS, LX, and C_{BS}) as short as possible.
- Provide dedicated wide copper traces for the power-path ground between the IC and the input and output capacitor grounds, rather than connecting each of these individually to an internal ground plane.
- Connect the exposed PGND pad to a large copper area and place several PGND vias on it for heat sinking and noise minimization.
- A four-layer layout is strongly recommended to achieve better thermal performance. For example, an 8.5cm × 8.5cm four-layer PCB with 2oz copper.
- Keep the high current traces (V_{IN}, PGND, LX, and V_{OUT} traces) as short and wide as possible.
- Provide large copper areas for V_{IN} and PGND on the top and bottom layers, and maximize their size. Middle1 layer should be used as the GND plane layer for conducting heat and shielding the Middle2 layer signal lines from top-layer crosstalk. Place signal lines on the Middle2 layer instead of the other layers to reduce any cuts in the GND planes on the other layers.

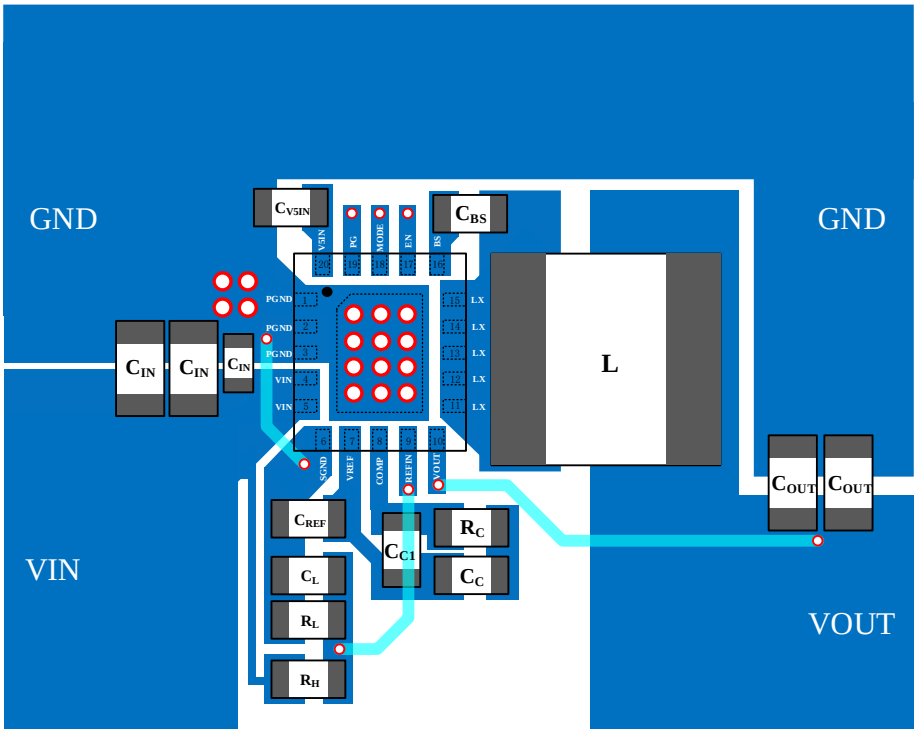

Figure 18. Suggested PCB Layout

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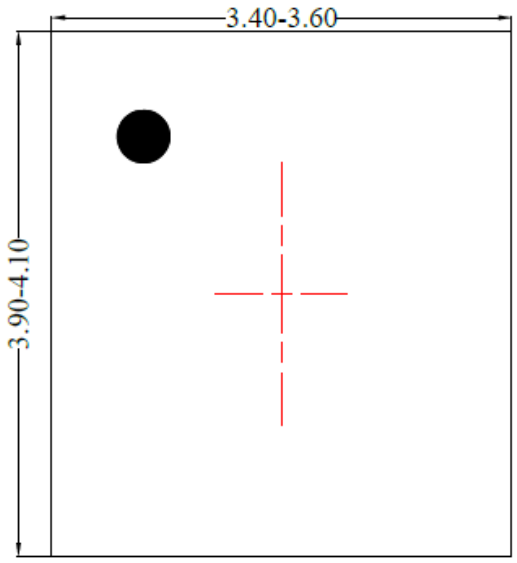
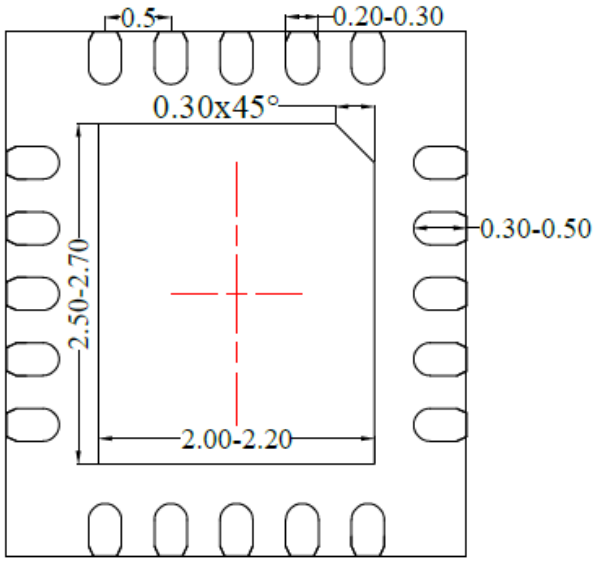
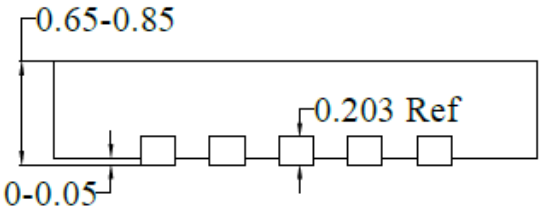
QFN3.5×4-20 Package Outline Drawing



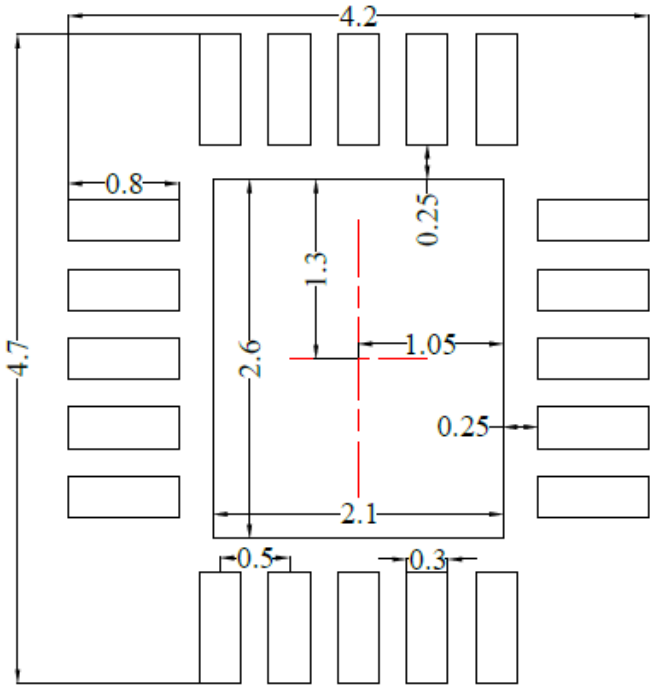
Top View



Bottom view



Side View



Recommended PCB layout

(reference only)

Note: *All dimensions are in millimeters and exclude mold flash and metal burr.*

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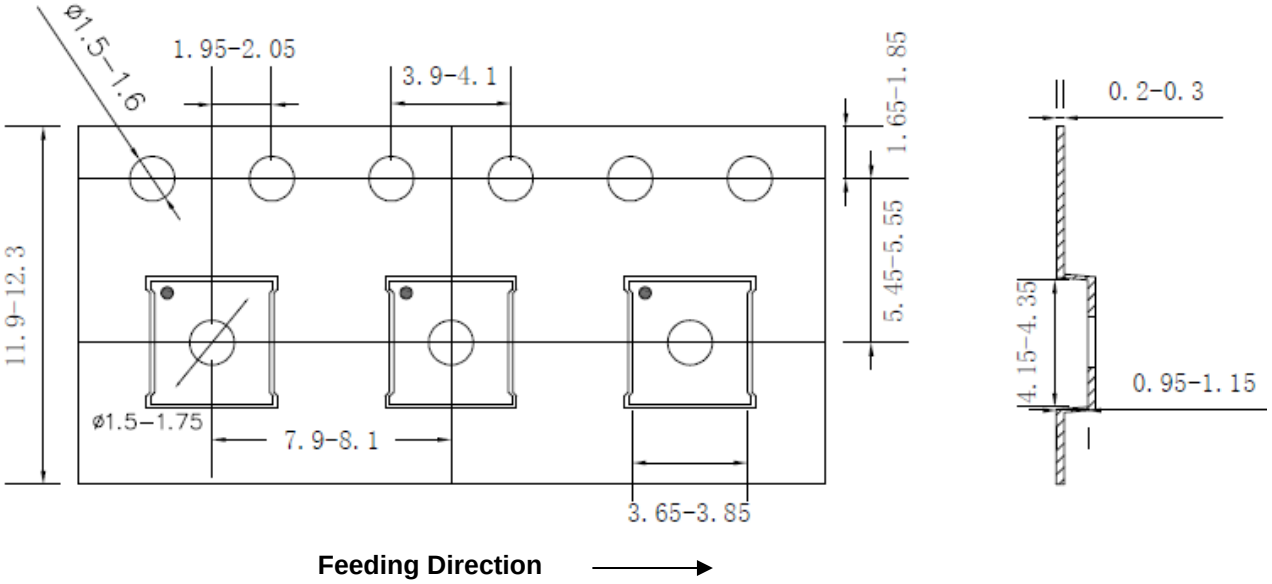
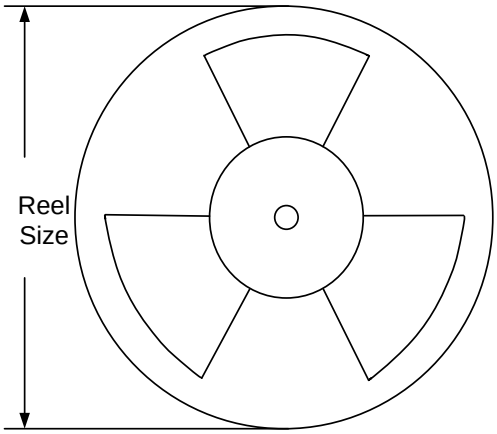
Taping and Reel Specification

QFN3.5×4 Package Orientation



Carrier tape and reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN3.5×4	12	8	13"	400	400	5000

Others: NA

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Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Sep.26, 2021	Revision 0.9	Initial Release
Sep.26, 2022	Revision 1.0	Production Release

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