SY26532

High Efficiency 1MHz, 2A Step-Up Regulator

General Description

The SY26532 high efficiency DC-to-DC step-up regulator operates using current mode control, and can deliver 2A current over a wide input voltage range from 3V to 30V. It integrates an N-channel MOSFET with low 200mΩ $R_{DS(ON)}$ to minimize conduction loss.

The 1MHz switching frequency and internal compensation reduce external inductor and capacitor sizes, and the built-in internal soft-start circuitry minimizes inrush current at startup.

The SY26532 is available in a compact SOT23-6 package.

Features

- 3V to 30V Bias Input Voltage Range, $33V_{OUT,MAX}$
- Up to 2A Output Current
- Quiescent Current I_Q 100 µA (typ.)
- Shutdown Current I_{SHDN} 5 µA (typ.)
- Low $R_{DS(ON)}$ for Internal N-Channel MOSFET: 200mΩ
- 1MHz Switching Frequency
- Minimum On-Time: 100ns Typical
- Minimum Off-Time: 100ns Typical
- Internal Soft-Start Limits Inrush Current
- ±2% 0.6V Reference
- RoHS-Compliant and Halogen-Free
- Compact SOT23-6 Package

Applications

- Digital Camera
- Cell Phone
- PDA, PMP, MP3

Typical Application

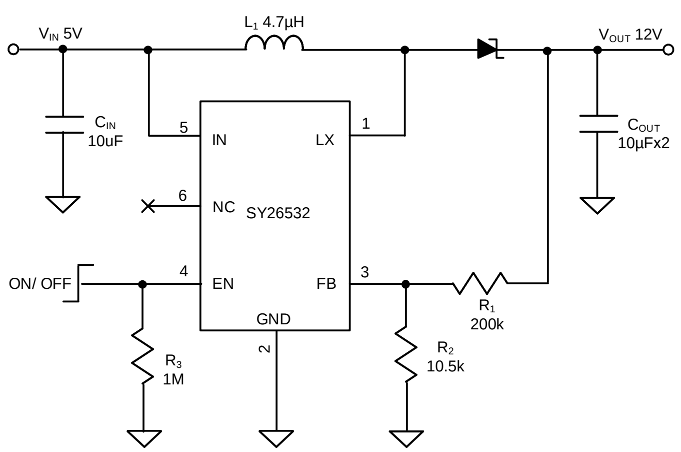


Figure 1. Typical Application Circuit

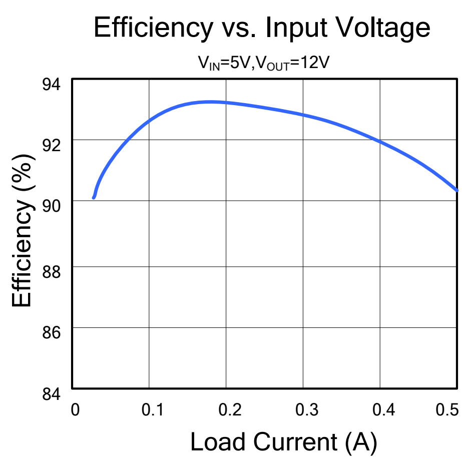


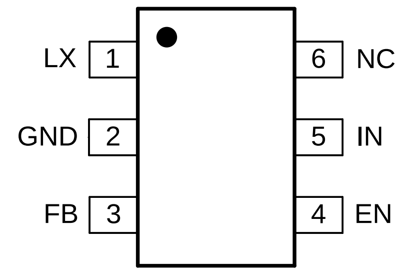
Figure 2. Efficiency vs. Output Current

Ordering Information

Ordering Part Number	Package type	Top Mark
SY26532ABC	SOT23-6 RoHS-Compliant and Halogen-Free	**9Q*xyz***

x = year code, y = week code, z = lot number code

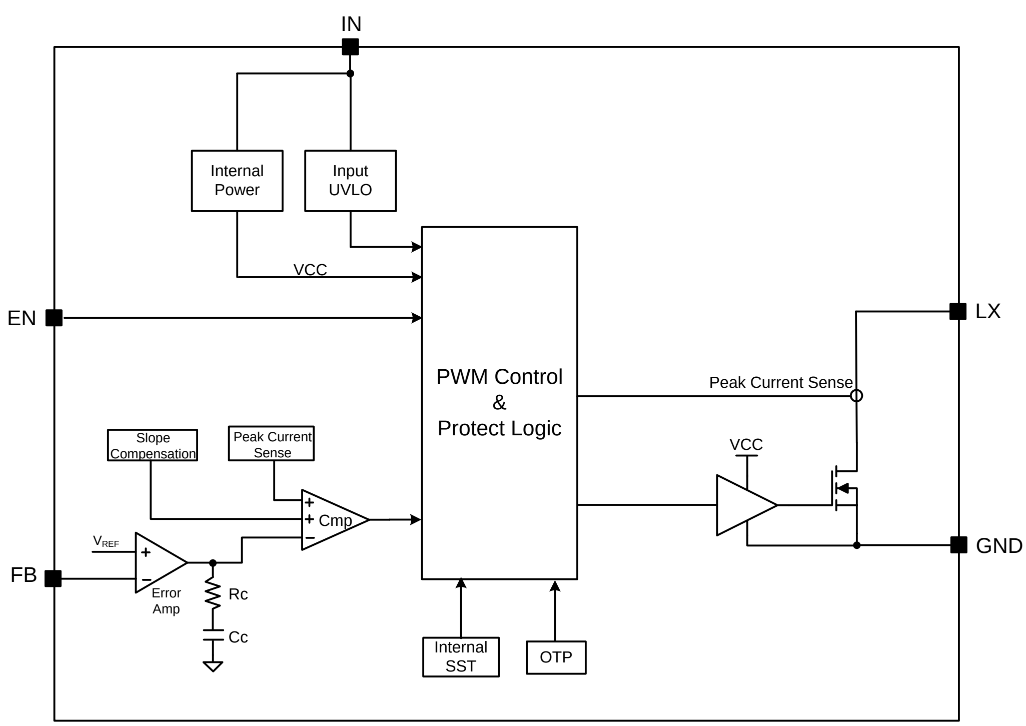
Pinout (top view)



Pin Description

Pin Number	Pin Name	Pin Description
1	LX	Inductor node. Connect an inductor between the IN and LX pins.
2	GND	Ground pin.
3	FB	Feedback pin. Connect a resistor R1 between V_{OUT} and FB, and a resistor R2 between FB and GND to program the output voltage: $V_{OUT} = 0.6V \times (R1/R2+1)$.
4	EN	Enable pin. Pull low to disable the device, pull high to enable. Do not leave this pin floating.
5	IN	Input pin. Decouple this pin to the GND pin with a 1µF ceramic capacitor.
6	NC	No connection.

Block Diagram



Absolute Maximum Ratings

Parameter (Note1)	Min	Max	Unit
LX	-0.3	36	V
IN, EN	-0.3	33	
FB	-0.3	4	
Lead Temperature (Soldering, 10 sec.)		260	°C
Junction Temperature, Operating	-40	150	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	161	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	130	
P_D Power Dissipation T_A= 25°C	0.6	W

Recommended Operating Conditions

Parameter (Note3)	Min	Max	Unit
IN	3	30	V
Junction Temperature, Operating	-40	125	°C
Ambient Temperature	-40	85	

Electrical Characteristics

(V_{IN} = 5V, V_{OUT} = 12V, I_{OUT} = 100mA, T_J = -40°C to +125°C. Typical values are at T_J = 25°C, unless otherwise specified. The values are guaranteed by test, design or statistical correlation.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		3		30	V
IN UVLO Rising Threshold	$V_{IN,UVLO}$		1.3		2.2	V
Quiescent Current	I_Q	V_{FB} = 0.66V		100	150	μA
Shutdown Current	I_{SHDN}	EN = 0		5	20	μA
Low Side Main FET R_{ON}	$R_{DS(ON)}$			200	320	mΩ
Main FET Current Limit	I_{LIM1}		2		3	A
Main FET Leakage Current	I_{LK}	EN = 0			1	μA
Switching Frequency	f_{SW}		0.8	1	1.32	MHz
Feedback Reference Voltage	V_{REF}		0.582	0.6	0.618	V
EN Rising Threshold	V_{ENH}		1.5			V
EN Falling Threshold	V_{ENL}				0.4	V
Maximum Duty Cycle	D_{MAX}		85	90		%
Minimum On-Time	$t_{ON, MIN}$			100	150	ns
Minimum Off-Time	$t_{OFF, MIN}$			10%	15%	T_S
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			10		°C

Note 1: Stresses beyond "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

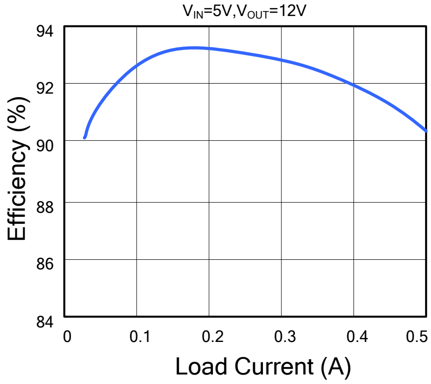
Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

(T_A= 25℃, V_{IN}=5V, V_{OUT} = 12V, L = 4.7μH, C_{OUT}= 20μF, unless otherwise specified.)

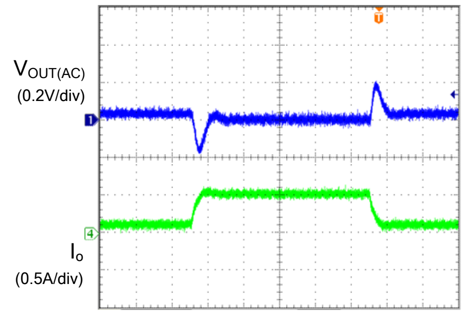
Efficiency vs. Input Voltage

(V_{IN}=5V,V_{OUT}=12V)



Load Transient

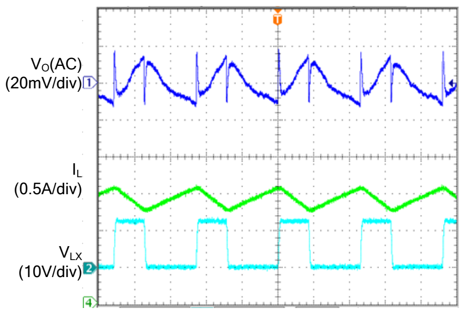
(V_{IN}=5V, V_{OUT}=12V,I_{load}=0.1~0.5A)



Time(100us/div)

Output Ripple

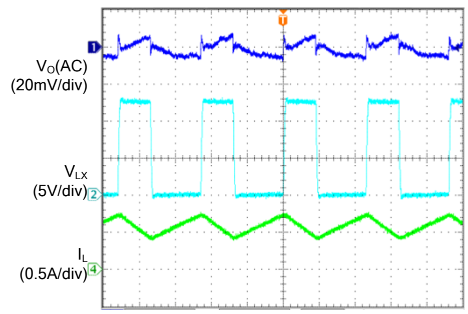
(V_{IN}=5V, V_{OUT}=12V,I_{load}=0.5A)



Time(400ns/div)

Output Ripple

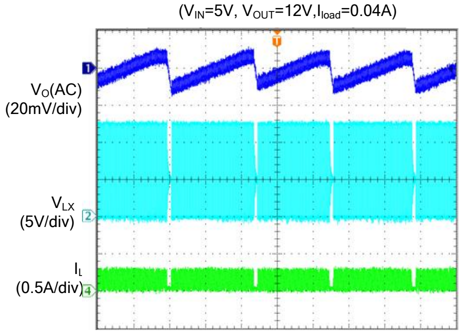
(V_{IN}=5V, V_{OUT}=12V,I_{load}=0.2A)



Time(400ns/div)

Output Ripple

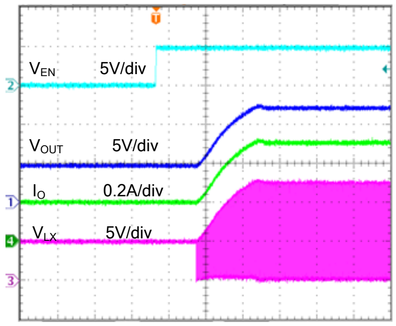
(V_{IN}=5V, V_{OUT}=12V,I_{load}=0.04A)



Time(40us/div)

Startup from Enable

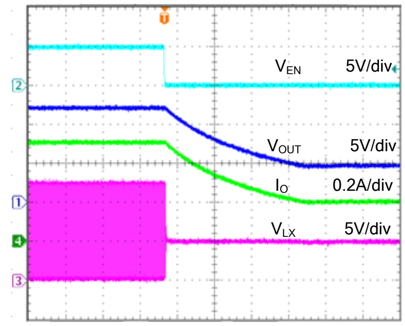
f=10Hz, V_{IN}=5V,V_{OUT}=12V,I_O=0.5A



Time (100us/div)

Shutdown from Enable

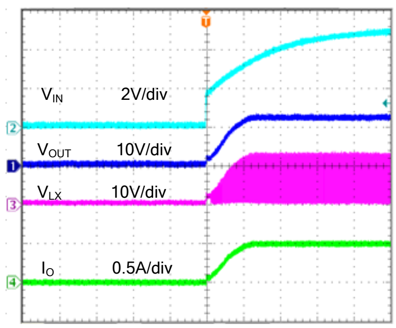
f=10Hz, V_{IN}=5V,V_{OUT}=12V,I_O=0.5A



Time (100us/div)

Startup from V_{IN}

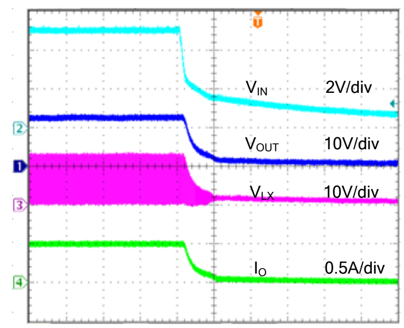
V_{IN}=5V,V_{OUT}=12V,I_O=0.5A



Time (2ms/div)

Shudown from V_{IN}

V_{IN}=5V,V_{OUT}=12V,I_O=0.5A



Time (2ms/div)

Detailed Description

The SY26532 high efficiency DC-to-DC step-up regulator operates using current mode control, and can deliver 2A current over a wide input voltage range from 3V to 30V. It integrates an N-channel MOSFET with low 200mΩ $R_{DS(ON)}$ to minimize conduction loss.

The 1MHz switching frequency and internal compensation reduce external inductor and capacitor sizes, and the built-in internal soft-start circuitry minimizes inrush current at startup.

The SY26532 is available in a compact SOT23-6 package.

Enable Operation

Driving the EN pin high (>1.5V) enables normal operation. Driving the EN pin low (<0.4V) will shut down the device. During shutdown mode, the SY26532 shutdown current drops to less than 5μA (typ.).

Soft-Start (EN Control)

The SY26532 has a built-in soft-start to control the rising slew rate of the output voltage and limit the input current surge during IC startup. With a 200μs turn-on delay time before the initial soft-start, the typical soft-start time is 1ms.

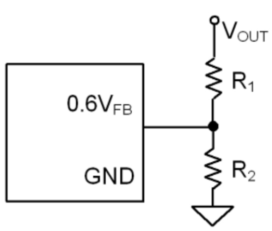
Application Information

The following paragraphs describe the selection process for the feedback resistors (R1 and R2), input capacitor C_{IN}, output capacitor C_{OUT}, boost inductor L, and diode D.

Feedback Resistor-Divider R1 and R2

Choose R1 and R2 to program the proper output voltage. Choose large resistance values between 10kΩ and 1MΩ for both R1 and R2 to minimize power consumption under light loads. If a value is chosen for R1, then R2 can be calculated as:

$$R2 = \frac{0.6V}{V_{OUT}\text{-}0.6V} R1$$



Input Capacitor C_{IN}

Input filter capacitors reduce the ripple voltage on the input, filter the switched current drawn from the input supply, and reduce potential EMI. When selecting an input capacitor, be sure to select a voltage rating at least 20% greater than the maximum voltage of the input supply and a temperature rating higher than the system requirements. X5R series ceramic capacitors are most often selected due to their small size, low cost, surge-current capability, and high RMS current ratings over a wide temperature and voltage range. However, systems that are powered by a wall adapter or other long and therefore inductive cabling may be susceptible to significant inductive ringing at the input to the device. In these cases, consider adding some bulk capacitance like electrolytic, tantalum, or polymer type capacitors. Using a combination of bulk capacitors (to reduce overshoot or ringing) in parallel with ceramic capacitors (to meet the RMS current requirements) is helpful in these cases.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

$$I_{CIN\_RMS} = \frac{V_{IN} \cdot (V_{OUT} - V_{IN})}{2\sqrt{3} \cdot L \cdot F_{SW} \cdot V_{OUT}}$$

For the best performance, select a typical X5R or better grade low ESR 10μF ceramic capacitor and place it as close as possible to the IN and GND pins. Minimize the loop area formed by C_{IN} and the IN/GND pins.

Output Capacitor C_{OUT}

Select the output capacitor C_{OUT} to handle the output ripple requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting the component. For the best performance, use an X5R or better grade ceramic capacitor with a 50V rating and capacitance of at least 22μF.

For applications where the design must meet stringent ripple requirements, the following considerations must be followed:

The output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔI_L) on the output capacitor's ESR (ESR ripple), as well as the stored charge (capacitive ripple). When calculating total ripple, both should be considered.

$$V_{RIPPLE,\ ESR1} = I_{LPEAK} \times ESR$$

$$V_{RIPPLE,\ ESR2} = I_{LVALLEY} \times ESR$$

$$V_{RIPPLE,CAP} = \frac{I_{OUT} \times (1\text{-}D)}{C_{OUT} \times f_{SW}}$$

The capacitive ripple might be higher because the effective capacitance for ceramic capacitors decreases with the voltage across the terminals. The voltage derating is usually included as a chart in the capacitor datasheet, and the ripple can be recalculated after taking the target output voltage into account.

Boost Inductor L

Consider the following when choosing this inductor:

1) Choose the inductance to provide a ripple current that is approximately 40% of the maximum output current. The recommended inductance is calculated as:

$$L = \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \frac{V_{OUT} - V_{IN}}{f_{SW}\, I_{OUT,MAX} \times 0.4}$$

where f_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY26532 has high tolerance for ripple current amplitude variation. As a result, the final choice of inductance can vary slightly from the calculated value with no significant performance impact.

2) The inductor's saturation current rating must be greater than the peak inductor current under full load:

$$I_{SAT,MIN} = \left(\frac{V_{OUT}}{V_{IN}}\right) \times I_{OUT,MAX} + \frac{V_{IN}(V_{OUT} - V_{IN})}{2 \times f_{SW} \times L \times V_{OUT}}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. Choose an inductor with DCR less than 50mΩ to achieve good overall efficiency.

Rectifier Diode

For high efficiency, choose a Schottky diode with low forward voltage drop and fast reverse recovery.

The reverse breakdown voltage of the Schottky diode should be greater than the output voltage.

Light Load Operation

The SY26532 operates in burst mode during light load conditions to maintain high-efficiency. DCM operation is automatically initiated when the inductor current falls to zero. As the load decreases further the resulting switching frequency will also decrease in order to keep the output close to the target value.

Overcurrent Protection

The SY26532 provides cycle by cycle overcurrent protection and turns off the power MOSFET once the inductor current reaches the overcurrent limit threshold. The limit status resets itself at the beginning of the next switching cycle. During the overcurrent protection, the output voltage drops as a function of the load on the output.

Thermal protection

The SY26532 includes over temperature protection circuitry to prevent overheating due to excessive power dissipation. This will shut down the device when the junction temperature exceeds 150°C. Once the junction temperature cools down by approximately 10°C, the device will resume normal operation after a complete soft-start cycle. For continuous operation, provide adequate cooling so that the junction temperature does not exceed the thermal protection threshold.

Applications with Large Bulk Capacitance

In applications with large bulk capacitance present on the output, a very high inrush current could flow through the inductor during power-on. In order to limit the current flowing into the device and prevent damage, a Schottky diode connected from the power input to the output or an RC delay circuit added on the EN pin are recommended, as shown in Figure 3.

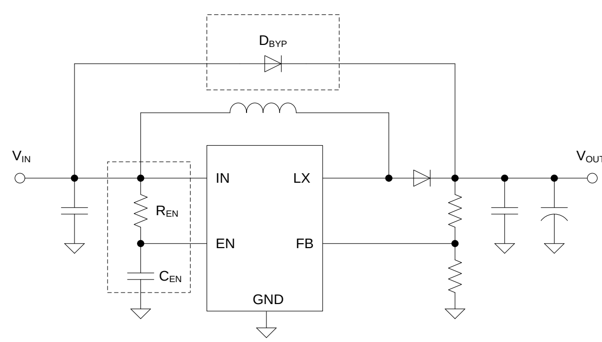
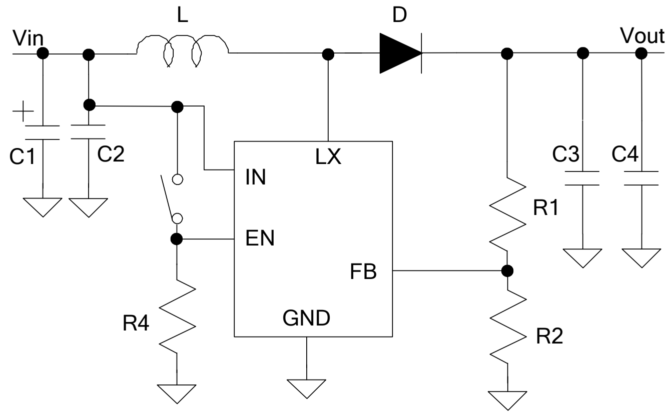


Figure 3. Inrush Current Limiting

Application Schematic



Design Specifications

Input Voltage (V)	Output Voltage(V)	Input Current Limit (A)
3–12	12	2

BOM List

Reference Designator	Description	Part Number	Manufacturer
U1		SY26532ABC	
L	4.7μH/3.8A	VLC6045-4R7M	TDK
C1	47μF/50V, EC		
C2, C3, C4	10μF/25V 1206	C3216X7R1E106K	TDK
R1	200k ,1%, 0603	RC0603FR-07200KL	YAGEO
R2	10.5k, 1%, 0603	RC0603FR-0710K5L	YAGEO
R3	0Ω,1%, 0603	RC0603FR-070RL	YAGEO
R4	1M, 1%, 0603	RC0603FR-071ML	YAGEO
D	3A/40V, Schottky	SS34	

Recommend Components for Typical Applications

V_{OUT}(V)	R1(kΩ)	R2(kΩ)	L(μH)	C_{OUT}
12	200	10.5	4.7	2×10μF/25V/X7R,1206
24	200	5.1	6.8	2×10μF/50V/X7R,1206

Layout Design

To achieve optimal design, follow these PCB layout considerations:

- Place C_{IN}, L, R1, and R2 close to the IC
- To achieve the best thermal and noise performance, maximize the PCB copper area connecting to the GND pin. A ground plane is highly recommended if board space allows.
- C_{IN} must be close to pins IN and GND. Minimize the loop area formed by C_{IN} and GND.
- To reduce the switching noise, minimize the PCB copper area connected to the LX pin.
- In order to reduce crosstalk, R1, R2, and the trace connected to the FB pin must not be adjacent to the LX net on the PCB layout.
- If the system chip interfacing with the EN pin has a high impedance state during shutdown mode, and the IN pin is connected directly to a power source such as a Li-ion battery, add a 1MΩ pulldown resistor between the EN and GND pins to prevent noise from falsely triggering the regulator during shutdown mode.

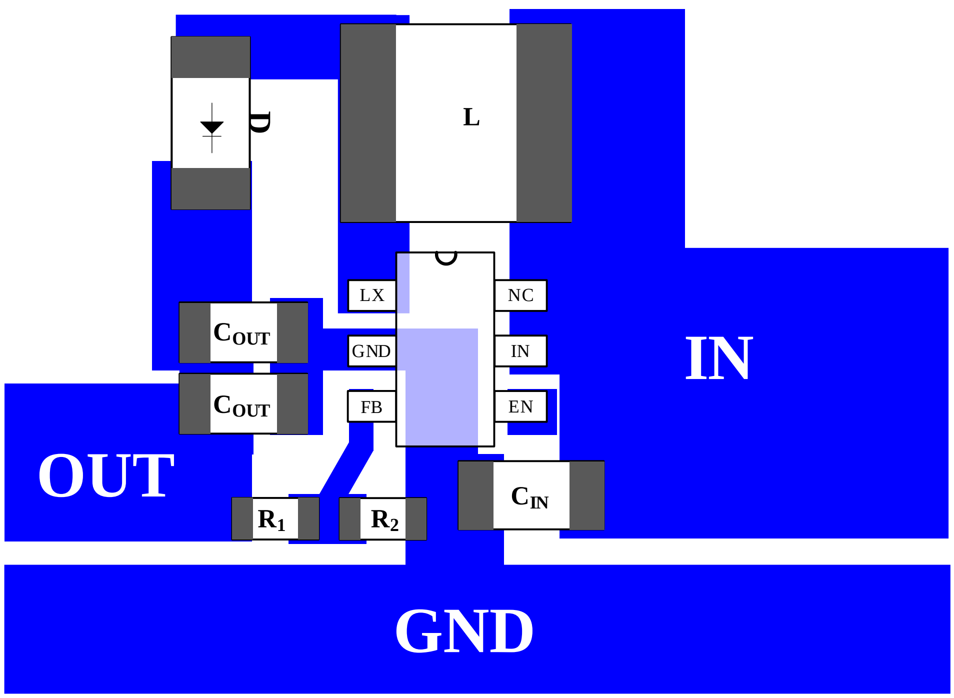
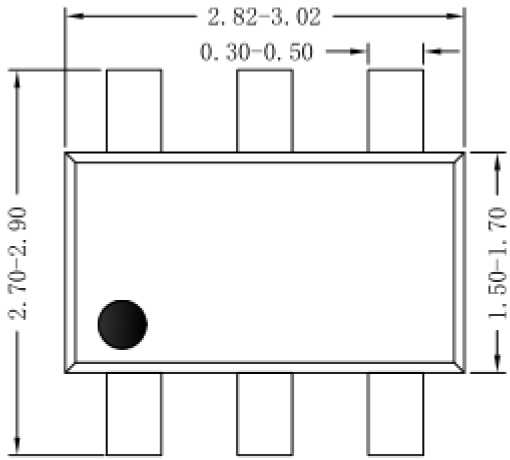
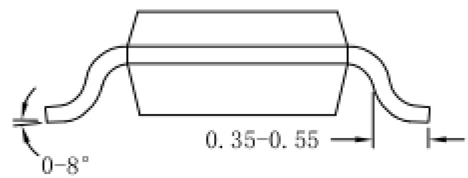


Figure 4. Suggested PCB Layout

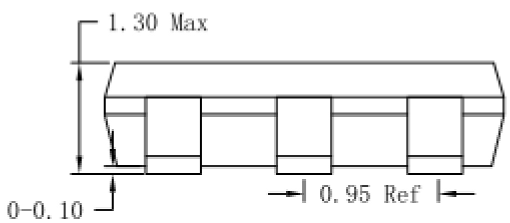
SOT23-6 Package Outline and PCB Layout



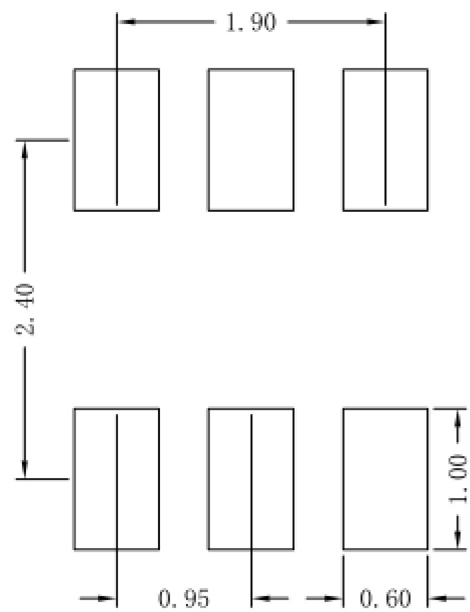
Top view



Side view



Side view

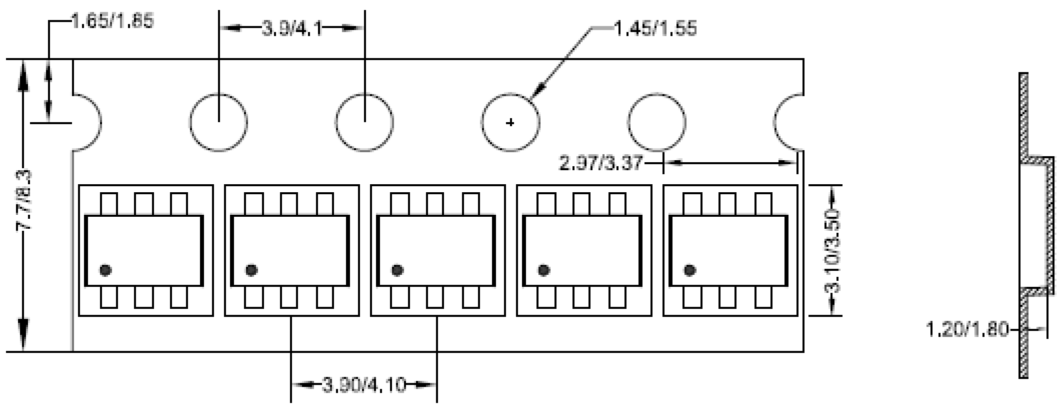


Recommended pad layout (reference only)

Note: *All dimensions are in millimeters and exclude mold flash and metal burr.*

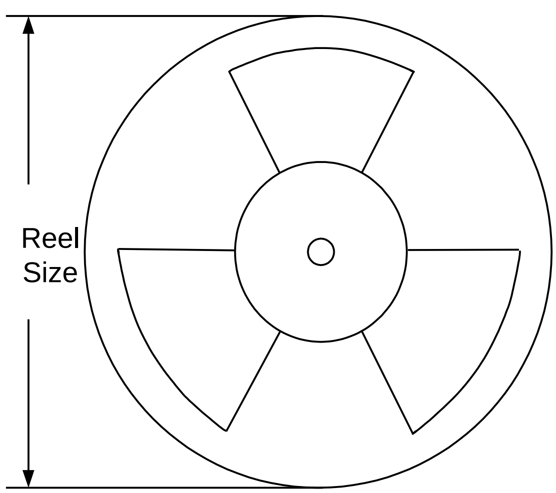
Taping and Reel Specification

SOT23-6 taping orientation



Feeding direction →

Carrier tape and reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SOT23-6	8	4	7"	280	160	3000

Others: NA

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
June 05, 2023	Revision 1.0	Production Release
June 03, 2020	Revision 0.9	Initial Release

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