SY20775

Sink and Source DDR Termination Regulator

General Description

The SY20775 is a sink and source double data rate memory (DDR) regulator designed for applications that require very low noise and low input voltage systems.

It supports power requirements for DDR, DDR2, DDR3, DDR3L, and DDR4 VTT BUS termination, and it uses remote sensing for increased output voltage accuracy and a fast transient response. Additionally, it has an enable pin to control VTT discharge during low power modes in DDR applications, and a PGOOD pin to monitor output regulation.

The SY20775 is available in a DFN 3mm×3mm-10pin package with exposed thermal pad and it operates over a temperature range of -40°C to 85°C.

Features

- System Voltage Range (VIN): 2.35V to 3.5V
- Wide VLDOIN Voltage Range: 1.1V to 3.5V
- Current Source/Sink Capability: 3A/3.5A
- PGOOD Pin Monitors Output Regulation
- Output Voltage Remote Sensing (VOSNS)
- REFIN Input Allows Flexible Input Voltage Tracking
- Output Current Limit Setting
- Thermal Shutdown Protection
- ±10mA Buffered Reference (REFOUT)
- Supports DDR, DDR2, DDR3, DDR3L, DDR4 VTT Applications
- Package: DFN3×3-10 with Thermal Pad

Applications

- Memory Termination Regulator for DDR, DDR2, DDR3, DDR3L, and DDR4 Applications
- Notebooks, Desktops, and Servers
- Base Stations

Typical Application

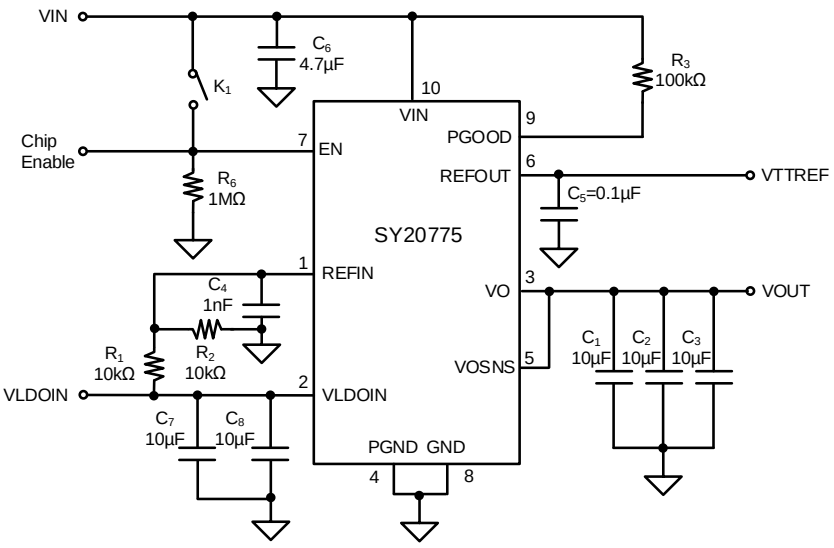


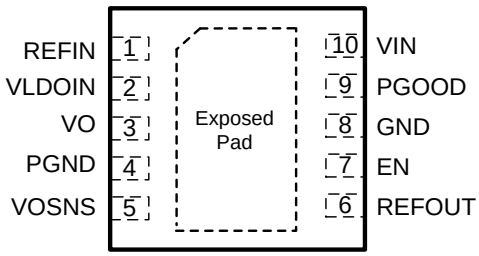
Figure 1. Schematic Diagram

Ordering Information

Ordering Part Number	Package Type	Top Mark
SY20775DBD	DFN3×3-10 RoHS Compliant and Halogen Free	**DRFxyz**

x=year code, y=week code, z= lot number code

Pinout (top view)



Pin Description

Pin Name	Pin Name	Pin Description
REFIN	1	Reference input. Connect to GND through a 0.1μF ceramic capacitor.
VLDOIN	2	Supply voltage for the LDO. Use a 10μF (or greater) ceramic capacitor.
VO	3	Power output pin for the LDO. For stable operation, the total capacitance of the VO output pin must be greater than 20μF. Attach three 10μF ceramic capacitors in parallel to reduce the series resistance (ESR) and equivalent series inductance (ESL).
PGND	4	Power ground pin for the LDO.
VOSNS	5	Voltage sense input for the LDO. Connect with a separate trace to the load.
REFOUT	6	Reference output. Connect to GND Through a 0.1uF ceramic capacitor.
EN	7	Enable input. Driving this pin high turns on the regulator. Driving this pin low shuts off the regulator. For the DDR VTT applications, connect EN to the low power mode input (SLP S3). Do not leave it floating.
GND	8	Signal ground pin.
PGOOD	9	Open drain power-good indicator: The output is in Hi-Z when the VO output is within ±20% of REFOUT.
VIN	10	Input supply pin. Place a large bulk capacitance close to this pin to ensure the input supply does not sag below the minimum VIN. A ceramic decoupling capacitor with a value between 1uF and 4.7μF can be used for most applications.
Exposed Pad	/	The exposed pad should be connected to the ground plane for improved thermal performance.

Block Diagram

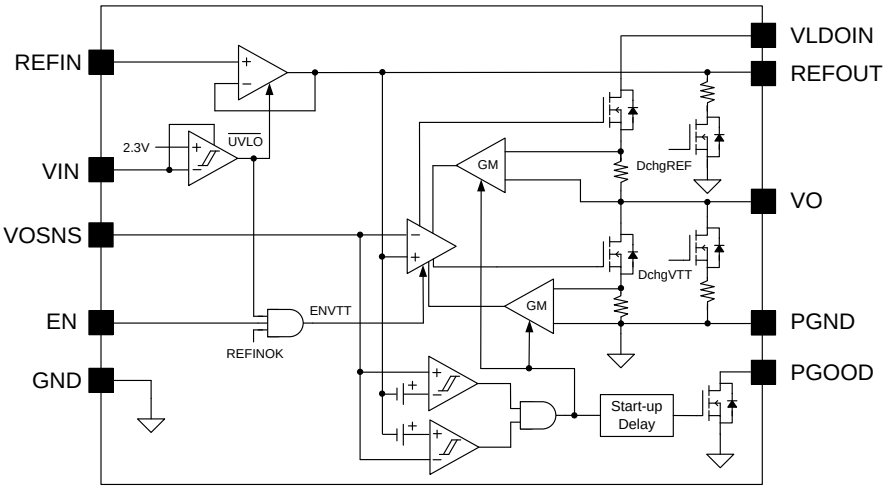


Figure 2. Block Diagram

Absolute Maximum Ratings

Parameter (Note1)	Min	Max	Unit
REFIN, REFOUT, VIN, VO, VLDOIN, VOSNS	-0.3	3.6	V
EN, PGOOD	-0.3	6.5	
PGND	-0.3	0.3	
Lead Temperature (Soldering, 10 sec.)		260	°C
Junction Temperature, Operating	-40	150	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note2)	Typ	Unit
θ_{JA} Junction-to-ambient Thermal Resistance	54.7	°C/W
θ_{JC} Junction-to-case Thermal Resistance	45.5	
P_D Power Dissipation T_A=25°C	1.8	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
VIN	2.375	3.5	V
EN, VLDOIN, VOSNS	-0.1	3.5	
REFIN	0.5	1.8	
PGOOD, VO	-0.1	3.5	
REFOUT	-0.1	1.8	
PGND	-0.1	0.1	
Junction Temperature, Operating	-40	125	°C
Ambient Temperature	-40	85	

Electrical Characteristics

(V_{VIN}=3.3V, V_{VLDOIN}=1.8V, V_{REFIN}=0.9V, V_{VOSNS}=0.9V, V_{EN}=V_{VIN}, C_{OUT}=3×10μF, T_A=-40°C to 125°C, typical values are T_A=25°C, unless otherwise specified. The values are guaranteed by test, design, or statistical correlation)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current	I_{IN}	V_{EN} = 3.3V, No Load		0.7	1	mA
Shutdown Current	$I_{IN(SDN)}$	V_{EN} = 0V, V_{REFIN} = 0V, No Load		65	80	μA
		V_{EN} = 0V, V_{REFIN} > 0.4V, No Load		200	400	
Supply Current of VLDOIN	I_{LDOIN}	V_{EN} = 3.3V, No Load		1	50	μA
Shutdown Current of VLDOIN	$I_{LDOIN(SDN)}$	V_{EN} = 0V, No Load		0.1	50	μA
Input Current of REFIN	I_{REFIN}	V_{EN} = 3.3V			1	μA
Output DC Voltage of VO	V_{VOSNS}	V_{REFOUT} = 1.25V(DDR1), I_O = 0A		1.25		V
			-15		15	mV
		V_{REFOUT} = 0.9V(DDR2), I_O = 0A		0.9		V
			-15		15	mV
		V_{REFOUT} = 0.75V(DDR3), I_O = 0A		0.75		V
			-15		15	mV
		V_{REFOUT} = 0.675V(DDR3L), I_O = 0A		0.675		V
			-15		15	mV
		V_{REFOUT} = 0.6V(DDR4), I_O = 0A		0.6		V
			-15		15	mV
Output Voltage Tolerance to REFOUT	V_{VOTOL}	V_{LDOIN}=1.50V, V_{OUT}=0.75V, --2 A< I_{VO} < 2 A	-20		20	mV
		V_{LDOIN}=1.35V, V_{OUT}=0.675V, --2 A< I_{VO} < 2 A	-20		20	
		V_{LDOIN}=1.20V, V_{OUT}=0.6V, --2 A< I_{VO} < 2 A	-20		20	
VO Source Current Limit	I_{VOSRCL}	V_{OSNS} = 0.9 ×V_{REFOUT}, T_A=25°C	3		4.5	A
VO Sink Current Limit	I_{VOSNCL}	V_{OSNS} = 1.1 ×V_{REFOUT}, T_A=25°C	3.5		5.5	A
OUT Shutdown Discharge Resistance	R_{DSCHRG}	V_{REFIN} = 0 V, V_{VO} = 0.3 V, V_{EN} = 0 V		18	25	Ω
VO PGOOD Threshold	$V_{TH(PG)}$	PGOOD window lower threshold with respect to REFOUT	-23.5%	-20%	-17.5%	
		PGOOD window upper threshold with respect to REFOUT	17.5%	20%	23.5%	
		PGOOD hysteresis		5%		
PGOOD Start-up Delay	$T_{PGSTUPDLY}$	Start-up rising edge, VOSNS within 15% of REFOUT		2		ms
PGOOD Output Low Voltage	$V_{PGOODLOW}$	I_{SINK} = 4 mA			0.4	V
PGOOD Bad Delay	$T_{PBADDLY}$	VOSNS is outside of the ±20% PGOOD window		10		μs
Leakage Current	$I_{PGOODLK}$	V_{OSNS} = V_{REFIN}(PGOOD high impedance), V_{PGOOD} =V_{VIN} + 0.2V			1	μA
REFIN Voltage Range	V_{REFIN}		0.5		1.8	V
REFIN Under Voltage Lockout	$V_{REFINUVLO}$	REFIN rising	360	390	420	mV

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
REFIN Under Voltage Lock Out Hysteresis	$V_{REFIN-UVHYS}$			20		mV
REFOUT Voltage	V_{REFOUT}			REFIN		V
REFOUT Voltage Tolerance to V_{REFIN}	$V_{REFOUTTOL}$	-10 mA< I_{REFOUT} < 10 mA, V_{REFIN} = 1.25 V	-15		15	mV
		-10 mA< I_{REFOUT} < 10 mA, V_{REFIN} = 0.9 V	-15		15	
		-10 mA< I_{REFOUT} < 10 mA, V_{REFIN} = 0.75 V	-15		15	
		-10 mA< I_{REFOUT} < 10 mA, V_{REFIN} = 0.675 V	-15		15	
		-10 mA< I_{REFOUT} < 10 mA, V_{REFIN} = 0.6 V	-15		15	
REFOUT Source Current Limit	$V_{REFOUT-SRCL}$	V_{REFOUT} = 0 V	10	40		mA
REFOUT Sink Current Limit	$I_{REFOUT-SNCL}$	V_{REFOUT} = 0 V	10	40		mA
UVLO Threshold	$V_{VINUVVIN}$	Wake up	2.2	2.3	2.375	V
		Hysteresis		50		mV
High-level Input Voltage	V_{ENIH}	Enable	1.2			V
Low-level Input Voltage	V_{ENIL}	Enable			0.3	
Hysteresis Voltage	V_{ENYST}	Enable		0.1		
Logic Input Leakage Current	I_{ENLEAK}	Enable	-1		1	μA
Thermal Shutdown Threshold	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			20		°C

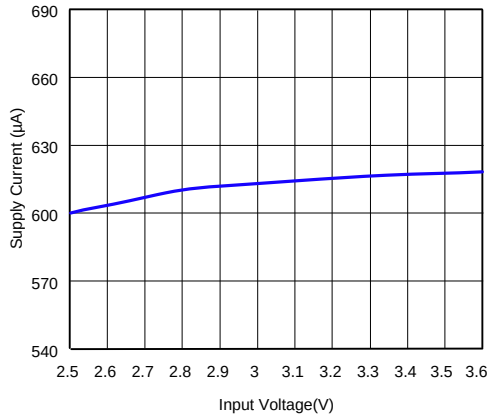
Note 1: Stresses beyond "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a Silergy EVB test board.

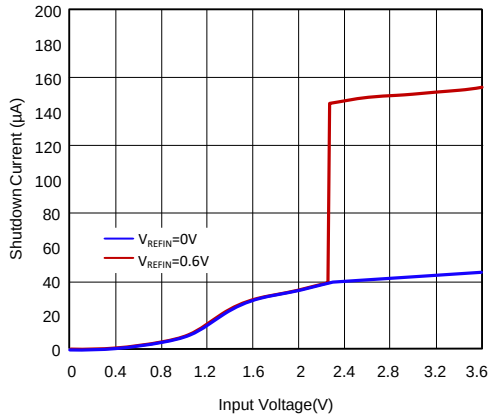
Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

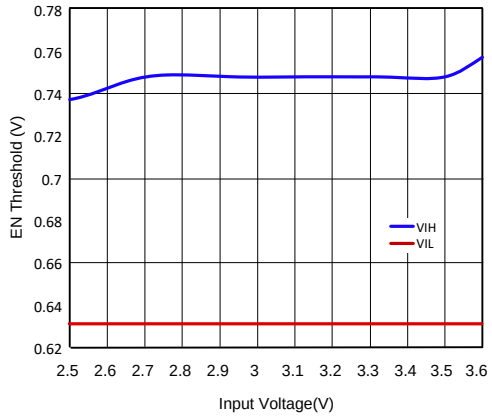
Supply Current vs. Input Voltage
(V_{LDOIN}=1.2V, V_{REFIN}=0.6V, EN ON, Null load)



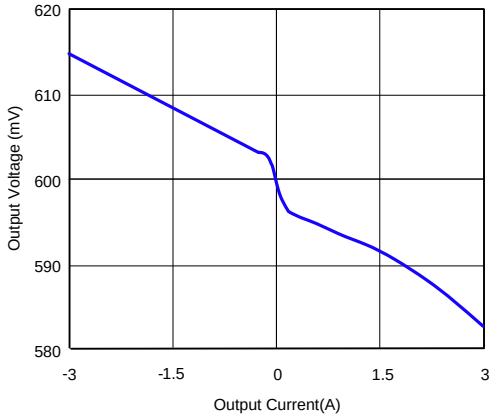
Shutdown Current vs. Input Voltage
(V_{EN}=0V, Null load)



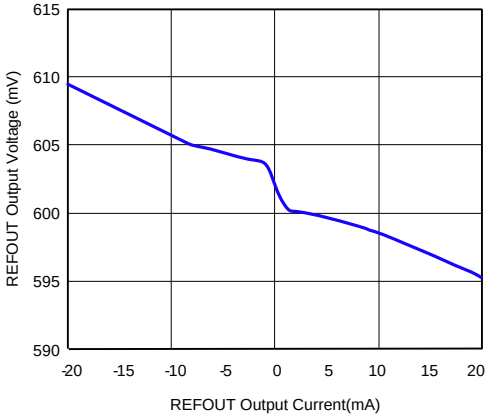
EN Threshold vs. Input Voltage
(V_{LDOIN}=1.2V, V_{REFIN}=0.6V, Null load)



OUT Load Regulation
(V_{IN}=3.3V, V_{LDOIN}=1.2V, V_{REFIN}=0.6V)

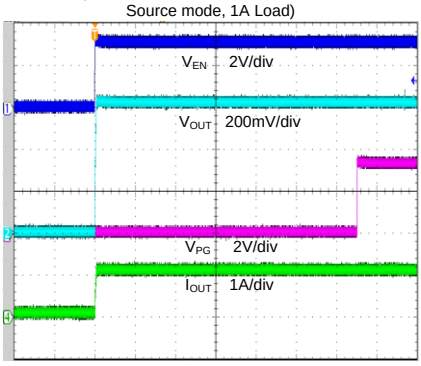


REFOUT Load Regulation
(V_{IN}=3.3V, V_{LDOIN}=1.2V, V_{REFIN}=0.6V)



Startup From Enable

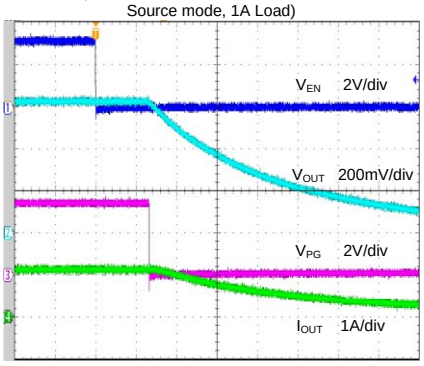
(V_{IN}=3.3V, V_{LDOIN}=1.2V, V_{REFIN}=0.6V, Source mode, 1A Load)



Time(400μs/div)

Shutdown From Enable

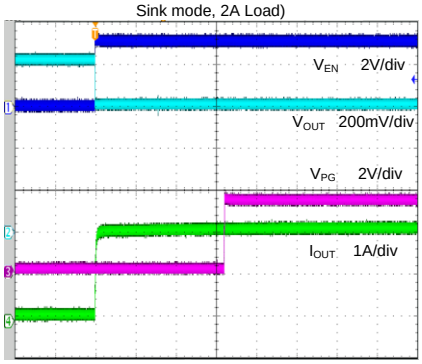
(V_{IN}=3.3V, V_{LDOIN}=1.2V, V_{REFIN}=0.6V, Source mode, 1A Load)



Time(4μs/div)

Startup From Enable

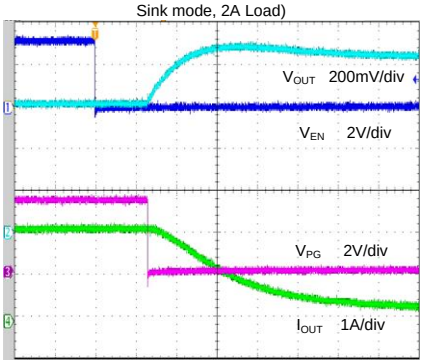
(V_{IN}=3.3V, V_{LDOIN}=1.2V, V_{REFIN}=0.6V, Sink mode, 2A Load)



Time(800μs/div)

Shutdown From Enable

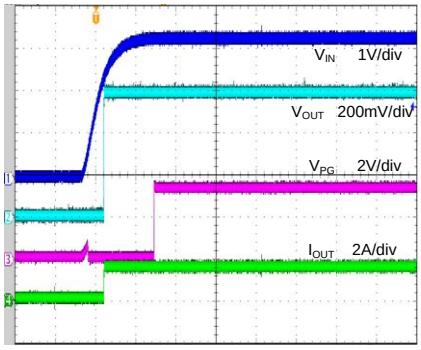
(V_{IN}=3.3V, V_{LDOIN}=1.2V, V_{REFIN}=0.6V, Sink mode, 2A Load)



Time(4μs/div)

Startup From VIN

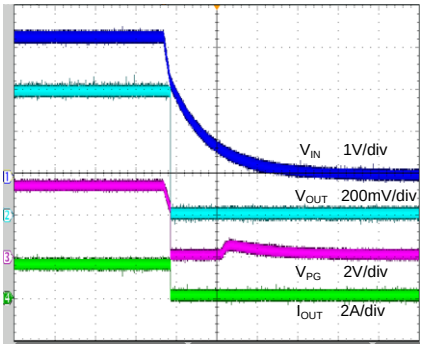
(V_{IN}=3.3V, V_{LDOIN}=1.2V, V_{REFIN}=0.6V, 2A Load)



Time(2ms/div)

Shutdown From VIN

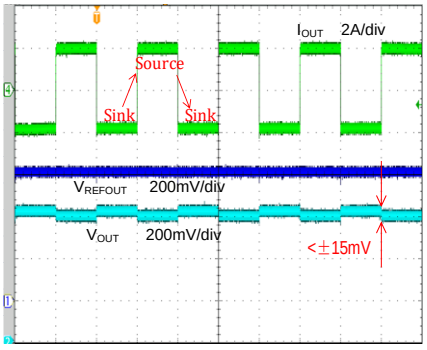
(V_{IN}=3.3V, V_{LDOIN}=1.2V, V_{REFIN}=0.6V, 2A Load)



Time(4μs/div)

Load Transient

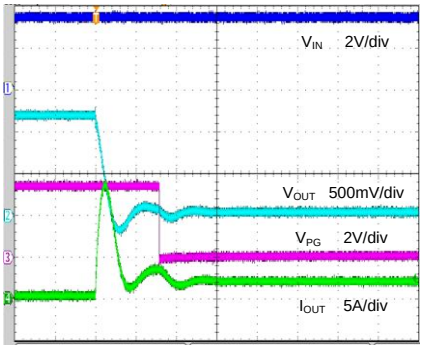
(V_{IN}=3.3V, V_{LDOIN}=1.2V, V_{REFIN}=0.6V, ±2A Load transient)



Time(10ms/div)

Short Circuit Response

(V_{IN}=3.3V, V_{LDOIN}=1.2V, V_{REFIN}=0.6V)



Time(10μs/div)

Application Information

The SY20775DBD is a sink and source tracking termination regulator specifically designed for low input voltage, low-cost, and low external component count systems with limited space.

The device integrates a high-performance, low-dropout (LDO) linear regulator capable of sourcing and sinking current. The LDO regulator employs a fast feedback loop so that small ceramic capacitors can support the fast load transient response. To achieve tight regulation with the minimum effect of trace resistance, connect the remote sensing terminal, VOSNS, at the load using a separate trace.

Reference Output Function

When configured for DDR termination applications, REFOUT generates the DDR VTT reference voltage for DDR memory applications. The device is capable of supporting both a sourcing and sinking load of 10mA. REFOUT becomes active when REFIN voltage rises above 0.390V, and V_{IN} is above the UVLO threshold. When REFOUT is less than 0.375V, the output is disabled and discharges to GND through an internal 10-kΩ resistor. REFOUT is independent of the EN pin state.

EN Control Function

When EN is driven high, the VO regulator begins normal operation. When EN is driven low, the VO regulator discharges to GND through an internal 18Ω resistor. REFOUT remains on when the EN input is low. Ensure that the EN pin voltage remains lower than or equal to V_{VIN} at all times.

Power Good Function

The SY20775DBD device provides an open-drain PGOOD output that goes to high impedance when the VO output is within ±20% of REFOUT. PGOOD is driven low within 10μs after the output voltage goes outside of the power good window. During the initial VO start-up, PGOOD is held low and released within 2ms after the VO enters the power good window. Because PGOOD is an open-drain output, a pull-up resistor between 1 kΩ and 100 kΩ is required, placed between PGOOD and a stable active supply voltage rail.

Current Limit Protection

The LDO has a constant over-current limit (OCL). The OCL level is reduced to one-half when the output voltage is not within the power good window. This reduction is a non-latch protection and the part resumes normal operation after the over-current condition disappears.

UVLO Protection

An under-voltage lockout (UVLO) protection is used in this device to ensure reliable operation. When the VIN voltage is lower than the UVLO threshold voltage, the VO and REFOUT regulators are turned off. Normal operation resumes when the voltage goes above the threshold. A 50 mV hysteresis is used to minimize the impact of noise that might be present in the system.

Thermal Shutdown Protection

The SY20775DBD monitors junction temperature. If the device junction temperature exceeds the threshold value of 150°C (typ.), the VO and REFOUT regulators are turned off, and the outputs are discharged by the internal discharge resistors. This shutdown is a non-latch protection.

Supply Filter Capacitor

Add a decoupling ceramic capacitor, with a value between 1μF and 4.7μF, placed close to the VIN bias supply (2.5V rail or 3.3V rail).

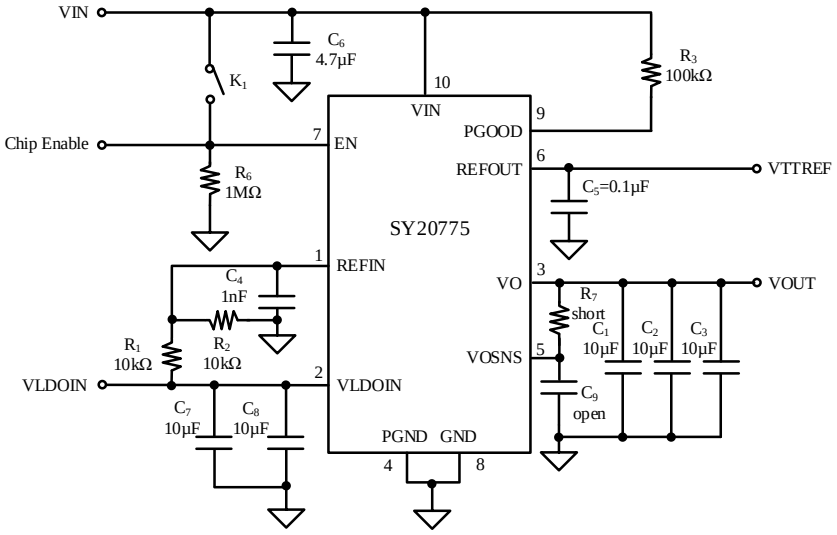
VLDOIN Input Capacitor

Use a 10μF (or greater) ceramic capacitor connected to the VLDOIN supply to support fast transient response. This rail is exposed to high current transients. Provide more input capacitance as more output capacitance is used at the VO pin. In general, use one-half of the C_{OUT} value for input.

Output Filter Capacitor

For stable operation, the total capacitance of the VO output pin must be greater than 20μF. For most applications using three, 10μF ceramic capacitors in parallel are recommended. This effectively reduces the equivalent series resistance (ESR) and equivalent series inductance (ESL). If the resulting ESR is greater than 2mΩ, insert an RC filter between the output and the VOSNS input to achieve loop stability. The RC filter time constant should be equal to or slightly less than the time constant of the output capacitor and its ESR.

Application Schematic



BOM List

Reference Designator	Description	Part Number	Manufacturer
C_1, C_2, C_3 , C_7, C_8	10µF/6.3V, 0603	GRM188R60J106KE47D+A01	Murata
C_4	1nF/50V, 0603	GCG1885G1H102GA01#	Murata
C_5	0.1µF/50V, 0603	GRM188R71H104KA93D	Murata
C_6	4.7µF/16V, 0603	GRM185R61C475KE11D+A01	Murata
C_9			
R_1, R_2	10kΩ, 0603	RC0603FR-0710KL	YAGEO
R_3	100kΩ, 0603	RC0603FR-07100KL	YAGEO
R_6	1MΩ, 0603	RC0603FR-071ML	YAGEO
R_7	R_7 Short circuit		

PCB Layout Guide

For best performance, the following guidelines must be followed:

1. Place the input capacitors as close to VDLOIN pin as possible with a short and wide connection.
2. Place the output capacitor as close to the VO pin as possible with a short and wide connection. Place a ceramic capacitor with a value of at least 10μF close to the VO pin if the rest of the output capacitors need to be placed on the load side.
3. Connect the VOSNS pin to the positive node of output capacitors as a separate trace. In a DDR VTT application, connect the VO sense trace to the DIMM side to ensure the VTT voltage accuracy at the DIMM side matches the specifications.
4. Consider adding a low-pass filter on the VOSNS signal if the VO sense trace is long.
5. Connect the GND pin and PGND pin to the thermal pad directly.
6. SY20775DBD uses its thermal pad to dissipate heat. Place numerous ground vias on the thermal pad to effectively remove heat from the package. Use a copper ground plane to connect and distribute heat, particularly on the surface layer.

   Maximize the copper area connected to GND on the top layer to improve heat dissipation.

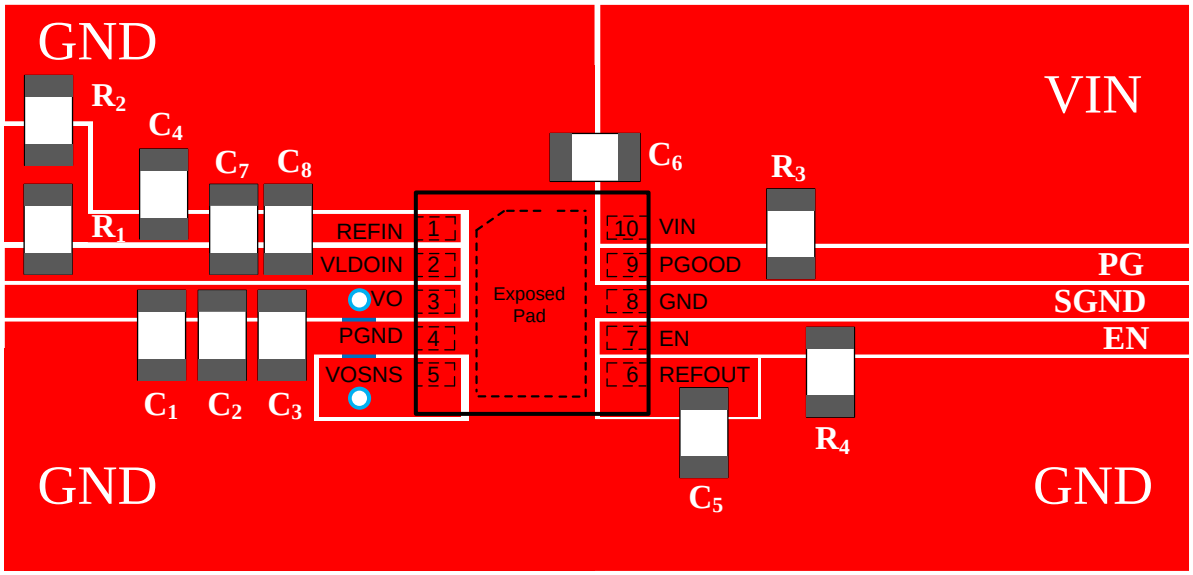
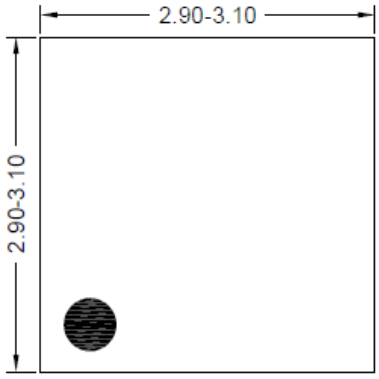
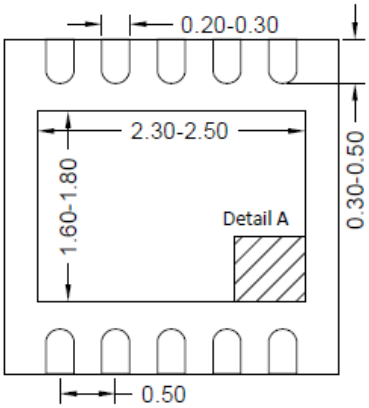


Figure 3. SY20775DBD PCB Layout Suggestion

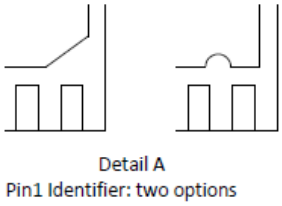
DFN3×3-10 Package Outline

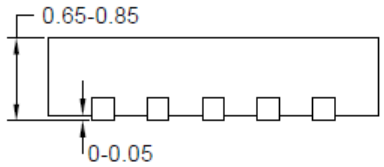


Top View

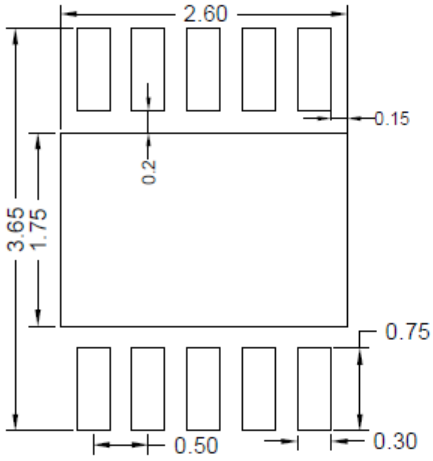


Bottom View





Side View

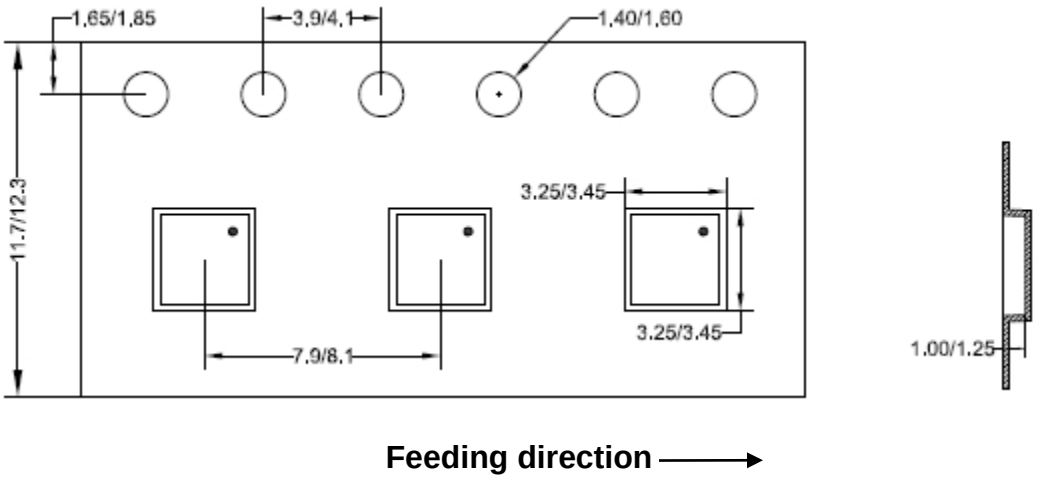


Recommended PCB Layout

Note: All dimensions are in millimeters and exclude mold flash and metal burr.

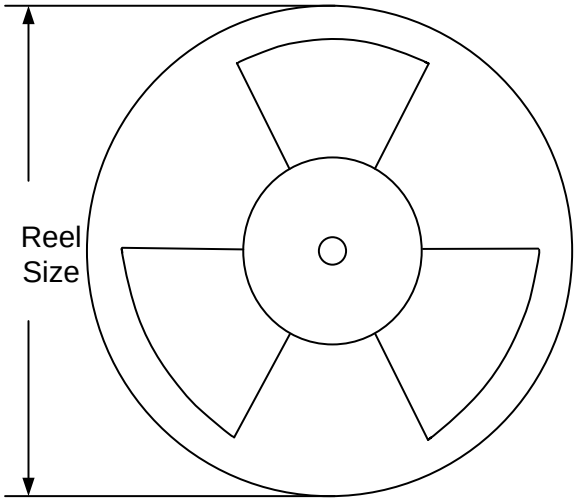
Taping & Reel Specification

1. DFN3×3-10 Taping Orientation



Feeding direction ⟶

2. Carrier Tape & Reel Specification for Packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN3×3	12	8	13"	400	400	5000

3. Others: NA

Revision History

The revision history provided is for informational purposes only and is believed to be accurate; however, it is not warranted. Please reference the latest revision.

Date	Revision	Change
Sep. 26, 2023	Revision 1.0	Language improvements for clarity.
Dec.09, 2020	Revision 0.9	Initial Release

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