SY28902B

IEEE 802.3af/at-compliant PD Interface Controller

General Description

The SY28902B is a power device (PD) controller with all the features needed to implement the IEEE802.3at/at protocol. It employs a high-power classification scheme, delivering 38.7W, 52.7W, 70W or 90W of power at the PD RJ45 connector. The SY28902B is fully compatible with IEEE 802.3af/at.

An internal charge-pump is used for enabling the use of external low $R_{DS(ON)}$ N-channel MOSFETs and increase the end-to-end power transmission efficiency. The SY28902B includes an integrated signature resistor, under-voltage lockout, a power good output and thermal protection. The start-up inrush current can be adjusted using an external capacitor. Auxiliary power override is supported for voltages higher than 9V applied to the AUX pin.

802.3at, 802.3af and up to 90W power levels are all supported by configuring external components.

The SY28902B is available in a compact DFN3×3-10 package.

Features

- IEEE 802.3af/at Powered Device (PD) Controller
- Supports Up to 90W PDs
- Supports All of the Following Standards:
  - High Power Mode: 38.7W, 52.7W, 70W and 90W
  - IEEE 802.3at 25.5W Compliant
  - IEEE 802.3af up to 13W Compliant
- 100V Robust Surge Protection (Abs. Max.)
- Integrated Signature Resistor
- Thermal Shutdown Protection
- External Hot Swap N-Channel MOSFET for Lowest Power Dissipation and Highest System Efficiency
- Configurable Aux Power Support as Low as 9V
- –40℃ to 125℃Junction Temperature Range

Applications

- Security Cameras
- Base Stations
- IEEE 802.3bt Compliant Devices
- Video and VoIP Telephones

Typical Application

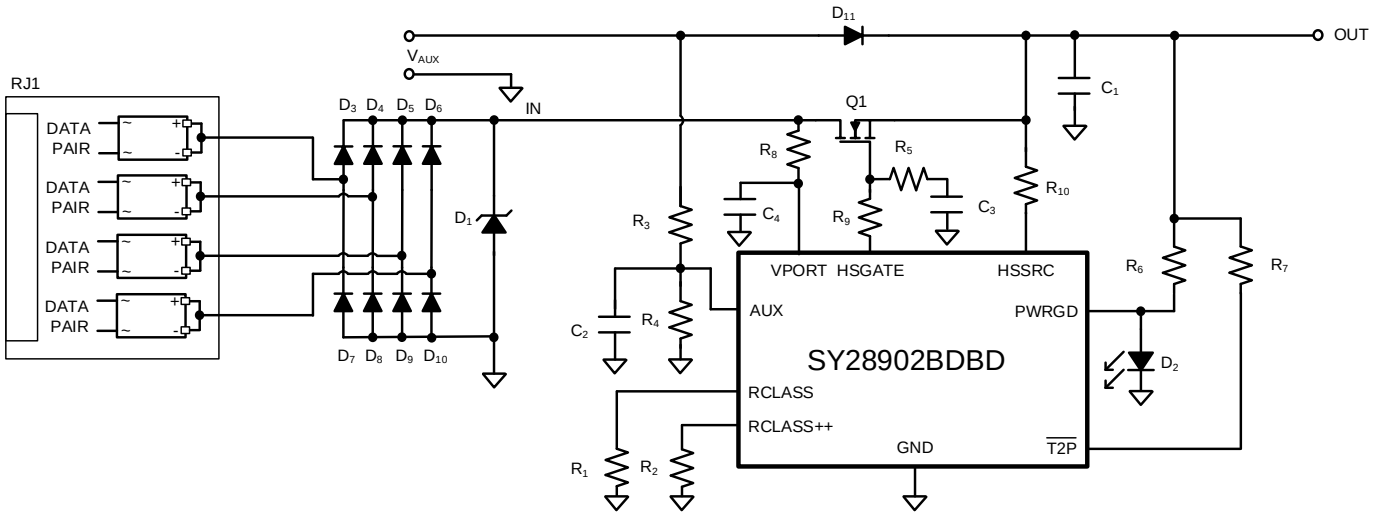


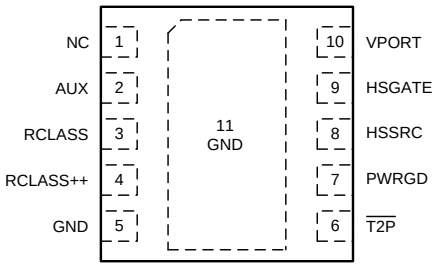
Figure 1. Schematic Diagram

Ordering Information

Ordering Part Number	Package Type	Top Mark
SY28902BDBD	DFN3×3-10 RoHS Compliant and Halogen Free	**EEMxyz**

x=year code, y=week code, z= lot number code

Pinout (top view)



Pin Name	NO.	TYPE	Pin Description
GND	5, 11	-	Device ground. The exposed pad must be electrically and thermally connected to pin5 and PCB GND.
AUX	2	I	Auxiliary sense pin. A resistive divider from the auxiliary power input to AUX sets the voltage at which the auxiliary supply takes over. In auxiliary power operation, HSGATE pulls down, the signature resistor disconnects, classification is disabled, and the PWRGD pin is high impedance and $\overline{T2P}$ indicates max available power. The AUX pin sinks I_{AUXH} when below its threshold voltage of V_{AUXT} to provide hysteresis. Connect to GND when not used.
RCLASS	3	O	Configurable PoE classification resistor.
RCLASS++	4	O	Configurable PoE classification resistor.
$\overline{T2P}$	6	O	PSE type indicator, open-drain output.
PWRGD	7	O	Power good indicator. Open-drain output. Pulls to GND during V_{CLASS} and inrush.
HSSRC	8	I	External hot-swap MOSFET source. Connect to the source of the external MOSFET.
HSGATE	9	O	External hot-swap MOSFET gate control, output. Connect to the gate of the external MOSFET.
VPORT	10	I	PD interface upper power rail and external hot-swap MOSFET drain connection.
NC	1	-	No electrical connection internally. May connect to any potential.

Block Diagram

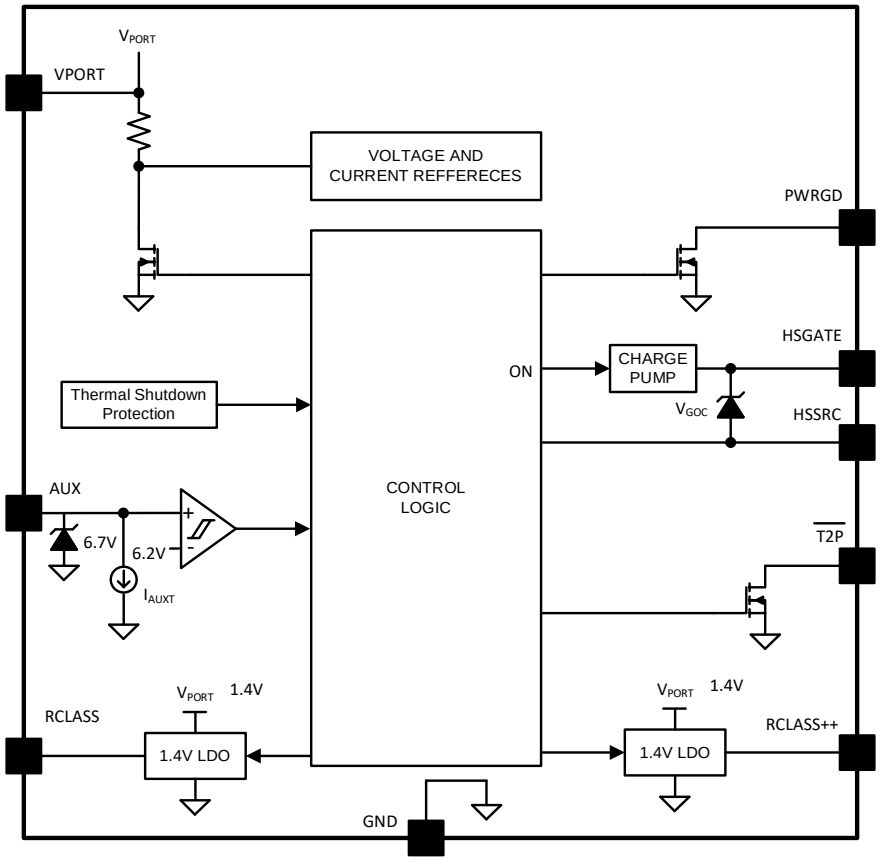


Figure 2. Block Diagram

Absolute Maximum Ratings

Parameter (Note1) (Note4)	Min	Max	Unit
VPORT, HSSRC, HSGATE, $\overline{T2P}$, PWRGD	–0.3	100	V
RCLASS, RCLASS++	-0.3	6 (and ≤ VPORT)	
HSGATE Current	-20	20	mA
AUX Current	-1.4	1.4	
$\overline{T2P}$, PWRGD Current		5	
Junction Temperature, Operating	-40	125	°C
Lead Temperature (Soldering, 10sec.)		300	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note2)	Typ	Unit
θ_{JA} Junction-to-ambient Thermal Resistance	60.5	°C/W
θ_{JC} Junction-to-case Thermal Resistance	31	
P_D Power Dissipation T_A=25°C	1.65	W

Recommended Operating Conditions

Parameter (Note5)	Min	Max	Unit
VPORT, HSSRC	0	60	V
RCLASS, RCLASS++	0	5 (and ≤ VPORT)	
Ambient Temperature	-40	125	°C

Electrical Characteristics

(The specification in the following table applies over the –40°C≤ T_J≤+125°C. Typical values are for T_A = 25°C, unless otherwise noted.). (Note4)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VPORT Operating Input Voltage		At VPORT Pin			60	V
VPORT Signature Range	V_{SIG}	At VPORT Pin	1.5		10	V
VPORT Classification Range	V_{CLASS}	At VPORT Pin	12.5		21	V
VPORT Mark Range	V_{MARK}	At VPORT Pin, Preceded by V_{CLASS}	5.6		10	V
VPORT Aux Mode Range		At VPORT Pin, AUX > V_{AUXT}	8		60	V
Signature/Class Hysteresis Window			1.0			V
Reset Threshold	V_{RESET}	At VPORT Pin, Preceded by V_{CLASS}	2.6		5.6	V
Hot Swap Turn-On Voltage	V_{HSON}			35	37	V
Hot Swap Turn-Off Voltage	V_{HSOFF}		30	31		V
Hot Swap On/Off Hysteresis Window			3			V
Supply Current						
Supply Current		V_{VPORT}=V_{HSSRC}=57V			1	mA
Supply Current During Classification		V_{VPORT} = 17.5 V, RCLASS and RCLASS++ Open	0.1	0.2	0.5	mA
Supply Current During Mark Event		V_{VPORT}=V_{MARK} After 1st Classification Event	0.5		1.8	mA
Detection and Classification Signature						
Detection Signature Resistance		V_{SIG} (Note 3)	23.7	24.4	25.2	kΩ
Resistance During Mark Event		V_{MARK} (Note 3)	5.8	8.3	11	kΩ
RCLASS/RCLASS++ Operating Voltage		–10mA ≥ I_{RCLASS} ≥ –36mA, V_{CLASS}	1.32	1.40	1.43	V
Classification Signature Stability Time		V_{VPORT} Step to 17.5V, 34.8Ω from RCLASS or RCLASS++ to GND			2	ms
Analog/Digital Interface						
AUX Threshold	V_{AUXT}		6.0	6.2	6.4	V
AUX Hysteresis	$V_{AUX,HYS}$			0.4		V
AUX Pin Hysteresis Current	I_{AUXT}	V_{AUX} = 6.1V	0.8	2.1	4	µA
$\overline{T2P}$ Output Low		1mA Load			0.8	V
PWRGD Output Low		1mA Load			0.8	V
PWRGD Leakage Current		V_{PWRGD} = 60V			5	µA
$\overline{T2P}$ Leakage Current		$\overline{T2P}$ = 60V			5	µA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Hot Swap Control						
HSGATE Pull-up Current	I_{GPU}	V_{HSGATE} - V_{HSSRC} = 5V (Note 7)	-27	-22	-18	μA
HSGATE Open Circuit Voltage	V_{GOC}	-10μA load, with Respect to HSSRC	10		17	V
HSGATE Pull-Down Current		V_{HSGATE} - V_{HSSRC} = 5V	200			μA
Timing						
$\overline{T2P}$ Frequency	f_{T2P}	V_{AUX} > V_{AUXT}, and RCLASS++ has resistor to GND	690	840	990	Hz
$\overline{T2P}$ Duty Cycle in PoE Operation (Note 6)		After 3-Event Classification		50		%
$\overline{T2P}$ Duty Cycle in Auxiliary Supply Operation (Note 6)		V_{AUX} > V_{AUXT}, and RCLASS++ has resistor to GND at T_A = 25°C.		50		%

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on the Silergy EVB test board.

Note 3: Signature resistance specifications do not include resistance added by the external diode bridge, which can add as much as 1.1kΩ to the port resistance.

Note 4: All voltages with respect to GND unless otherwise noted. Positive currents flow into pins; negative currents flow out of pins unless otherwise noted.

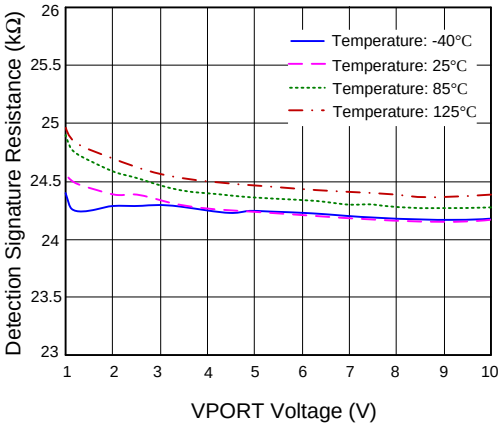
Note 5: This IC includes over-temperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 150°C when over-temperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 6: Specified as the percentage of the period which $\overline{T2P}$ is low impedance with respect to the GND.

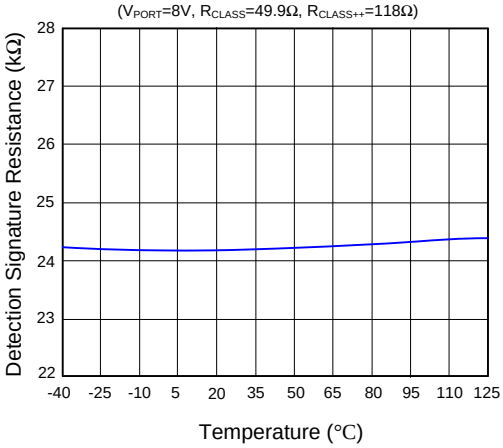
Note 7: I_{GPU} available in PoE-powered operation. That is, available after V_{VPORT} > V_{HSON} and V_{AUX} < V_{AUXT}, over the range where V_{VPORT} is between V_{HSOFF} and 60V.

Typical Performance Characteristics

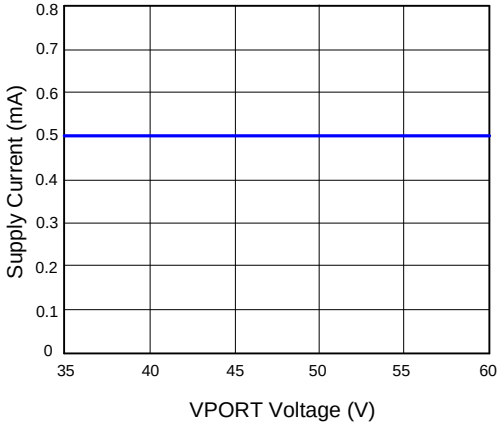
Detection Signature Resistance vs. VPORT Voltage



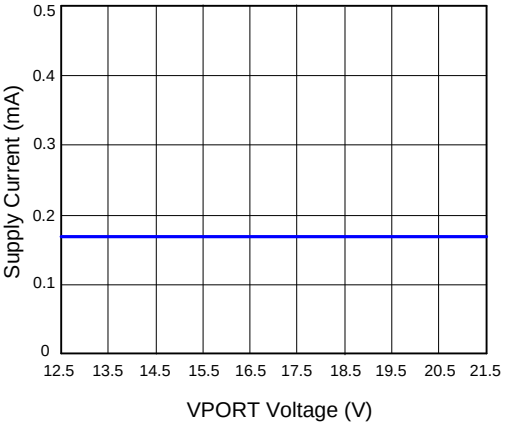
Detection Signature Resistance vs. Temperature
(V_{PORT}=8V, R_{CLASS}=49.9Ω, $R_{CLASS++}$=118Ω)



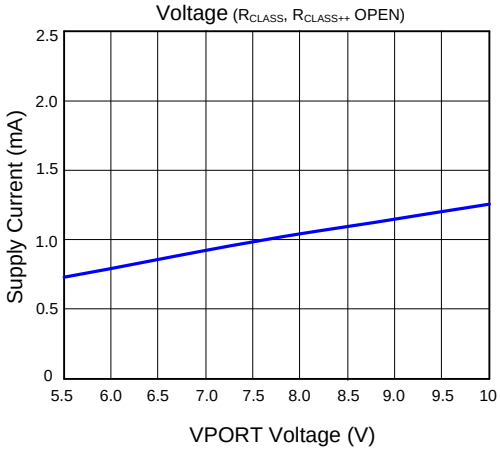
Supply Current during PWRFET Turn on vs. VPORT Voltage (R_{CLASS}, $R_{CLASS++}$ OPEN)



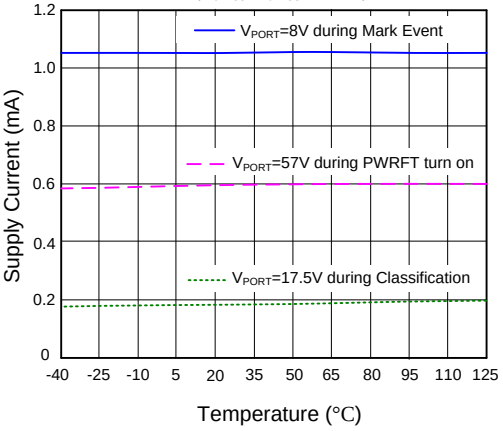
Supply Current during Classification vs. VPORT Voltage (R_{CLASS}, $R_{CLASS++}$ OPEN)



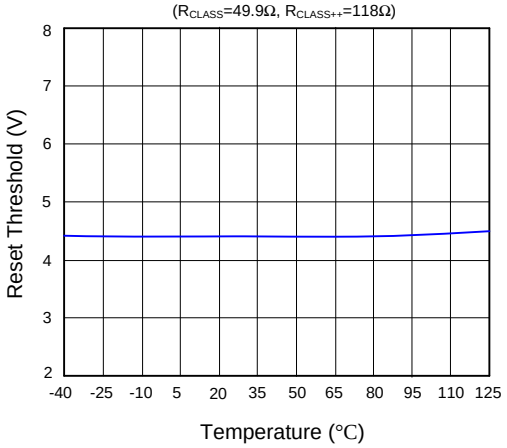
Supply Current during Mark Event vs. VPORT Voltage (R_{CLASS}, $R_{CLASS++}$ OPEN)



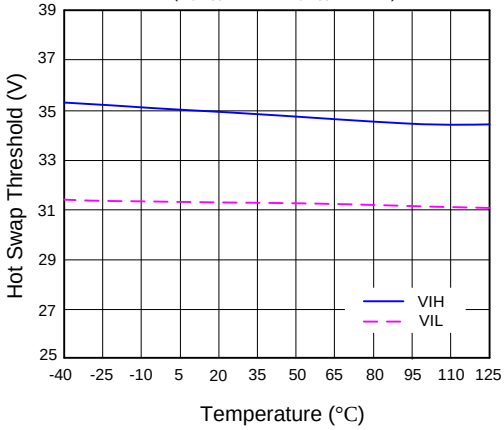
Supply Current vs. Temperature
(R_{CLASS}, $R_{CLASS++}$ OPEN)



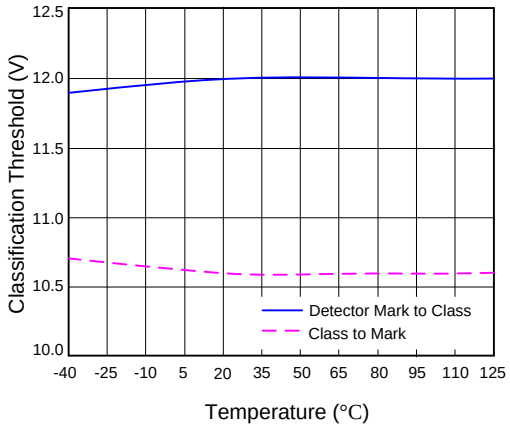
Reset Threshold vs. Temperature
(R_{CLASS}=49.9Ω, $R_{CLASS++}$=118Ω)



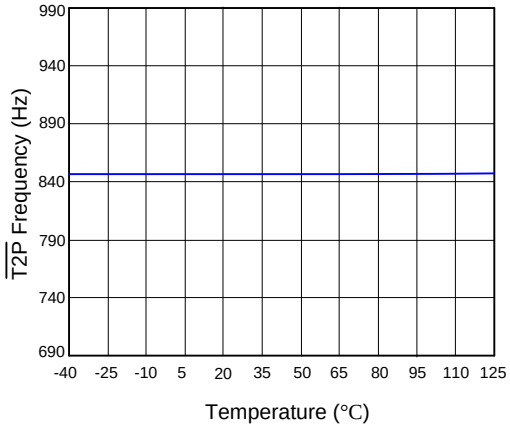
Hot Swap Threshold vs. Temperature
(R_{CLASS}=49.9Ω, $R_{CLASS++}$=118Ω)



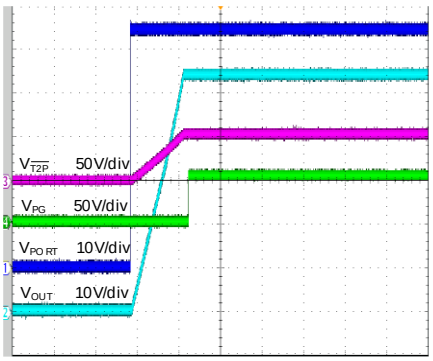
Classification Threshold vs. Temperature
(R_{CLASS}=49.9Ω, $R_{CLASS++}$=118Ω)



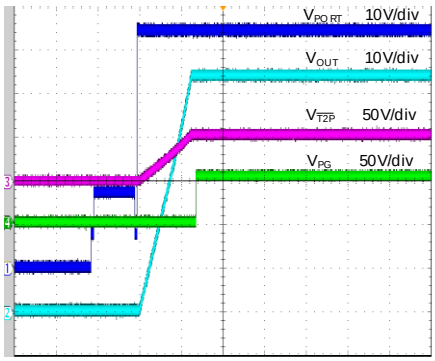
$\overline{T2P}$ Frequency vs. Temperature



Event 0 Operation Test
(V_{PORT}=0→54V, R_{CLASS}=49.9Ω, $R_{CLASS++}$=118Ω)

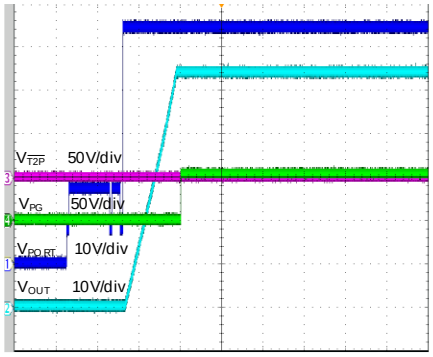


Event 1 Operation Test
(V_{PORT}=0→8V→17.5V→54V, R_{CLASS}=49.9Ω, $R_{CLASS++}$=118Ω)



Event 2 Operation Test

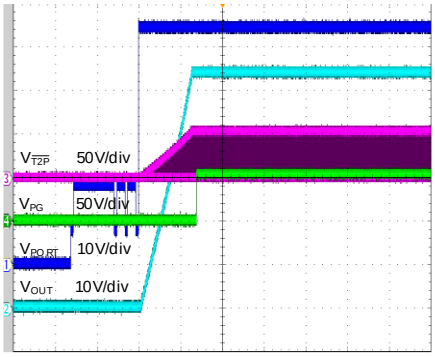
(V_{PORT}=0→8V→17.5V→54V, R_{CLASS}=49.9Ω $R_{CLASS++}$=118Ω)



Time (100ms/div)

Event 3 Operation Test

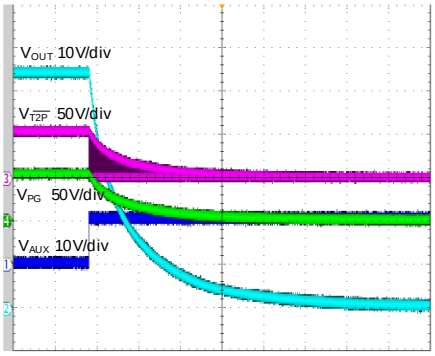
(V_{PORT}=0→8V→17.5V→54V, R_{CLASS}=49.9Ω $R_{CLASS++}$=118Ω)



Time (100ms/div)

AUX ON

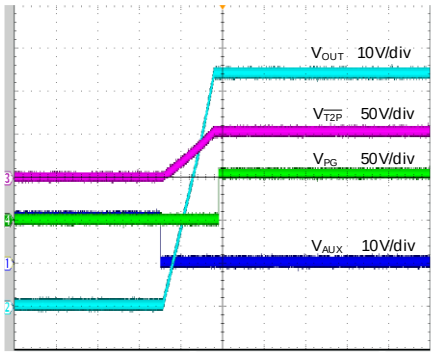
(V_{PORT}=54V, V_{AUX}=0→10V, R_{CLASS}=49.9Ω $R_{CLASS++}$=118Ω)



Time (100ms/div)

AUX OFF

(V_{PORT}=54V, V_{AUX}=10→0V, R_{CLASS}=49.9Ω $R_{CLASS++}$=118Ω)



Time (100ms/div)

Application Information

Overview

The IEEE 802.3af/at specification defines a process for safely powering a PD over a cable and removing power if a PD is disconnected. The process consist of three operational states: detection, classification, and operation.

The SY28902B is designed to support higher power applications while maintaining backward compatibility with existing PSE systems. To eliminate expensive heat sinks, the SY28902B uses an external low $R_{DS(ON)}$ N-channel hot-swap MOSFET to increase end-to-end power transmission efficiency.

Modes of Operation

Detection Signature

When a voltage in the range of 2.7V to 10.1V is applied to the PI, an incremental resistance of 25kΩ signals the Power Supply Equipment (PSE) that the PD can accept power. Figure 3 shows the detection voltages of PSE. The PSE calculates the signature resistance using a ΔV/ΔI measurement technique.

The SY28902B integrates a temperature-compensated, precision 24.4k signature resistor between the VPORT and GND pins. The PSE requests power to be applied if a valid PD is recognized. Typically, the SY28902B signature resistor is smaller than 25k to compensate for the additional series resistance on the line.

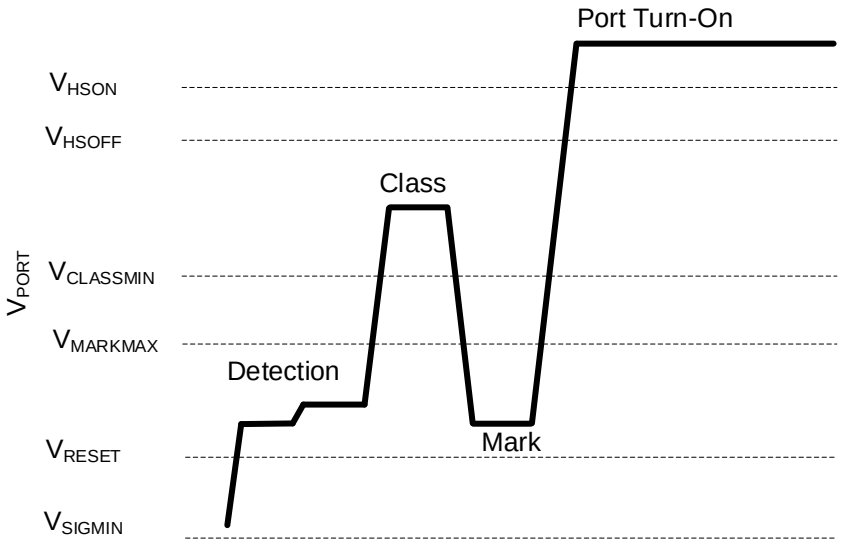


Figure 3. Type 1 PSE, 1-Event Class Sequence

Classification Signature and Mark

The SY28902B may optionally provide a classification signature to the PSE, indicating the maximum power it will draw during operation. The IEEE specification defines this signature as a constant current draw when the PSE port voltage is in the V_{CLASS} range (between 14.5V and 20.5V). If the PSE applies a classification probe voltage, the PSE returns the PD voltage to the mark voltage range before applying another classification probe voltage or powering up the PD.

An example of 1-Event classification is shown in Figure 3. In a 2-Event classification, a PSE probes for power classification twice, as shown in Figure 4. The SY28902B recognizes this and pulls the T2P pin down to signal to the load that Type 2 power is available. If a SY28902B senses a PSE of high-power mode, it will alternate between pulling T2P down and floating T2P at a rate of f_{T2P}.

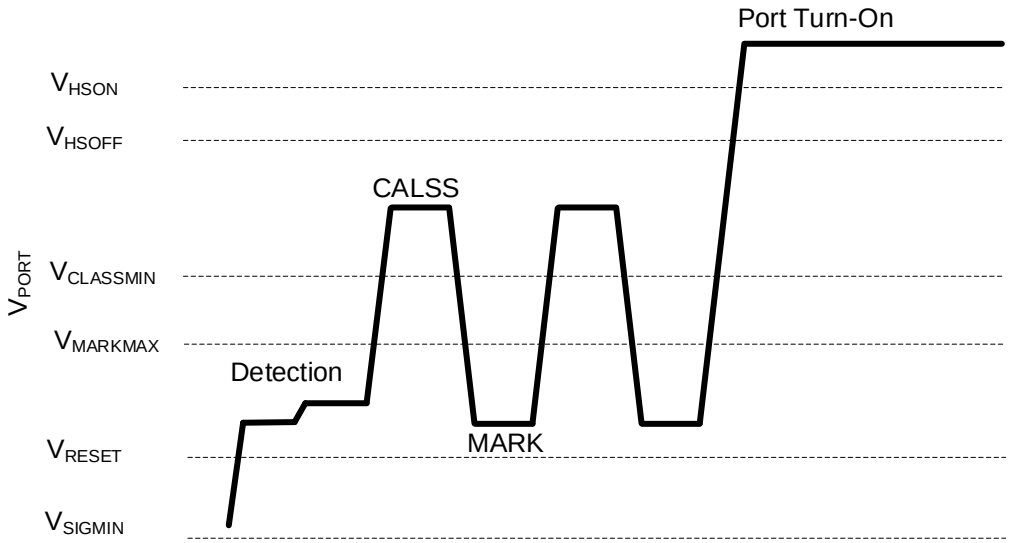


Figure 4. Type 2 PSE, 2-Event Class Sequence

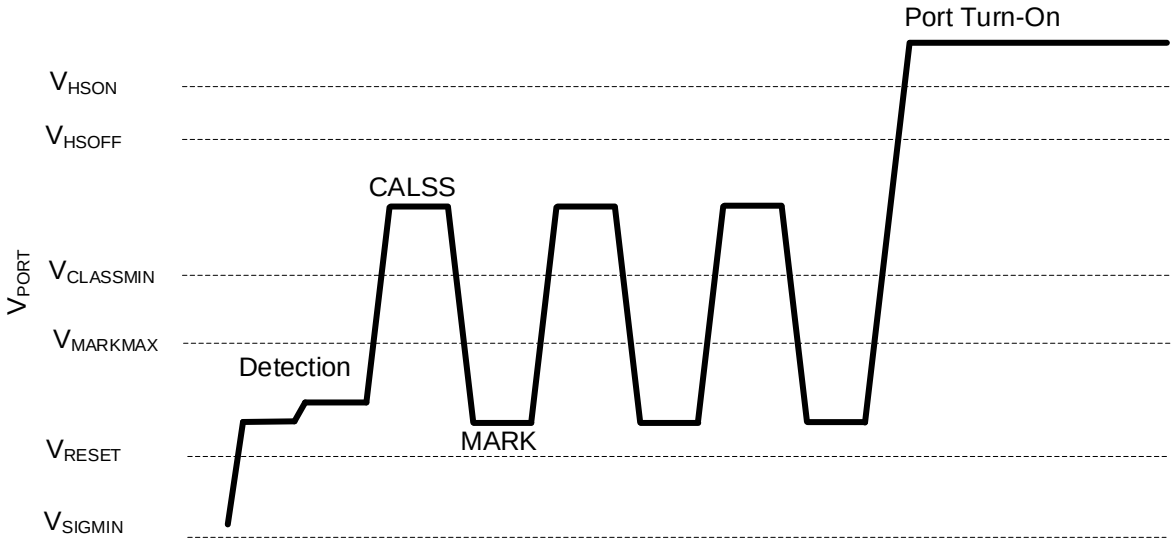


Figure 5. Type 3 or 4 PSE, 3-Event Class Sequence

Table 1. Classification Codes, Power Levels, and Resistor Selection

PD REQUESTED CLASS	PD POWER AVAILABLE	PD TYPES	NOMINAL CLASS CURRENT	RESISTOR (1%)	
				R_{CLS}	R_{CLS++}
0	13W	Type 1	2.5mA	1.00kΩ	Open
1	3.84W	Type 1	10.5mA	140Ω	Open
2	6.49W	Type 1	18.5mA	76.8Ω	Open
3	13W	Type 1	28mA	49.9Ω	Open
4	25.5W	Type 2	40mA	34.8Ω	Open
High-power Mode (38.7W or 5)	32.7W	High-power Mode	40mA/2.5mA	1.00kΩ	37.4Ω
High-power Mode (52.7W or 6)	52.7W	High-power Mode	40mA/10.5mA	140Ω	46.4Ω
High-power Mode (70W or 7)	70W	High-power Mode	40mA/18.5mA	76.8Ω	64.9Ω
High-power Mode (90W or 8)	90W	High-power Mode	40mA/28mA	49.9Ω	118Ω

High-Power Mode

The SY28902B allows higher power allocation while maintaining backward compatibility with existing PSE systems by extending the classification signaling of IEEE 802.3.

The PSEs supporting high-power modes present up to three classification events. As shown in Figure 5, a PSE of high-power mode probes for power classification three times in 3-event classification. The SY28902B recognizes this and alternates between pulling $\overline{T2P}$ down and floating $\overline{T2P}$ at a rate of f_{T2P} to signal the load that higher power is available.

Signature Corrupt During Mark Event

In this case, the SY28902B presents a resistance value <11kΩ to the port according to the requirements of the IEEE 802.3 specification during the mark event.

Demotion and Denial in High-Power Mode

IEEE 802.3 PSEs may demote PDs to a lower power state when the PD Requested Power exceeds the PSE available power. When two or fewer class/mark events are received, PD allocated power is at or below 25.5W, and the PSEs of high-power mode are considered equivalent to IEEE 802.3 PSEs.

Table 2. PSE Allocated Power

PD REQUESTED CLASS	NUMBER OF PSE CLASS/MARK EVENTS		
	1	2	3
0	13W		
1	3.84W		
2	6.49W		
3	13W		
4	**13W**	25.5W	
High-power Mode (38.7W or 5)	**13W**	**25.5W**	38.7W
High-power Mode (52.7W or 6)	**13W**	**25.5W**	52.7W
High-power Mode (70W or 7)	**13W**	**25.5W**	70W
High-power Mode (90W or 8)	**13W**	**25.5W**	90W

Note: Bold indicates the PD has been demoted.

Selection of Classification Resistors (R_{CLS} and R_{CLS++})

Select the value R_{CLS} and R_{CLS++} resistors to configure the classification currents from Table 1 to the PD power classification. Connect each 1% resistor between the R_{CLASS}, $R_{CLASS++}$ pins, and GND.

Detection Signature Corrupt During Mark Event

The SY28902B presents <11kΩ to the port according to the requirements of the IEEE 802.3 specification during the mark event.

Inrush and Power On

The PSE turns on the power to the PD once the PSE detects and classifies the PD. The SY28902B begins to source I_{GPU} out of the HSGATE pin when the port voltage rises above the V_{HSON} threshold. This current flows into an external capacitor, such as C_{GATE} shown in Figure 8, which causes the gate of the external MOSFET to rise. The external N-channel MOSFET acts as a source follower and causes the voltage ramp on the output bulk capacitor C_{OUT} to rise, thereby determining the inrush current (I_{INRUSH}). A typical design target for I_{INRUSH} is approximately 100mA. The value for C_{GATE} can be calculated using the following equation:

$$I_{INRUSH} = I_{GPU} \frac{C_{PORT}}{C_{GATE}}$$

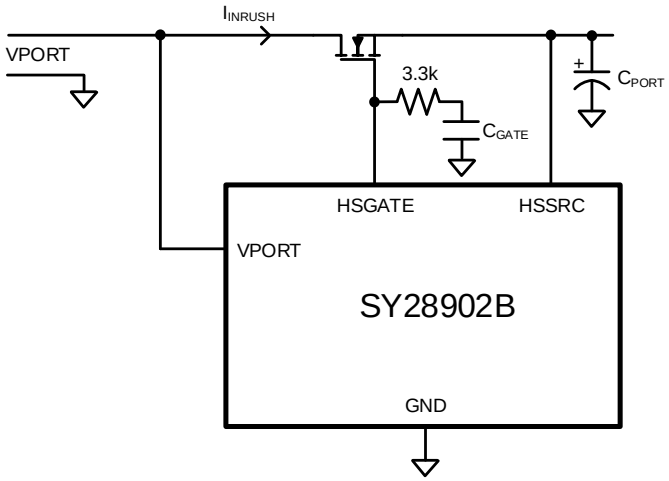


Figure 6. I_{INRUSH} Configuration

The SY28902 internal charge pump enables the use of N-channel MOSETs due to their lower cost and $R_{DS(ON)}$. Using a low $R_{DS(ON)}$ MOSFET maximizes power transmission efficiency, reduces power and heat dissipation, and simplifies thermal design.

Power Good Indicator

The PWRGD pin can be used to disable the downstream circuits until the external MOSFET is fully biased and inrush time is complete. The PWRGD pin remains low until HSGATE is charged to approximately 8V above HSSRC. The HSGATE pin remains high, and the PWRGD pin is in high-impedance until the port voltage falls below V_{HSOFF}.

Auxiliary Supply Override

The SY28902B enters auxiliary power supply override mode if the AUX pin is held above V_{AUXT}. In this mode of operation, the signature resistor disconnects, HSGATE pulls down, classification is turned off, the PWRGD pin is high-impedance, and the $\overline{T2P}$ pin indicates max available power.

The AUX pin allows for setting the auxiliary supply turn on and turn off voltage thresholds, V_{AUXON}, and V_{AUXOFF}, respectively. The auxiliary supply hysteresis voltage, V_{AUXHYS}, is generated with a current sink, I_{AUXH}, and is active only when the AUX pin voltage is less than V_{AUXT}. Use the following equations to set V_{AUXON} and V_{AUXOFF} via R1 and R2 in Figure 7. Note that an internal 6.7V Zener limits the voltage on the AUX pin.

A capacitor up to 1000pF may be placed between the AUX pin and GND to improve noise immunity. V_{AUXON} must be lower than V_{HSOFF}.

$$V_{AUXON} = \left(\frac{R_1}{R_2} + 1\right) V_{AUXT} + I_{AUXT} R_1$$

$$V_{AUXOFF} = V_{AUXON} - \left(\frac{R_1}{R_2} + 1\right) V_{AUX\_HY}$$

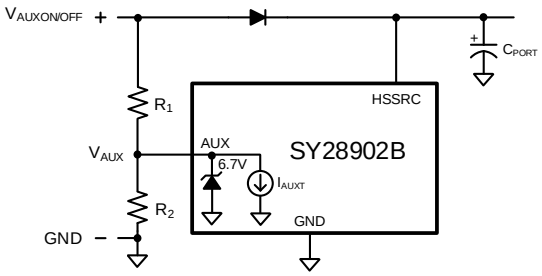


Figure 7. AUX Threshold and Hysteresis Calculation

AUX Zener Limit

If the AUX pin is driven above the internal Zener voltage threshold of 6.7V**,** the SY28902 will clamp the voltage to this level. For safe operation, the maximum current flowing into the AUX pin has to be lower than 1.4mA. Use a R_1 value higher than the resistance value calculated using the following equation:

$$R_1 \geq \frac{V_{AUXON(MAX)} - 6.7V}{1.4mA}$$

$\overline{T2P}$ Output

The $\overline{T2P}$ pin state is determined by the number of classification events, the RCLASS++ pin, and the AUX pin and also depends on the PSE allocated power. The SY28902 uses a 5-state encoding for the $\overline{T2P}$ output by changing the pin level and/or the duty cycle. Table 3 lists the $\overline{T2P}$ state based on the above input conditions:

Table 3. $\overline{T2P}$ Response to Determine PSE Allocated Power

AUX STATE	PD REQUESTED CLASS (RCLASS/ RCLASS++)	NUMBER OF CLASSIFICATION EVENTS	$\overline{T2P}$ WITH RESPECT TO GND	PSE ALLOCATED POWER
AUXILIARY	0-4	N/A	Low-Z	AUX Power
	5-8	N/A	50% Low-Z 50% HI-Z	AUX Power
PoE af/at	0-4	1	HI-Z	13W
		≥ 2	Low-Z	25.5W
High-power Mode	5-8	1	HI-Z	13W
		2	Low-Z	25.5W
		≥ 3	50% Low-Z 50% HI-Z	PD requested higher power

The AUX pin is the highest priority input. AUX is de-asserted to enter the PoE state and is asserted to enter the auxiliary power state. Based on PD requested class, the $\overline{T2P}$ pin indicates the highest available power in the auxiliary power state. The auxiliary power supply must be sized to provide at least the power required by the PD.

As shown in Table 1, the PD Requested Class is configured using the RCLASS and RCLASS++ pins. The RCLASS++ pin can be used to determine if the PD Class is 0-4 or high-power mode.

As shown in Table 2, the number of classification events determines the power allocated by the PSE.

Thermal Shutdown Protection

A PD must meet the IEEE 802.3 specification required to indefinitely withstand any applied voltage from 0V to 57V.

However, during the classification process, the power dissipation of the SY28902B may be as high as 1.5W. The SY28902B easily tolerates this during the maximum IEEE classification timing, but it can overheat if this condition persists for a long time. The SY28902B includes a thermal shutdown protection function to protect equipment under transient overload conditions. If the junction temperature exceeds the over-temperature threshold, the SY28902B pulls down HSGATE pin and disables classification.

External Interface and Component Selection

PoE Input Bridge

A PD needs to perform polarity correction of its input voltage. There are several options for bridge rectifiers: ideal diodes, silicon diodes, and Schottky diodes. When using Schottky or silicon diode bridges, the voltage at the VPORT pin will be reduced due to the forward voltage across the diodes. The SY28902 is designed to tolerate these voltage drops.

Silicon diode bridges perform poorly, are unbalanced from wiring pair to pair, and consume up to 4% of the available power. In addition, thermal runaways can cause significant, non-compliant current unbalance between pair sets. Although using Schottky diodes can help reduce power loss and offer lower forward voltages, Schottky bridges may not be suitable for high-temperature PD applications, due to the increase of leakage currents at high temperature and a dependance of the leakage with voltage, as this can lead to an invalid detection signature. The increased leakage currents can also back-feed through the unpowered branch and the unused bridge, violating the IEEE 802.3 specifications.

Auxiliary Input Diode Bridge

Some PDs require an auxiliary power source to receive AC or DC power. A diode bridge is typically required to handle the polarity correction and voltage rectification.

Input Capacitor

Add a 0.1μF capacitor between VPORT and GND to meet the input impedance requirement of IEEE 802.3 and appropriately bypass the SY28902B.

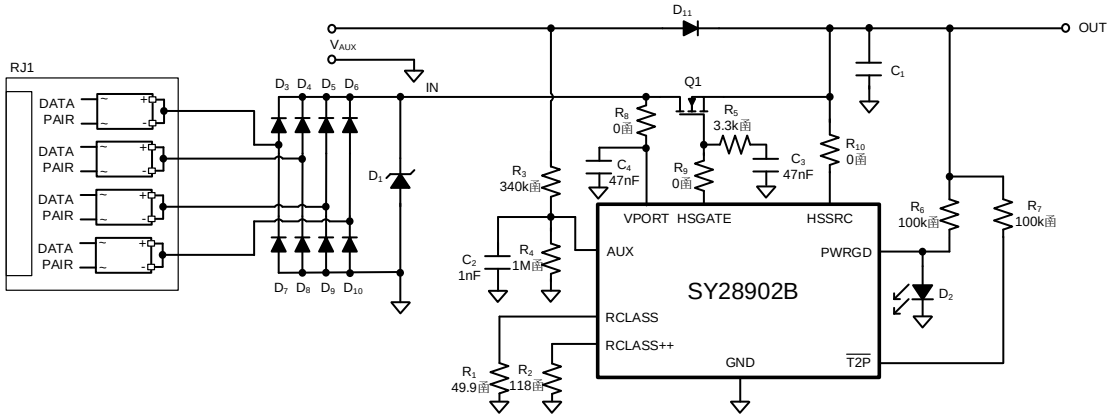
Transient Voltage Suppressor

The SY28902 is specified to withstand an absolute maximum input voltage of 100V, and it can tolerate brief over-voltage events due to Ethernet cable surges. To protect the SY28902 from an over-voltage event, a unidirectional transient voltage suppressor (TVS), such as an SMAJ60A, should be used between the VPORT and GND pins.

Exposed Pad

The SY28902B DFN package has an exposed pad internally electrically connected to the GND. The exposed pad may only be connected to GND on the printed circuit board.

Application Schematic



BOM List

Designator	Description	Part Number	Manufacturer
C_1	/	/	/
C_2	1nF/50V, 0603	GRM1885C1H102GA01D	Murata
C_3	47nF/100V, 0805	GRM21BR72A4473KA01L	Murata
C_4	47nF/100V, 0805	GRM21BR72A4473KA01L	Murata
R_1	49.9Ω, 0603	RC0603FR-0749R9L	YAGEO
R_2	118Ω, 0603	RC0603FR-07118RL	YAGEO
R_3	340kΩ, 0603	RC0603FR-07340KL	YAGEO
R_4	1MΩ, 0603	RC0603FR-071ML	YAGEO
R_5	3.3kΩ, 0603	RC0603FR-073K3L	YAGEO
R_6	100kΩ, 0603	RC0603FR-07100KL	YAGEO
R_7	100kΩ, 0603	RC0603FR-07100KL	YAGEO
R_8, R_9,R_{10}	0	/	/
D_1	TVS/60V, SMA	SMAJ60A	Littelfuse
D_2	LED	/	/
D_3-D_{11}	Schottky/100V	SS3100	TOSHIBA
RJ1	RJ45	RJ45-B-1*1	BOOMELE
Q_1	NMOS/100V	FDMS86150	Fairchild

Layout Considerations

Place resistors R_{CLS} and R_{CLS++} close to the SY28902B to avoid excessive parasitic capacitance on the RCLASS and RCLASS++ pins.

It is strictly required for maximum protection to place the 0.1μF input capacitor, C_{PD}, and transient voltage suppressor as close to the SY28902B as possible.

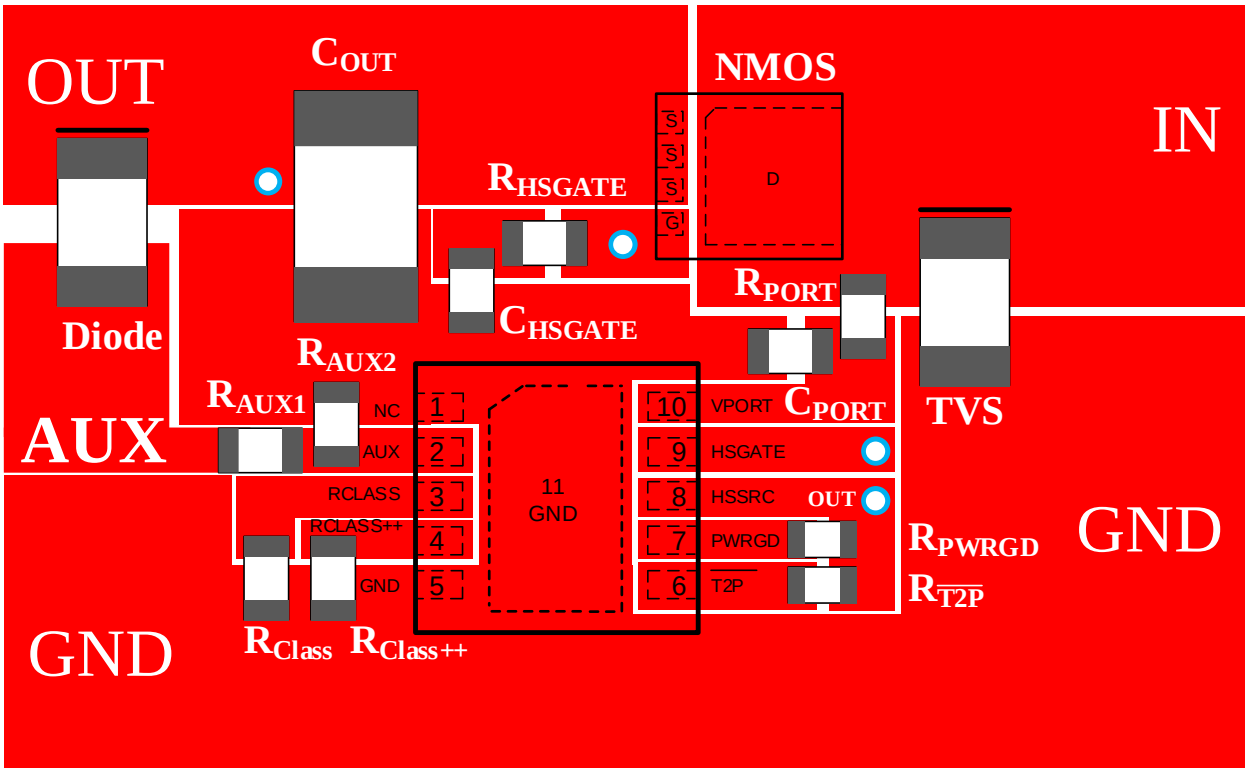
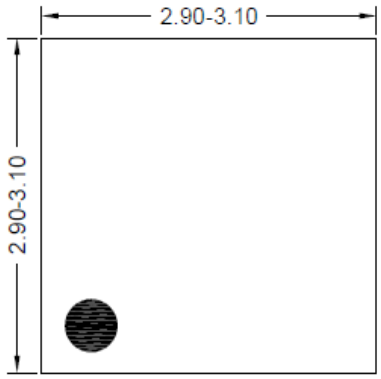
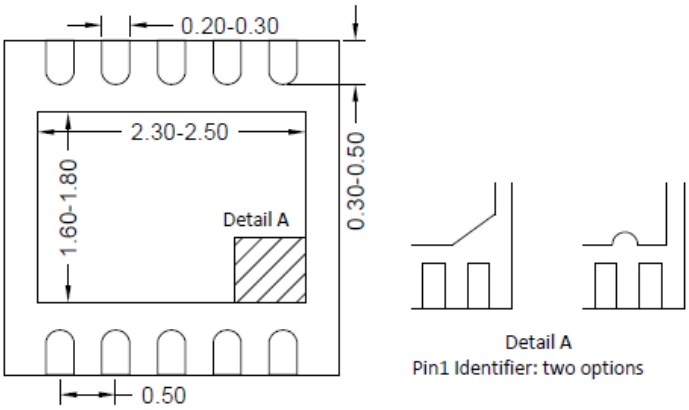


Figure 8. PCB Layout Suggestion

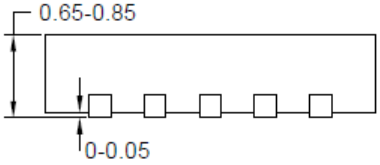
DFN3×3-10 Package Outline



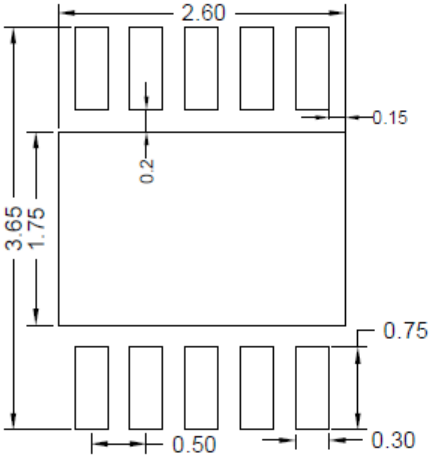
Top View



Bottom View



Side View

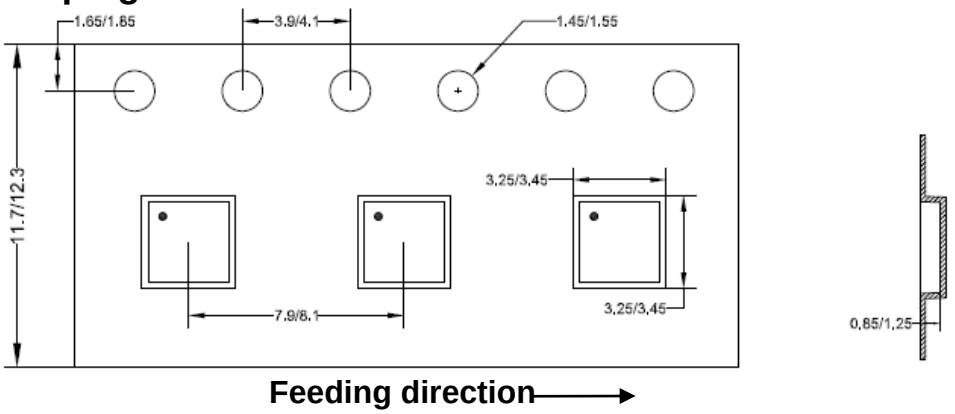


PCB layout (recommended)

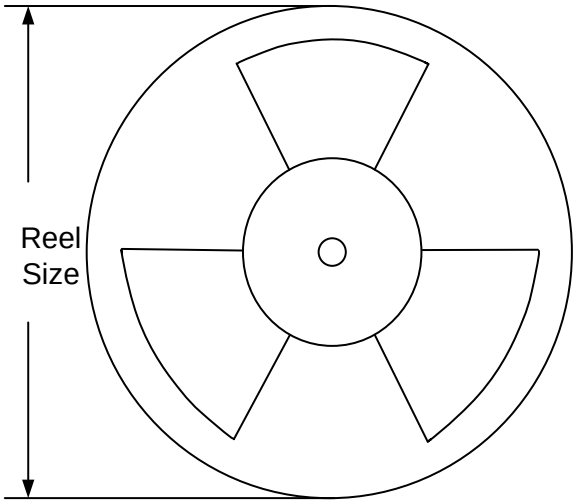
Notes: All dimensions are in millimeters and exclude mold flash and metal burr.

Taping & Reel Specification

DFN3×3-10 Taping Orientation



Carrier Tape & Reel Specification for Packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN3×3	12	8	13"	400	400	5000

Others: NA

Revision History

Date	Revision	Change
Oct.19, 2023	Revision 1.0	Language improvements for clarity.
Jan.10, 2022	Revision 0.9	Initial Release

The revision history provided is for informational purposes only and is believed to be accurate; however, it is not warranted. Please make sure that you have the latest revision.

IMPORTANT NOTICE

1. **Right to make changes.** Silergy and its subsidiaries (hereafter Silergy) reserve the right to change any information published in this document, including but not limited to circuitry, specification and/or product design, manufacturing or descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to Silergy's standard terms and conditions of sale.

2. Applications. Application examples that are described herein for any of these products are for illustrative purposes only. Silergy makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Buyers are responsible for the design and operation of their applications and products using Silergy products. Silergy or its subsidiaries assume no liability for any application assistance or designs of customer products. It is customer's sole responsibility to determine whether the Silergy product is suitable and fit for the customer's applications and products planned. To minimize the risks associated with customer's products and applications, customer should provide adequate design and operating safeguards. Customer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Silergy assumes no liability related to any default, damage, costs or problem in the customer's applications or products, or the application or use by customer's third-party buyers. Customer will fully indemnify Silergy, its subsidiaries, and their representatives against any damages arising out of the use of any Silergy components in safety-critical applications. It is also buyers' sole responsibility to warrant and guarantee that any intellectual property rights of a third party are not infringed upon when integrating Silergy products into any application. Silergy assumes no responsibility for any said applications or for any use of any circuitry other than circuitry entirely embodied in a Silergy product.

3. **Limited warranty and liability.** Information furnished by Silergy in this document is believed to be accurate and reliable. However, Silergy makes no representation or warranty, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. In no event shall Silergy be liable for any indirect, incidental, punitive, special or consequential damages, including but not limited to lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges, whether or not such damages are based on tort or negligence, warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, Silergy' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Standard Terms and Conditions of Sale of Silergy.

4. **Suitability for use.** Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Silergy components in its applications, notwithstanding any applications-related information or support that may be provided by Silergy. Silergy products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of a Silergy product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Silergy assumes no liability for inclusion and/or use of Silergy products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

5. **Terms and conditions of commercial sale**. Silergy products are sold subject to the standard terms and conditions of commercial sale, as published at http://www.silergy.com/stdterms, unless otherwise agreed in a valid written individual agreement specifically agreed to in writing by an authorized officer of Silergy. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Silergy hereby expressly objects to and denies the application of any customer's general terms and conditions with regard to the purchase of Silergy products by the customer.

6. **No offer to sell or license**. Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights. Silergy makes no representation or warranty that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right. Information published by Silergy regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from Silergy under the patents or other intellectual property of Silergy.

For more information, please visit: www.silergy.com