

### General Description

SY205220SFC is an octal, uni-directional, ultra-low capacitance transient voltage suppressor (TVS) designed to provide electrostatic discharge (ESD) protection for super-speed data interfaces. With a typical capacitance of 0.42pF, SY205220SFC is designed to protect against over-voltage and over-current transient events. It complies with IEC 61000-4-2 (ESD), ( $\pm 15\text{kV}$  air,  $\pm 15\text{kV}$  contact discharge), IEC 61000-4-5 (surge) 6A (8/20  $\mu\text{s}$ ).

The combined features of ultra-low capacitance, small size, and high ESD robustness make SY205220SFC ideal for super-speed data ports and high-frequency lines (e.g., HDMI & USB3.x) applications. The low clamping voltage of the SY205220SFC guarantees minimum stress on the protected IC.

Each SY205220SFC device can protect eight high-speed data lines. The SY205220SFC is available in a DFN3.8x1.0-9 package.

### Features

- Fast Turn-On and Low Clamping Voltage
- Ultra-Low Capacitance: 0.42pF @ 1.65V (Typical)
- Transient Protection for Super-Speed Data Lines
  - IEC 61000-4-2 (ESD)  $\pm 15\text{kV}$  (Air)  $\pm 15\text{kV}$  (Contact)
  - IEC 61000-4-5 (Surge) 6A (8/20  $\mu\text{s}$ )
- ESD Protection for High-Speed Differential Signals (Above 10Gbps Channels)
- Protects Eight Data Lines
- Low Leakage Current: 0.01 $\mu\text{A}$  @ 3.6V (Typical)
- Each I/O pin can withstand over 1000 ESD strikes for  $\pm 8\text{kV}$  contact discharge.

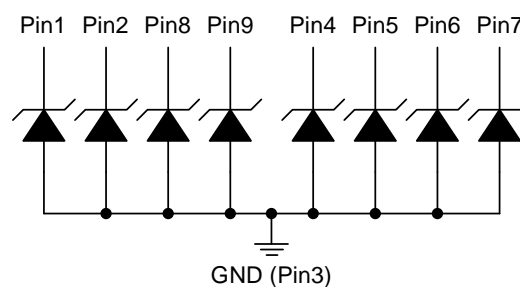
### Applications

- USB 3.1/3.0 Data Line Protection
- USB 3.1/3.0 Type-C
- HDMI 1.3, 1.4, and 2.0

### Mechanical Characteristics

- DFN3.8x1.0-9 Package
- Marking: Device Code, Date Code
- Packaging: Tape and Reel

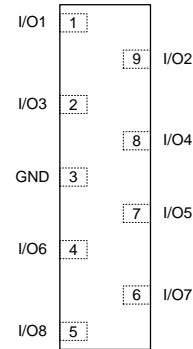
### Circuit Diagram



## Ordering Information

Part Number	Package Type	Top Mark
SY205220SFC	DFN3.8x1.0-9 RoHS Compliant and Halogen Free	DENYWA

## Pinout (Top View)



## Marking Codes



**Note 1:** “DEN” is device code, fixed.

**Note 2:** “YWA” is date code.

Absolute Maximum Rating				
Parameter	Symbol	Min	Max	Unit
Maximum Peak Pulse Current (8/20μs)	$I_{PP}$		6	A
Maximum Peak Pulse Power (8/20μs)	$P_{PK}$		30	W
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	$V_{ESD}$	-15	15	kV
Operating Temperature	$T_{OPT}$	-40	+125	°C
Storage Temperature	$T_{STG}$	-55	+150	°C

Electrical Characteristics $T_A = 25^\circ\text{C}$						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Nominal Reverse Working Voltage	$V_{RWM}$				3.6	V
Reverse Leakage Current @ $V_{RWM}$	$I_R$	$V_{RWM} = 3.6\text{V}, T_A = 25^\circ\text{C}$		0.01	0.1	μA
Reverse Triggering Voltage @ $I_T$	$V_{T1}$	$I_{T1} = 1\text{mA}$	3.7	4.5	6	V
Holding Current	$V_h$	$I_h = 100\text{mA}$	0.8			V
Clamping Voltage @ $I_{PP}$	$V_C(1)$	$I_{PP} = 6\text{A}, t_p = 8/20\mu\text{s}$		4.5		V
Clamping Voltage @ $I_{PP}$	$V_C(1)$	$I_{PP} = 16\text{A}, t_p = 10/100\text{ns}$		6.0		V
Dynamic Resistance	$R_{DYN(1,2)}$	$t_p = 10/100\text{ns}$		0.30		Ω
Parasitic Capacitance	$C_{ESD(1)}$	$V_R = 1.65\text{V}, f = 1\text{MHz}$		0.42	0.55	pF

**Note 1:** Guaranteed by design and not subject to production test.

**Note 2:**  $R_{DYN}$  calculated based on  $I_{PP}=8\text{A}$  to  $I_{PP}=16\text{A}$ ,  $t_p = 10/100\text{ns}$ .

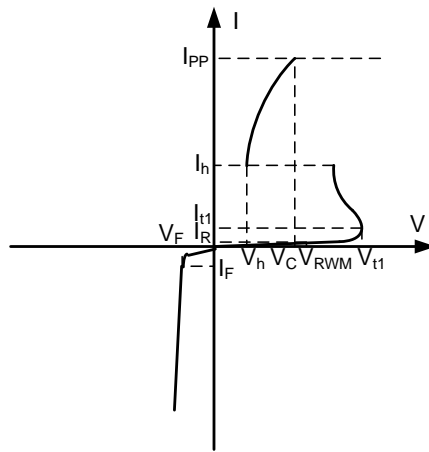
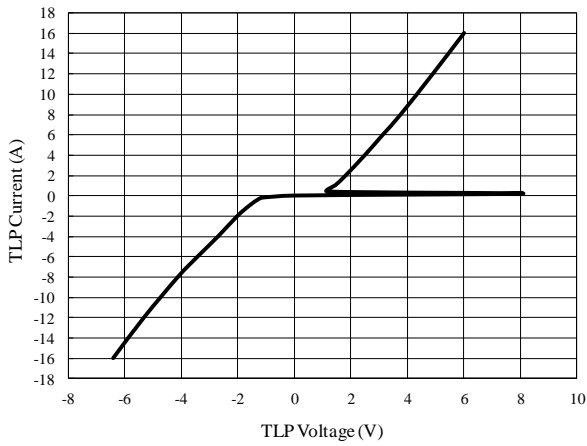


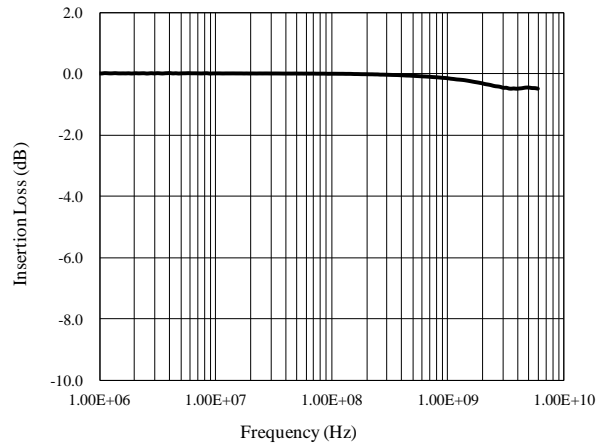
Figure 1. Uni-directional TVS

## Typical Performance Characteristics

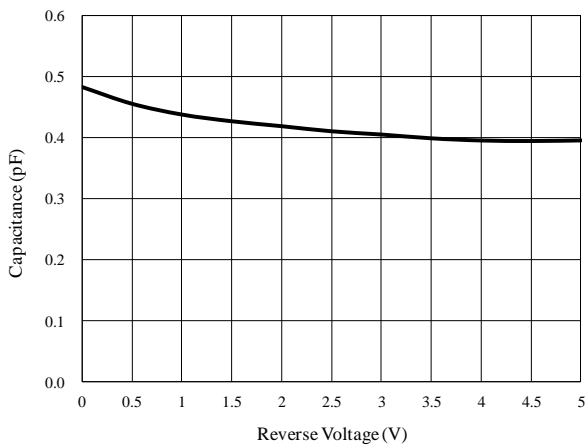
### TLP Testing of I/O to GND



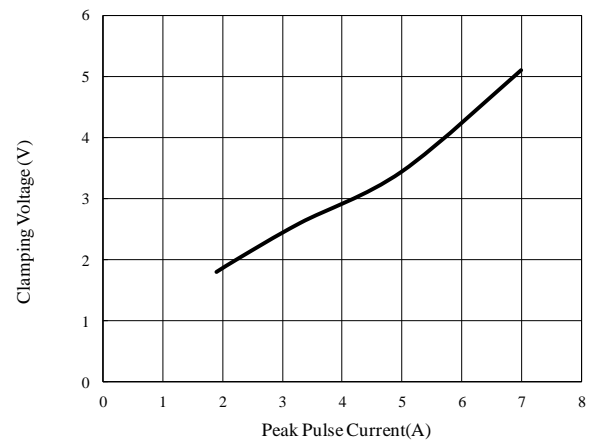
### Insertion Loss S21 of I/O to GND



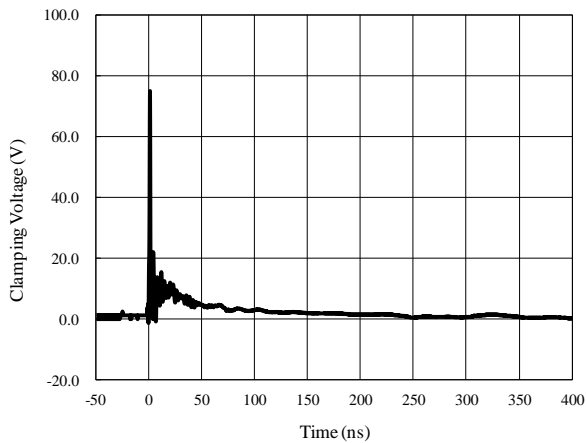
### Capacitance vs. Voltage of I/O to GND



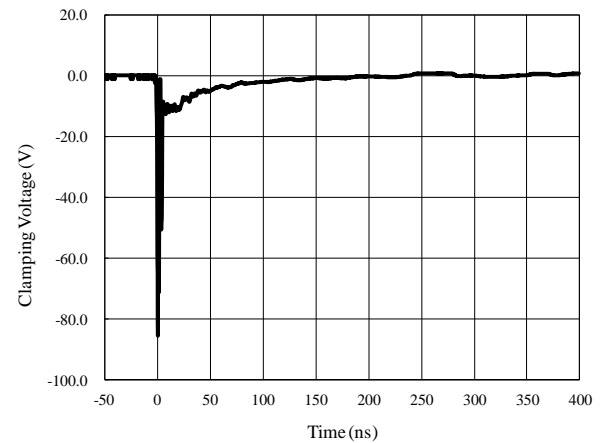
### Clamping Voltage vs. Peak Pulse Current (8/20μs)



### ESD Clamping of I/O to GND (+8kV Contact per IEC 61000-4-2)



### ESD Clamping of I/O to GND (-8kV Contact per IEC 61000-4-2)



## Application Information

### PCB Pin Connections

SY205220SFC provides ESD protection for eight data lines simultaneously. The pin connections of SY205220SFC are shown in Figure 2. Eight parallel data lines, from the protected device and going to the I/O port connector, can be connect directly to the eight SY205220SFC I/O pins.

Pin3 of SY205220SFC is the GND pin and should connect to the ground. All path lengths connected to pins of SY205220SFC should be as short as possible to minimize the parasitic inductance

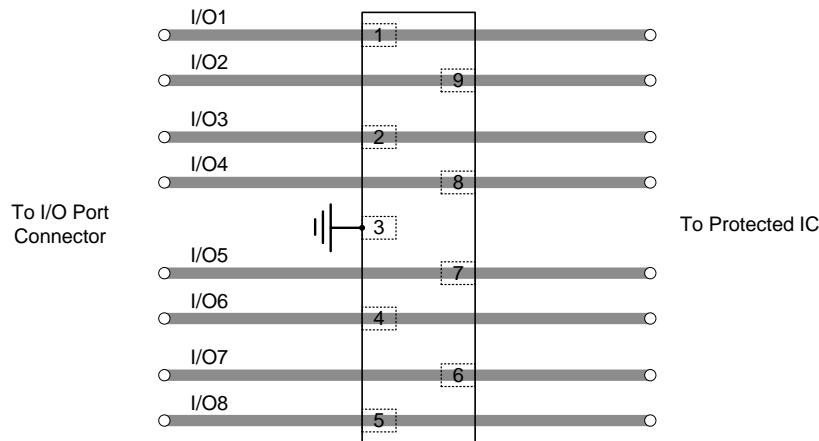


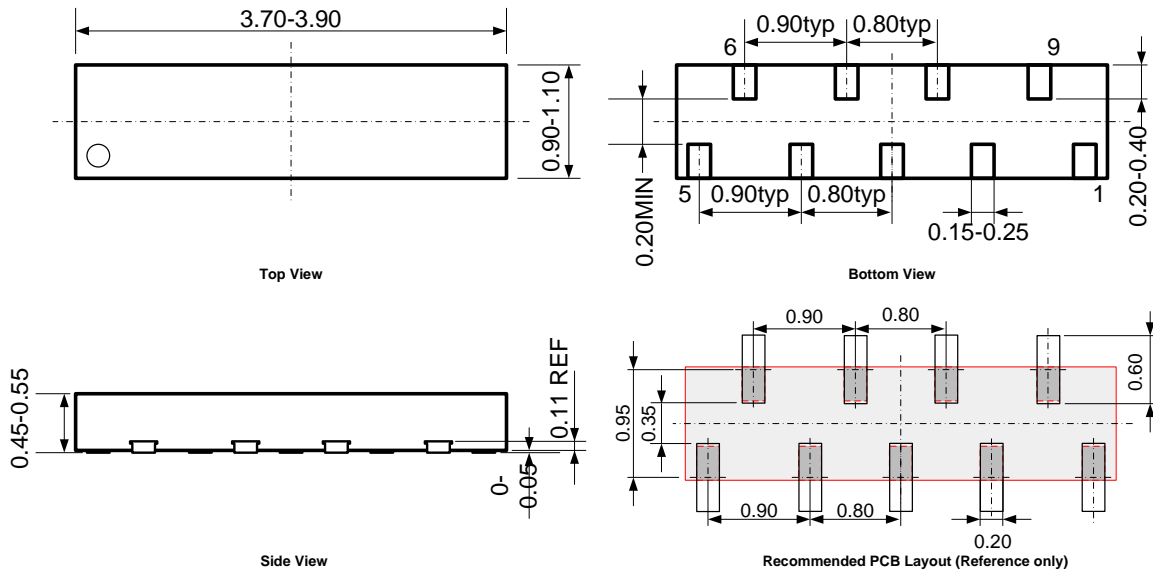
Figure 2. SY205220SFC Pin Connections in PCB

### PCB Layout Guidelines

For optimum ESD protection and circuit performance, the following PCB layout guidelines are recommended:

- Place SY205220SFC as close to the connector or terminal ports as possible.
- Use a large via to connect the SY205220SFC pin to the ground.
- Avoid running signals near board edges.
- While routing the signals avoid trace discontinuities to minimize impedance changes and reduce reflections.
- The SY205220SFC should be placed near the protected lines.
- The distance between the SY205220SFC ground pin and the GND reference path should be as short as possible.

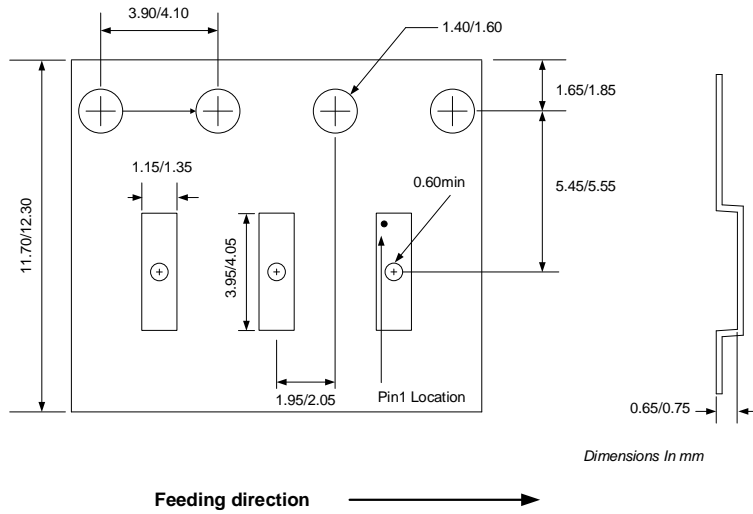
## DFN3.8x1.0-9 Package Outline



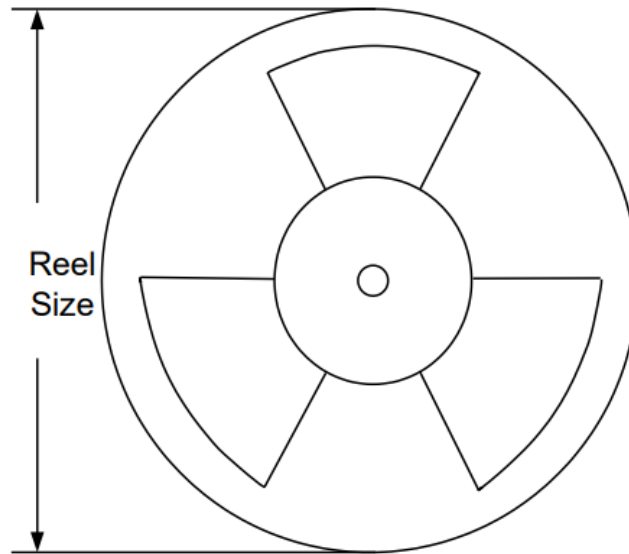
**Note:** All dimensions are in millimeters and exclude mold flash and metal burr.

## Tape and Reel Specification

### DFN3.8x1.0-9 Taping Orientation



### Carrier Tape & Reel Specification for Packages



Package Types	Tape Width (mm)	Pocket Pitch(mm)	Reel Size (Inch)	Qty per Reel(pcs)
DFN3.8x1.0-9	12	4	7"	3000



**Revision History**

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Revision Number	Revision Date	Description	Pages changed
0.9	07/02/2021	Initial Release	
1.0	07/02/2022	Production Release	



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