SY26083

21μA Ultra Low I_Q, 3A, 2.2MHz Synchronous Step Down Regulator

General Description

The SY26083 is a high efficiency synchronous step-down DC/DC regulator capable of delivering up to 3A output current. It can operate over a wide input voltage range from 2.5V to 5.5V and integrates main and synchronous MOSFETs with very low $R_{DS\,(ON)}$ to minimize the conduction loss.

The 2.2 MHz switching frequency permits low output-voltage ripple and reduces external inductor and capacitor sizes. The SY26083 also provides overtemperature protection (OTP), short-circuit protection (SCP), overvoltage protection (OVP) and internal soft-start to limit inrush current during power-on.

The SY26083 is available in a space saving, low profile DFN1.5mm×1.5mm-6 pin package.

Features

- 2.5V to 5.5V Input Voltage Range
- Ultra-Fast Load Transient Speed
- Low $R_{DS(ON)}$ for Power MOSFETs (Top/Bottom): 38mΩ /30mΩ
- High Switching Frequency 2.2MHz Minimizes the External Components
- ±1% Feedback or Output Voltage Accuracy (Full Temperature Range)
- PFM Mode for Light Load Efficiency
- 21μA Operating Quiescent Current
- Internal Soft-start Limits the Inrush Current
- 100% Dropout Operation
- Output Auto Discharge Function
- Power Good Indicator
- Auto Recovery for SCP/OVP/OTP Protection
- RoHS Compliant and Halogen Free
- Compact Package: DFN1.5×1.5-6

Applications

- Portable Electronics
- Notebooks and Desktop PCs
- Smart Phones

Typical Application

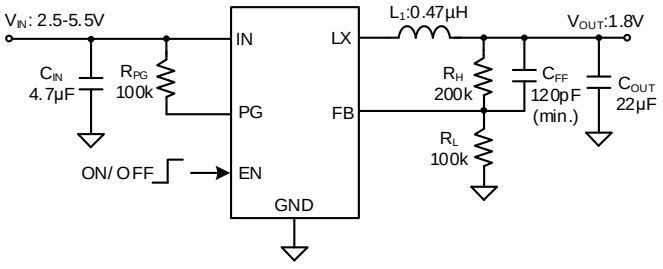


Figure1. Schematic Diagram

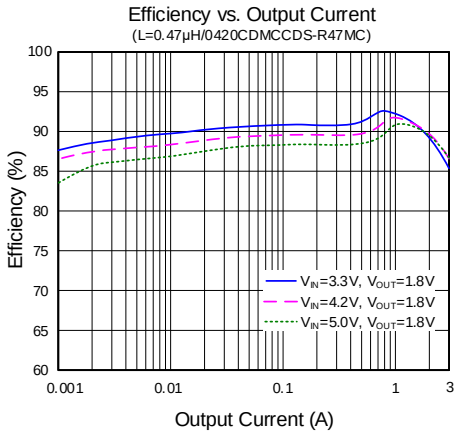
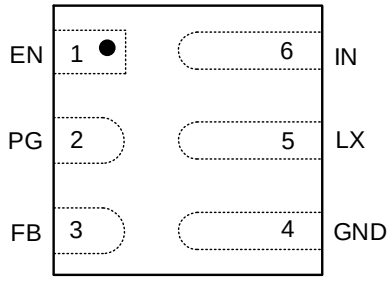


Figure2. Efficiency vs. Output Current

Ordering Information

Ordering Part Number	Package type	Top Mark
SY26083DQD	DFN1.5×1.5-6 RoHS Compliant and Halogen Free	**2a*xyz***

Pinout (top view)



Pin Description

Pin No	Pin Name	Pin Description
1	EN	Enable control. Pull high to turn on. Do not leave floating.
2	PG	Power good indicator. Open Drain Output. Low if the V_{FB} < 91.5% or the V_{FB}>108.5% of V_{REF}; high-impedance otherwise. Connect a pull-up resistor to the desired external voltage rail.
3	FB	Output feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{OUT}=0.6\times(1+R_H/R_L)$.
4	GND	Power ground pin.
5	LX	Inductor pin. Connect this pin to the switching node of inductor.
6	IN	Input pin. Decouple this pin to the GND pin with at least a 4.7μF ceramic capacitor.

Block Diagram

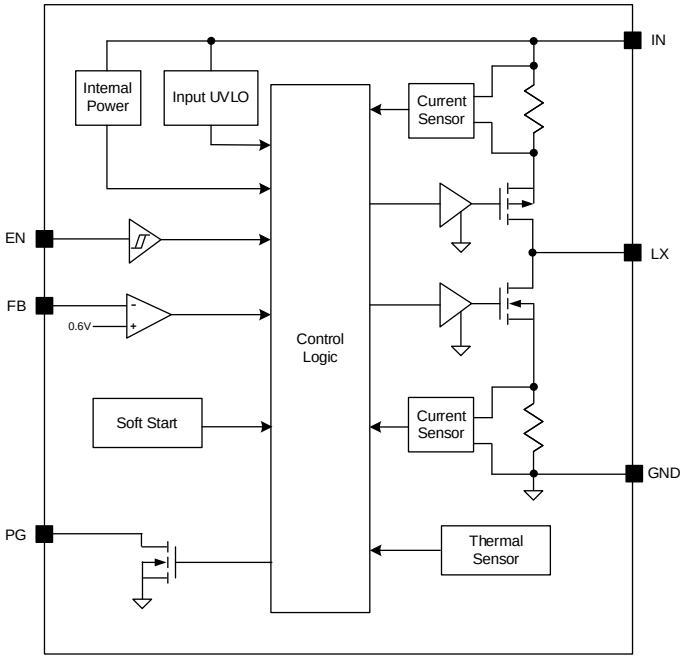


Figure3. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
IN	-0.3	6	V
FB, EN, PG	-0.3	IN + 0.6	
LX	-0.3	6	
LX, 20ns duration	-3	7	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering,10s)		260	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 2)	Min	Max	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance		62	°C/W
θ_{JC} Junction-to-Case Thermal Resistance		8	
P_D Power Dissipation T_A = 25°C		1.6	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
IN	2.5	5.5	V
Junction Temperature	-40	125	°C

Electrical Characteristics

(T_J = -40°C ~125°C, and V_{IN} = 2.5V to 5.5V. Typical values are at T_J = 25°C and V_{IN} = 5V, unless otherwise specified. The values are guaranteed by test, design or statistical correlation.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.5		5.5	V
Input UVLO Threshold	V_{UVLO}	V_{IN} falling	2.1	2.2	2.3	
Input UVLO Hysteresis	V_{HYS}			160		mV
Quiescent Current	I_Q	V_{FB}=105%×V_{REF}		21	40	μA
Shutdown Current	I_{SHDN}	V_{EN}=0V, T_A=25°C		0.05	0.5	
Feedback Reference Voltage	V_{REF}	I_{OUT}=1A, CCM	0.594	0.6	0.606	V
Output Voltage Load Regulation (Note 4)	ΔV_{LDR}	I_{OUT}=0.5A to 3A, V_{OUT}=1.8V		0.1		%/A
Output Discharge FET R_{ON}	R_{DIS}	V_{EN}=0V, V_{LX}=0.4V, T_J=25°C		8	12	Ω
Top FET R_{ON}	$R_{DS(ON)1}$	V_{IN}=5V, T_J=25°C		38	57	mΩ
Bottom FET R_{ON}	$R_{DS(ON)2}$	V_{IN}=5V, T_J=25°C		30	45	
EN Input Voltage High	$V_{EN, H}$		1.0			V
EN Input Voltage Low	$V_{EN, L}$				0.4	
EN Leakage Current	$I_{EN, LKG}$	EN=high		0.01	1	μA
Power Good Threshold	V_{PG}	V_{FB} falling, PG from high to low	88	91.5	94.5	%
		V_{FB} rising, PG from low to high	93	96	99	
		V_{FB} rising, PG from high to low	105.5	108.5	112	
		V_{FB} falling, PG from low to high	101	104	107	
Power Good Delay	$t_{PG,R}$	PG from low to high		100		μs
	$t_{PG,F}$	PG from high to low		20		
Power Good Output Low	$V_{PG, L}$	I_{PG}=1mA			0.4	V
PG Leakage Current	$I_{PG, LKG}$	V_{PG}=5V		0.01	1	μA
Min ON Time (Note 4)	$t_{ON,MIN}$	T_J=25°C		110	150	ns
Maximum Duty Cycle (Note 4)	D_{MAX}		100			%
Soft-start Time	t_{SS}	from EN high to 95% of V_{OUT} nominal, T_J=25°C	1.2	2	3	ms
Switching Frequency	f_{SW}	I_{OUT}=1A, V_{OUT}=1.8V, T_J=25°C	1.76	2.2	2.64	MHz
Top FET Current Limit	$I_{LMT, TOP}$		4	4.6	5.4	A
Bottom FET Current Limit	$I_{LMT, BOT}$		3	3.6	4.4	
Thermal Shutdown Temperature (Note 4)	T_{SD}			150		°C
Thermal Shutdown Hysteresis (Note 4)	T_{HYS}			20		

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Package thermal resistance is measured in the natural convection at T_A=25°C on a 6cm×6cm size 2-oz two-layer Silergy Evaluation Board.

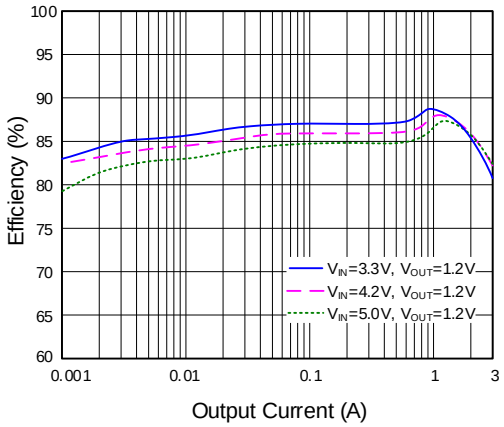
Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Guaranteed by design.

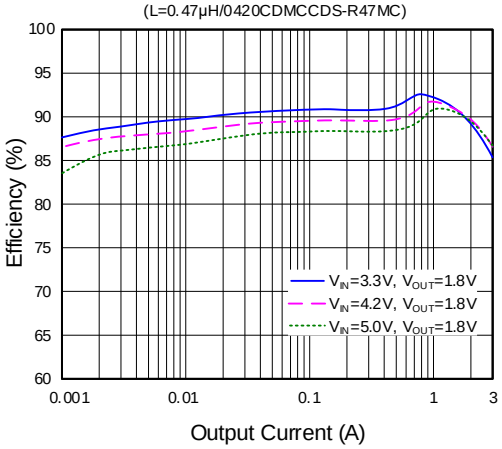
Typical Performance Characteristics

(T_A = 25°C, V_{IN} = 5V, L = 0.47μH, C_{OUT} = 2×10μF, unless otherwise specified.)

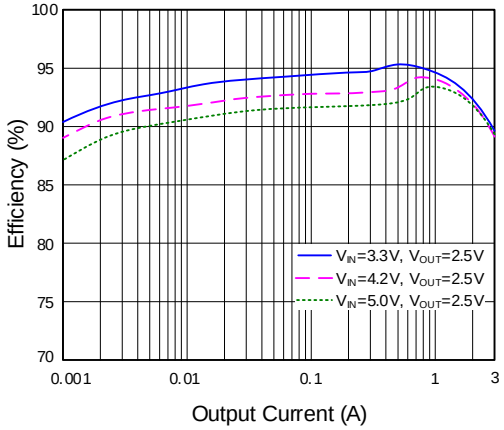
Efficiency vs. Output Current
(L=0.33μH/0420CDMCCDS-R33MC)



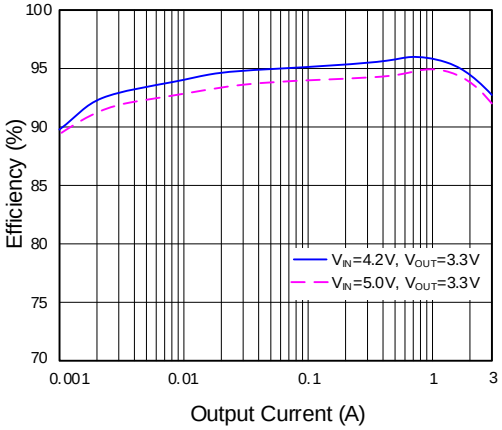
Efficiency vs. Output Current
(L=0.47μH/0420CDMCCDS-R47MC)



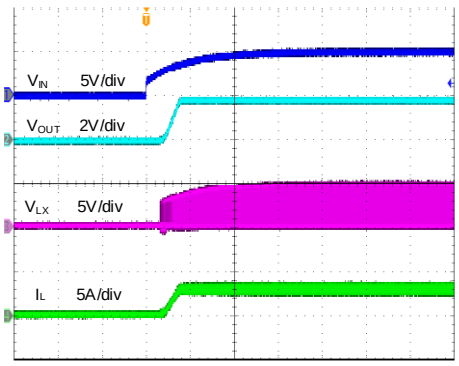
Efficiency vs. Output Current
(L=0.47μH/0420CDMCCDS-R47MC)



Efficiency vs. Output Current
(L=0.47μH/0420CDMCCDS-R47MC)

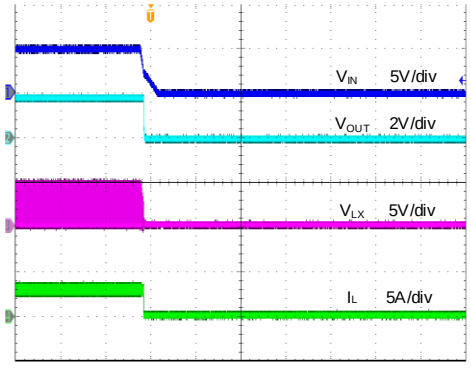


Startup from V_{IN}
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=3A)



Time (4ms/div)

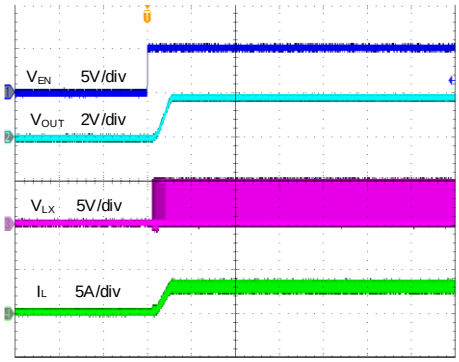
Shutdown from V_{IN}
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=3A)



Time (4ms/div)

Startup from EN

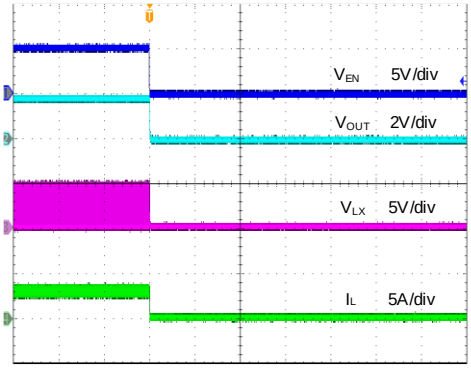
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=3A)



Time (4ms/div)

Shutdown from EN

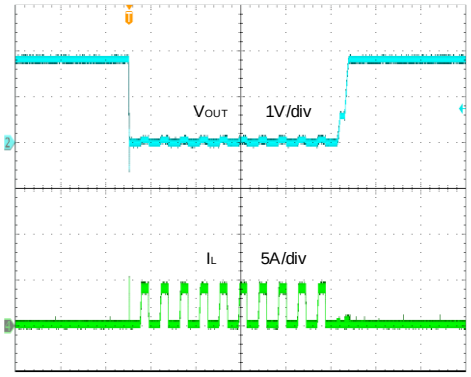
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=3A)



Time (4ms/div)

Short Circuit Protection

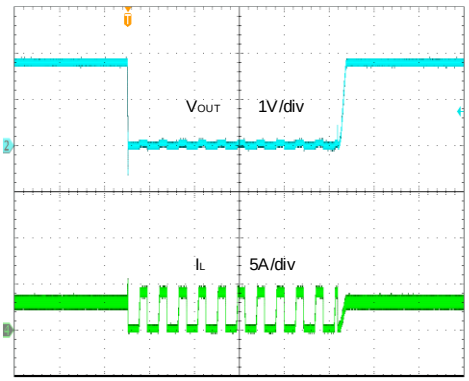
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=0A~short)



Time (10ms/div)

Short Circuit Protection

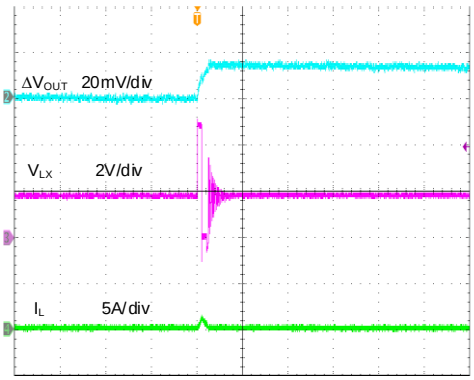
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=3A~short)



Time (10ms/div)

Output Ripple

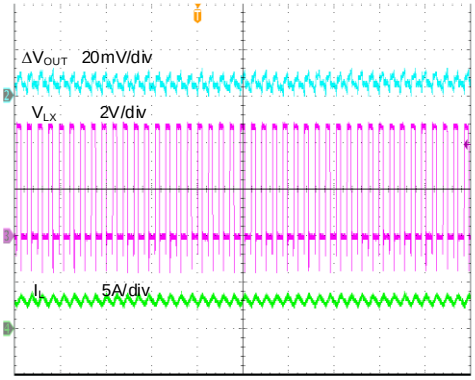
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=0A)



Time (2μs/div)

Output Ripple

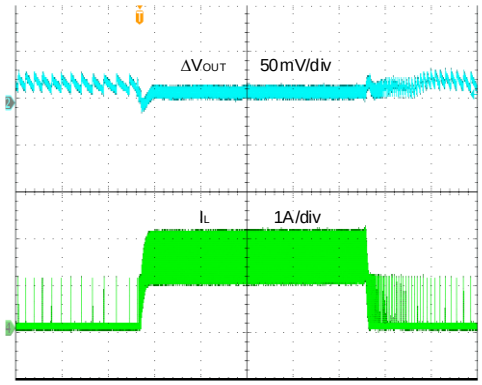
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=3A)



Time (2μs/div)

Load Transient

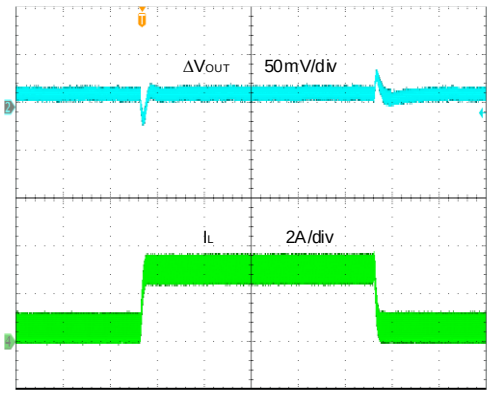
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=0~1.5A)



Time (100μs/div)

Load Transient

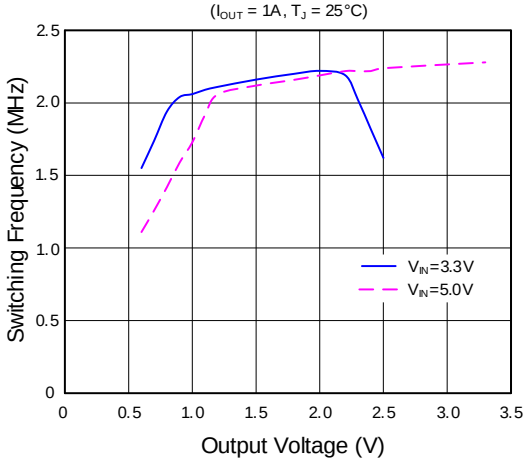
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=0.3~3A)



Time (100μs/div)

Switching Frequency vs. Output Voltage

(I_{OUT} = 1A, T_J = 25°C)



Operation

The SY26083 is a high efficiency 2.2MHz synchronous step-down DC/DC regulator capable of delivering up to 3A output current. It can operate over a wide input voltage range from 2.5V to 5.5V and integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

The SY26083 uses the instant PWM architecture to achieve fast transient responses for high step-down applications and high efficiency at light loads.

The SY26083 provides protection functions such as cycle by cycle current limit and thermal shutdown protection. Low output voltage ripple, small external inductor and capacitor sizes are achieved with 2.2MHz switching frequency.

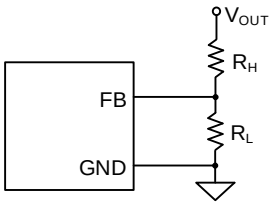
Applications Information

The selection process for the input capacitor C_{IN}, output capacitor C_{OUT}, output inductor L, and feedback resistors (R_H and R_L) is described in the following sections.

Feedback Resistor Divider R_H and R_L

Choose R_H and R_L to configure the output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_H and R_L. A value between 10kΩ and 1MΩ is recommended for both resistors. If V_{OUT} is 1.8V and R_H = 100kΩ is selected, then using following equation, R_L can be calculated to be 49.9kΩ:

$$R_L = \frac{0.6V}{V_{OUT} - 0.6V} \times R_H$$



Input Capacitor C_{IN}

Input filter capacitors reduce the ripple voltage on the input, filter the switched current drawn from the input supply, and reduce potential EMI. When selecting an input capacitor, it is recommended to select a voltage rating at least 20% greater than the maximum voltage of the input supply and a temperature rating higher than the system requirements. X5R series ceramic capacitors are most often selected due to their small size, low cost, surge-current capability, and high RMS current ratings over a wide temperature and voltage range. Systems that are powered by a wall adapter or other long and therefore inductive wires may be susceptible to significant inductive ringing at the input to the device. In these cases, consider adding some bulk capacitance like electrolytic, tantalum, or polymer type capacitors. Using a combination of bulk capacitors (to reduce overshoot or ringing) in parallel with ceramic capacitors (to meet the RMS current requirements) is helpful in these cases.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

The worst-case condition occurs at D = 0.5, then

$$I_{CIN\_RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplicity, use an input capacitor with an RMS current rating greater than 50% of the maximum load current.
The input capacitor value determines the input voltage ripple of the converter. If there is a voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification.
Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated using the formula:

$$V_{CIN\_RIPPLE,CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1 - D)$$

The worst-case condition occurs at D = 0.5, then

$$V_{CIN\_RIPPLE,CAP,MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

A single 4.7µF X5R capacitor is sufficient for most applications.

Output Capacitor C_{OUT}

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use X5R or better grade ceramic capacitors with 6.3V rating and more than 2×10µF capacitance.

For applications where the design must meet stringent ripple requirements, the following considerations must be followed.

The output voltage ripple at the switching frequency is caused by the inductor-current ripple (ΔI_L) on the output

capacitor's ESR (ESR ripple), as well as the stored charge (capacitive ripple). When calculating total ripple, consider both.

$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$
$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

The measured capacitive ripple might be higher because the effective capacitance for ceramic capacitors decreases with the voltage across the terminals. The voltage derating is usually included as a chart in the capacitor datasheet, and the ripple can be recalculated after taking the target output voltage into account.

Output Inductor L

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT} / V_{IN,MAX})}{f_{sw} \times I_{OUT,MAX} \times 40\%}$$

where f_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY26083 is tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > \mathrm{I_{OUT,MAX}} + \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{2 \times f_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<25mΩ to achieve a good overall efficiency.

Inductor vs. Output Capacitor

The ripple base control strategy needs very little C_{OUT} for stable operation. Too large inductance and output capacitance might lead to instability. The recommended inductance and output capacitance range are shown as below:

Inductance vs. Output Capacitance Selection Table (Note 5)

L (µH)	C_{OUT} (µF)					
	22	44	88	120	180	220
0.33	Note6	√	√	√	√	√
0.47	√	√	√	√	√	√
0.68	√	√	√	√	×	×

Note 5: Tested with 120pF feedforward capacitor.
Note 6: Only suitable for V_{OUT}<2.0V application.

Minimum Duty Cycle and Maximum Duty Cycle

In the constant on-time (COT) architecture, there is no limitation for small duty cycles, since even at very low duty cycles, the switching frequency can be reduced as needed once the on-time is close to the minimum on time, to always ensure a proper operation.

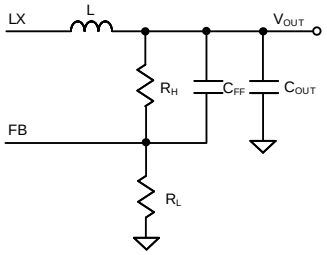
The device will enter 100% dropout mode if the output voltage is very close to the input voltage, while the top FET is constantly turned on, the bottom FET is turned off.

Power Good Indicator

The power good indicator is an open drain output controlled by a window comparator connected to the feedback signal. If V_{FB} is greater than $V_{PG,R}$ and less than V_{OVP} for at least the power good delay time (low to high), PG will be high-impedance. Otherwise, it is pulled low. PG should be connected to V_{IN} or another voltage source through a resistor (e.g., 10kΩ~100kΩ).

Load Transient Considerations

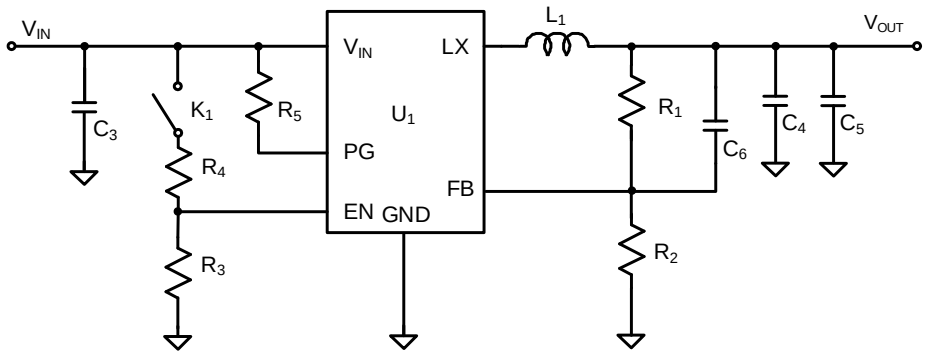
The SY26083 integrates the compensation components to achieve good stability and fast transient responses. Adding a small ceramic capacitor with more than 120pF capacitance in parallel with R_H may further speed up the load transient responses and is thus highly recommended for applications with large load-transient step requirements.



OCP and UVP Protection

TheSY26083 uses cycle by cycle current limit for both high-side (HS) and low-side (LS) MOSFETs. If the high side power MOSFET current gets higher than the peak current limit threshold, it will turn off and the low side power MOSFET will turn on. If the low side MOSFET current gets higher than the valley current limit threshold, the low side FET will stay on until the low side MOSFET current decreases below the valley current limit threshold. As a result, both peak and valley current are limited. If the load current continues to increase in these conditions, the output voltage will drop. When the output voltage falls below 33% of the target voltage, the UVP will be triggered and the device will operate in hic-cup mode. The hiccup on time and hiccup off time ratio is 1:1. If the overcurrent condition is removed, the device will return to normal operation.

Application Schematic (V_{OUT} = 1.8V)



BOM List

Reference Designator	Description	Part Number	Manufacturer
U_1	3A, Buck	SY26083DQD	Silergy
C_3, C_4, C_5	10μF/16V/X5R,1206	GRM319R61C106KE15D	muRata
C_6	220pF/50V/C0G,0603	GRM1885C1H221JA01D	muRata
L_1	0.47μH/inductor	0420CDMCCDS-R47MC	Sumida
R_1, R_5	100kΩ ,1%,0603		
R_2	49.9kΩ ,1%,0603		
R_3	1MΩ, 1%, 0603		
R_4	10kΩ ,1%,0603		

Layout Design

The following components should be placed close to the IC: C_{IN}, L, R_H, R_L and C_{FF}.

1) It is desirable to maximize the PCB copper area connecting to GND pin to improve thermal performance and reduce noise. If the board space allows a large copper pour on the top layer is highly desirable. Place vias connected to a GND plane for heat sinking.

2) C_{IN} must be close to Pins IN and GND. The loop area formed by C_{IN} and GND must be minimized.

3) The PCB copper area associated with the LX pin must be minimized to reduce EMI.

4) The components R_H and R_L, and the trace connecting to the FB pin must not be adjacent to the LX net on the PCB layout to avoid the noise coupling.

5) The feedback sampling point should be connected to C_{OUT} rather than the inductor output terminal.

6) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a 1MΩ pull down resistor between the EN and GND pins to prevent noise from falsely turning on the regulator during system shutdown.

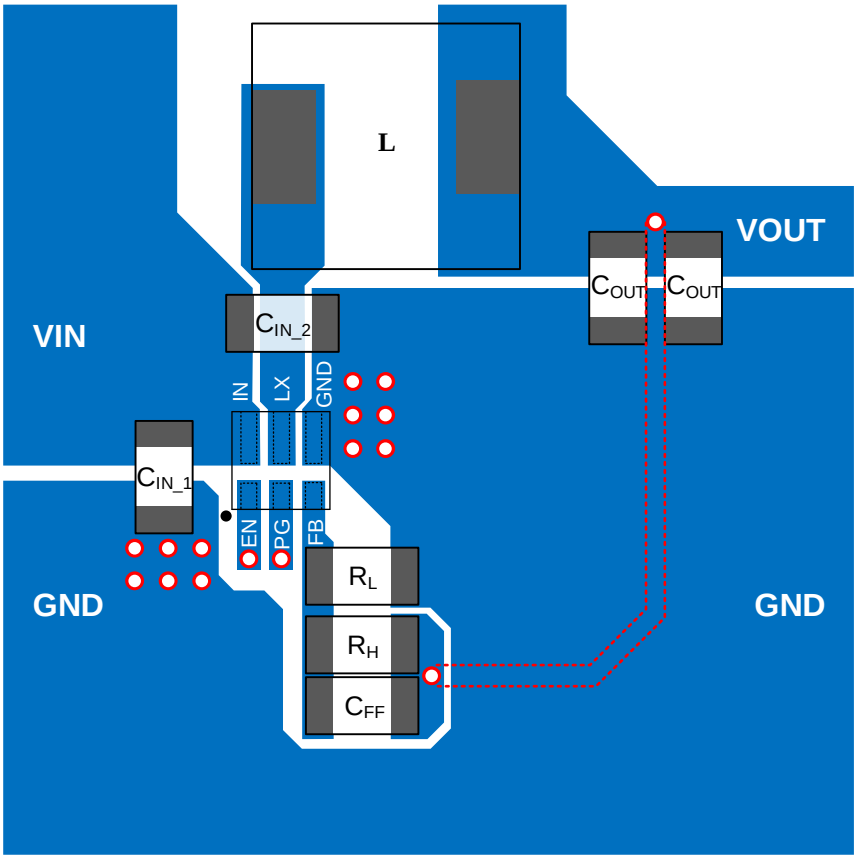
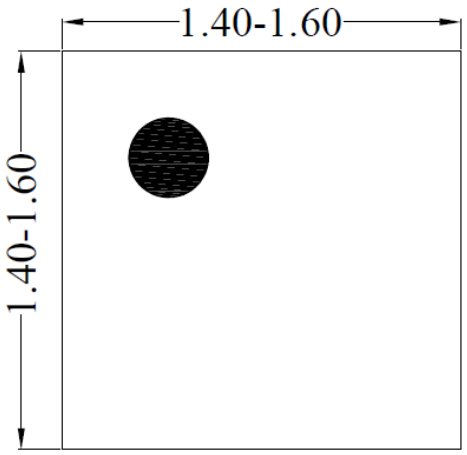
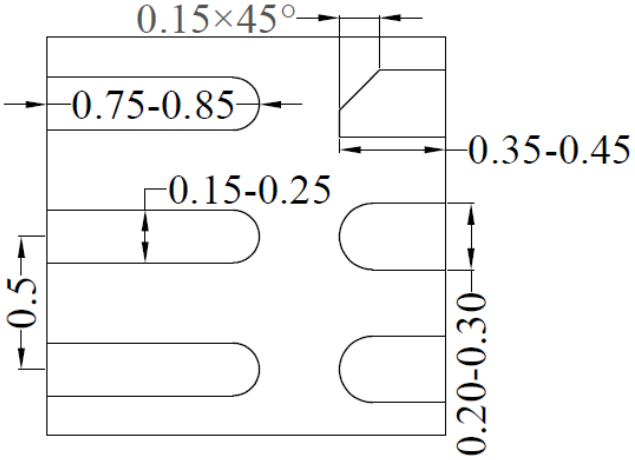


Figure4. PCB Layout Suggestion

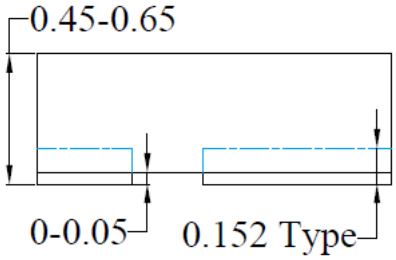
DFN1.5x1.5-6 Package Outline



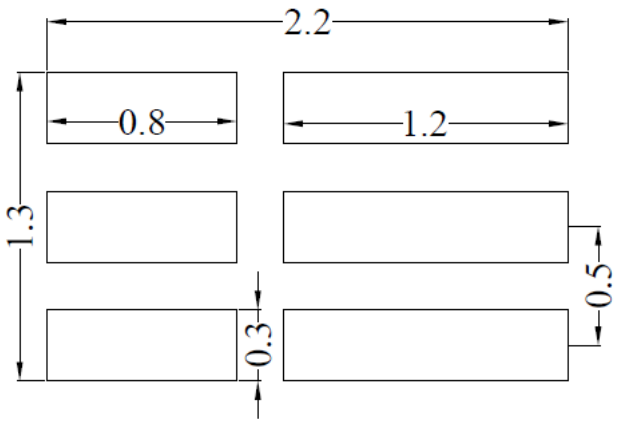
Top View



Bottom View



Front View



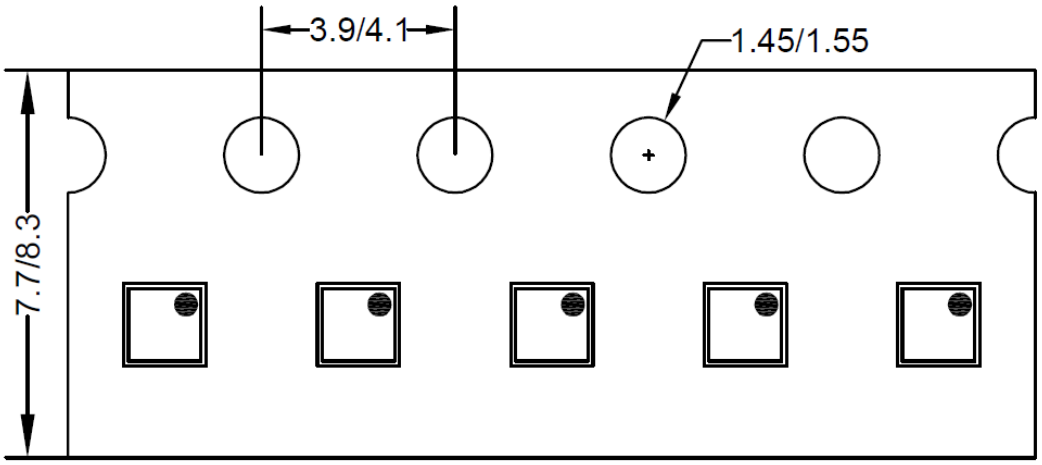
Recommended PCB layout
(only for reference)

Notes: 1, All dimension in millimeter and exclude mold flash & metal burr.

Tape and Reel Specification

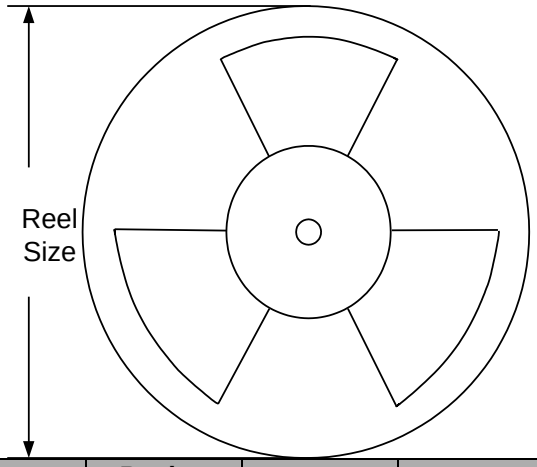
1. Tape orientation

DFN1.5×1.5



Feeding direction ⟶

2. Carrier Tape and Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN1.5×1.5	8	4	7"	400	160	3000

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change
Mar.26, 2024	Revision 1.0	Product Release
Nov.28, 2022	Revision 0.9	Initial Release

IMPORTANT NOTICE

1. **Right to make changes.** Silergy and its subsidiaries (hereafter Silergy) reserve the right to change any information published in this document, including but not limited to circuitry, specification and/or product design, manufacturing or descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to Silergy's standard terms and conditions of sale.

2. Applications. Application examples that are described herein for any of these products are for illustrative purposes only. Silergy makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Buyers are responsible for the design and operation of their applications and products using Silergy products. Silergy or its subsidiaries assume no liability for any application assistance or designs of customer products. It is customer's sole responsibility to determine whether the Silergy product is suitable and fit for the customer's applications and products planned. To minimize the risks associated with customer's products and applications, customer should provide adequate design and operating safeguards. Customer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Silergy assumes no liability related to any default, damage, costs or problem in the customer's applications or products, or the application or use by customer's third-party buyers. Customer will fully indemnify Silergy, its subsidiaries, and their representatives against any damages arising out of the use of any Silergy components in safety-critical applications. It is also buyers' sole responsibility to warrant and guarantee that any intellectual property rights of a third party are not infringed upon when integrating Silergy products into any application. Silergy assumes no responsibility for any said applications or for any use of any circuitry other than circuitry entirely embodied in a Silergy product.

3. **Limited warranty and liability.** Information furnished by Silergy in this document is believed to be accurate and reliable. However, Silergy makes no representation or warranty, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. In no event shall Silergy be liable for any indirect, incidental, punitive, special or consequential damages, including but not limited to lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges, whether or not such damages are based on tort or negligence, warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, Silergy' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Standard Terms and Conditions of Sale of Silergy.

4. **Suitability for use.** Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Silergy components in its applications, notwithstanding any applications-related information or support that may be provided by Silergy. Silergy products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an Silergy product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Silergy assumes no liability for inclusion and/or use of Silergy products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

5. **Terms and conditions of commercial sale**. Silergy products are sold subject to the standard terms and conditions of commercial sale, as published at http://www.silergy.com/stdterms, unless otherwise agreed in a valid written individual agreement specifically agreed to in writing by an authorized officer of Silergy. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Silergy hereby expressly objects to and denies the application of any customer's general terms and conditions with regard to the purchase of Silergy products by the customer.

6. **No offer to sell or license**. Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights. Silergy makes no representation or warranty that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right. Information published by Silergy regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from Silergy under the patents or other intellectual property of Silergy.

For more information, please visit: www.silergy.com