SY28846B

2.7V-18V Load Switch With Reverse Blocking

General Description

The SY28846B protection switch is a compact power management device with a full suite of protection functions, including a low-power device sleep (DevSleep) mode. The wide operating range allows control of many popular DC BUS voltages.

Integrated back-to-back MOSFETs provide bidirectional current control, making the device well-suited for systems with load-side energy reservoirs that must not drain back to a failed supply BUS.

The device provides many programmable features, including overcurrent, dVo/dt ramp, over-voltage, and under-voltage thresholds using very few external components. The device provides PGOOD, /FLT and precise current monitor output for system status monitoring and downstream load control. The precise programmable and low I_Q DevSleep mode simplifies SSD power management design.

The SY28846B provides true reverse current blocking by monitoring V_{IN} < (V_{OUT} - 25mV). This function supports swift change over to a boosted voltage energy storage element in systems with higher backup voltage than the BUS voltage.

The SY28846B also integrates latch-off protection.

Features

- 2.7V to 18V Operating Voltage, 30V (Max)
- Ultra-low $R_{DS(ON)}$: 42mΩ R_{ON} (Typical)
- 0.6A to 5.3A Adjustable Current Limit (±8%)
- IMON Current Indicator Output (±8%)
- Operating I_Q: 115μA (typ.)
- Reverse Current Blocking
- Programmable dV/dt Control
- Power Good and Fault Outputs
- 4ms Fault Timer Then Shutoff
- -40℃ to 125℃ Junction Temperature Range
- Compact Package: QFN3×4-20

Applications

- PCIe/SATA/SAS HDD and SSD Drives
- Enterprise and Micro Servers
- Smart Load Switch
- PLCs, SS Relays, and Fan Control
- RAID Cards - Holdup Power Management
- Telecom Switches and Routers
- Adapter Powered Devices

Typical Application Circuit

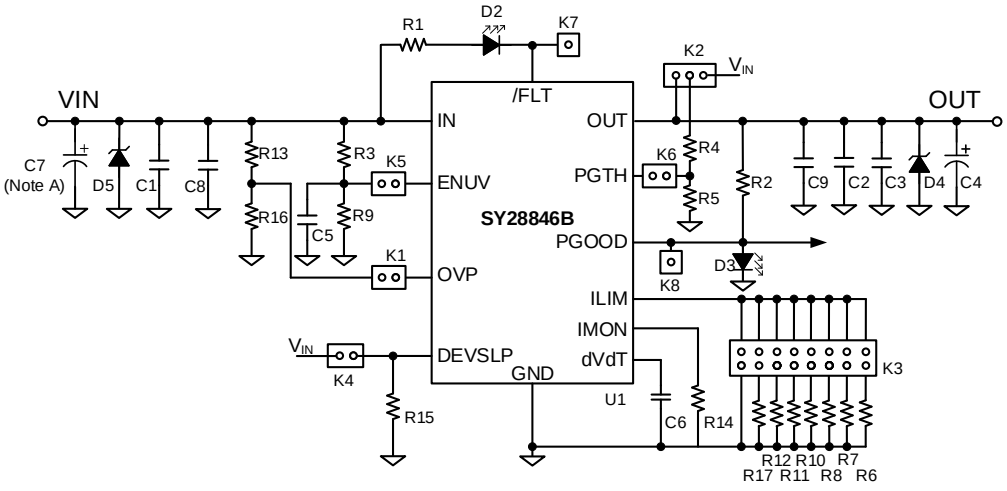


Figure.1 Schematic Diagram

Note: Optional and only for overload test, not recommended for hot-plug applications

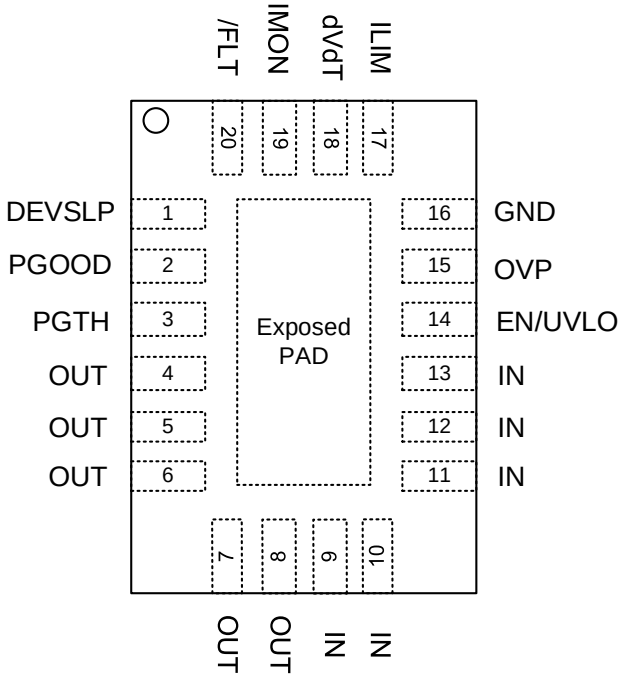
Ordering Information

Ordering Number	Package Type	Top Mark
SY28846BQSQ	QFN3×4-20 RoHS Compliant and Halogen Free	**EAW*xyz***

Device code: **EAW**

x=year code, y=week code, z= lot number code

Pinout (Top View)



Pin Name	Pin NO.	I/O	Pin Description
DEVSLP	1	I	Active High. DevSleep Mode control. A high on this pin will activate the DevSleep mode (Low Power Mode).
PGOOD	2	O	Active High. A high indicates PGTH has crossed the threshold value. It is an open drain output.
PGTH	3	I	Positive input of PGOOD comparator.
OUT	4-8	O	Power output of the device.
IN	9-13	I	Power input and supply voltage of the device.
EN/UVLO	14	I	Input for setting programmable undervoltage lockout threshold. An undervoltage event will open the internal FET and assert /FLT to indicate power failure. When pulled to GND, resets the fault latch in the SY28846B.
OVP	15	I	Input for setting programmable overvoltage protection threshold. An overvoltage event will open the internal MOSFET and assert /FLT to indicate overvoltage.
GND	16	-	Ground pin.
ILIM	17	I/O	A resistor from this pin to GND sets the overload and short-circuit current limit.
dVdT	18	I/O	A capacitor from this pin to GND sets the ramp rate of output voltage.
IMON	19	O	This pin sources a scaled down ratio of current through the internal FET. A resistor from this pin to GND converts current to proportional voltage, and can be used as an analog current monitor.
/FLT	20	O	Fault event indicator -goes low to indicate fault condition due to undervoltage, overvoltage, reverse voltage, circuit breaker timeout, and thermal shutdown events. It is an open drain output.
Exposed Pad	-		The GND terminal must be connected to the Exposed PAD. This exposed PAD must be connected to a PCB ground plane using multiple vias for good thermal performance.

Block Diagram

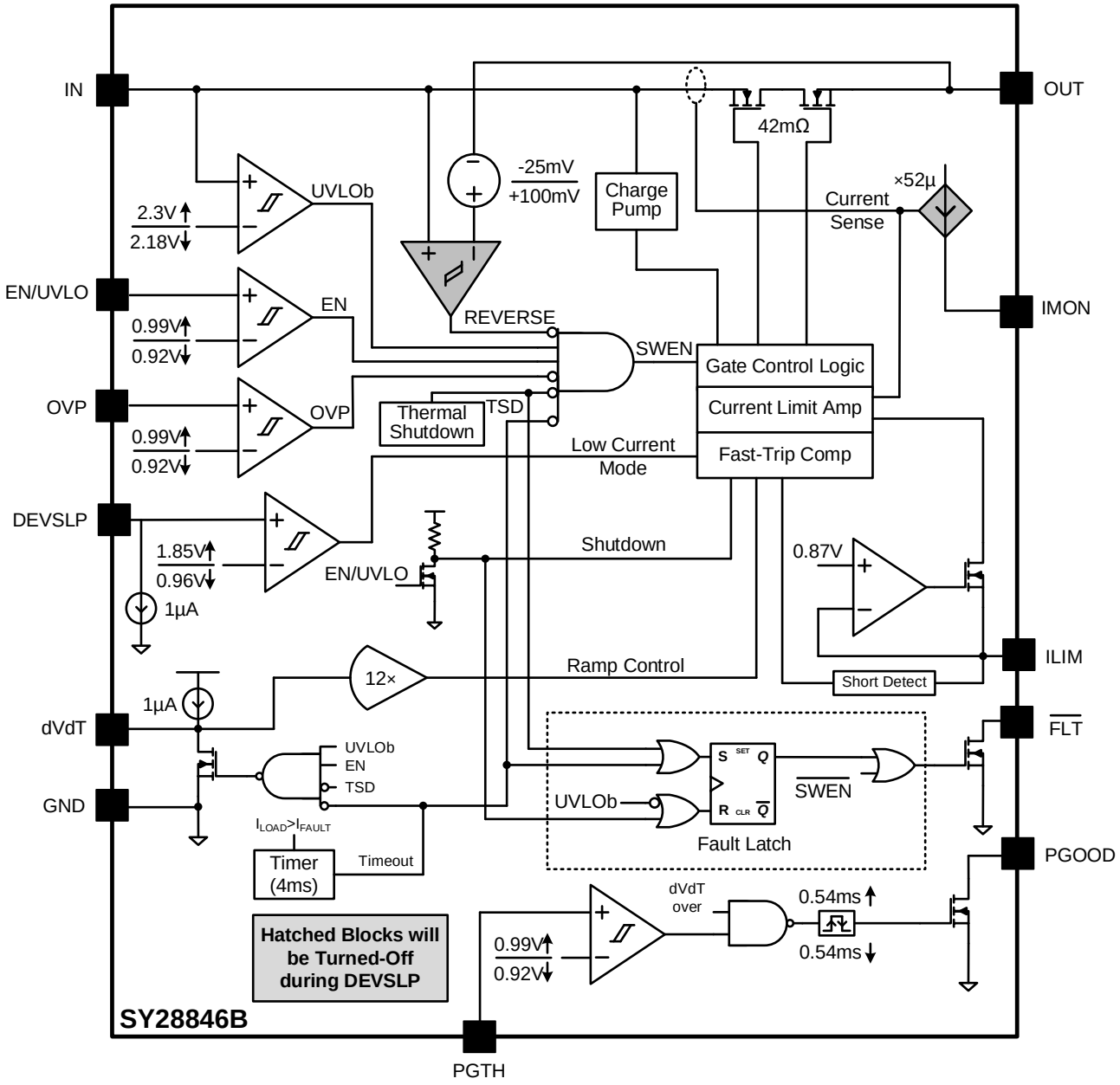


Figure 2. Block Diagram

Absolute Maximum Ratings

Parameter (Note1)	Min	Max	Unit
IN, PGTH, PGOOD, EN/UVLO, OVP, DEVSLP, /FLT	-0.3	30	V
OUT	-0.3	20	
dVdT, ILIM, IMON	-0.3	7	
PGOOD, /FLT, dVdT Sink Current		10	mA
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering,10sec.)		260	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-ambient Thermal Resistance	31.5	°C/W
θ_{JC} Junction-to-case Thermal Resistance	26	
P_D Power Dissipation T_A=25°C	3.17	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
IN	2.7	18	V
OUT, PGTH, PGOOD, EN/UVLO, OVP, DEVSLP, /FLT	0	18	
dVdT, ILIM, IMON	0	6	V
R_{ILIM}	16.9	150	kΩ
R_{IMON}	1		
C_{OUT}	0.1		μF
C_{dVdT}		470	nF
Junction Temperature	-40	125	°C
Ambient Temperature Range	-40	105	°C

Electrical Characteristics

(–40℃≤ T_J=T_A ≤ 125℃, 2.7V ≤V_{IN} =18V, $V_{EN/UVLO}$ = 2V, V_{OVP} =V_{DEVSLP} =V_{PGTH} = 0V, R_{ILIM} = 150kΩ, C_{OUT} =1μF, C_{dVdT} = OPEN, PGOOD = /FLT = IMON = OPEN. Positive current reaches terminals. All voltages referenced to GND, unless otherwise specified. The values are guaranteed by test, design or statistical correlation.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage and Internal Undervoltage Lockout						
Input Voltage Range	V_{IN}		2.7		18	V
Input UVLO Threshold	V_{UVLO}		2.2	2.3	2.4	V
UVLO Hysteresis	V_{HYS}		112	122	132	mV
Shutdown Current	I_{SHDN}	$V_{EN/UVLO}$ = 0 V, V_{IN} = 3 V	3	8.6	15	μA
		$V_{EN/UVLO}$ = 0 V, V_{IN} = 12 V	3	15	20	
		$V_{EN/UVLO}$ = 0 V, V_{IN} = 18 V	3	18.5	25	
Quiescent Current	I_Q	$V_{EN/UVLO}$ = 2 V, V_{IN} = 3 V	60	110	160	μA
		$V_{EN/UVLO}$ = 2 V, V_{IN} = 12 V	65	115	165	
		$V_{EN/UVLO}$ = 2 V, V_{IN} = 18 V	65	115	165	
DevSleep Mode Current	I_{Q_DEVSLP}	V_{DEVSLP} = 0 V, V_{IN} = 2.7V to 18V	60	100	140	μA
Enable And Under-voltage Lockout (EN/UVLO) Input						
EN/UVLO Logic High	V_{ENH}		0.97	0.99	1.01	V
EN/UVLO Logic Low	V_{ENL}		0.9	0.92	0.94	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
EN Threshold Voltage for Low I_Q Shutdown, Falling	V_{SHUTF}		0.3	0.47	0.63	V
EN Hysteresis for Low I_Q Shutdown				66		mV
EN Input Leakage Current	I_{EN}	0 V ≤ $V_{EN/UVLO}$ ≤ 18 V	-100	0	100	nA
Over Voltage Protection (OVP) Input						
Overvoltage Threshold Voltage, Rising.	V_{OVPR}		0.97	0.99	1.01	V
Overvoltage Threshold Voltage, Falling.	V_{OVPF}		0.9	0.92	0.94	V
OVP Input Leakage Current	I_{OVP}	0 V ≤ V_{OVP} ≤ 5 V	-100	0	100	nA
DEVSLP Mode Input (DEVSLP): Active High						
DEVSLP Threshold Voltage, Rising.	$V_{DEVSLPR}$		1.6	1.85	2	V
DEVSLP Threshold Voltage, Falling.	$V_{DEVSLPF}$		0.8	0.96	1.1	V
DEVSLP Input Leakage Current	I_{DEVSLP}	0.2 V ≤ V_{DEVSLP} ≤ 18 V	0.6	1	1.25	µA
Output Ramp Control (dVdT)						
dVdT Charging Current	I_{dVdT}	V_{dVdT} = 0 V	0.85	1	1.15	µA
dVdT Discharging Resistance	R_{dVdT}	$V_{EN/UVLO}$ = 0V, I_{dVdT} = 10mA sinking		16	35	Ω
dVdT to OUT Gain	G_{dVdT}	$\Delta V_{OUT}/\Delta V_{dVdT}$	11.65	11.9	12.05	V/V
dVdT Maximum Capacitor Voltage	V_{dVdT_MAX}		1.4	2.5	3.1	V
MOSFET – Power Switch						
IN to OUT - ON Resistance	$R_{DS(ON)}$	1A ≤ I_{OUT}≤ 5A, T_J = 25℃	34	42	49	mΩ
		1A ≤I_{OUT}≤ 5A, -40℃≤T_J≤85℃	26		58	
		1A ≤I_{OUT}≤ 5A, -40℃≤T_J≤125℃	26		66	
Current Limit Programming (ILIM)						
ILIM Bias Voltage	V_{ILIM}			0.87		V
Current Limit	I_{FAULT}	R_{ILIM} = 150 kΩ, (V_{IN} - V_{OUT}) = 1V	0.53	0.58	0.63	A
		R_{ILIM} = 88.7 kΩ, (V_{IN} - V_{OUT}) = 1V	0.9	0.99	1.07	
		R_{ILIM} = 42.2 kΩ, (V_{IN} - V_{OUT}) = 1V	1.92	2.08	2.25	
		R_{ILIM} = 24.9 kΩ, (V_{IN} - V_{OUT}) = 1V	3.25	3.53	3.81	
		R_{ILIM} = 20 kΩ, (V_{IN} - V_{OUT}) = 1V	4.09	4.45	4.81	
		R_{ILIM} = 16.9 kΩ, (V_{IN} - V_{OUT}) = 1V	4.78	5.2	5.62	
		R_{ILIM} = OPEN	0.35	0.45	0.55	
		R_{ILIM} = SHORT	0.55	0.67	0.8	
DevSleep Mode Current Limit	I_{FAULT_DSLP}		0.55	0.67	0.8	A
Short-Circuit Current Limit	I_{OS}	R_{ILIM} = 42.2 kΩ, V_{IN}=12V, (V_{IN} - V_{OUT}) = 5V	1.91	2.07	2.24	A
		R_{ILIM} = 24.9 kΩ, V_{IN}=12V, (V_{IN} - V_{OUT}) = 5V	3.21	3.49	3.77	
		R_{ILIM} = 16.9 kΩ, V_{IN}=12V, (V_{IN} - V_{OUT}) = 5V, -40℃≤T_J≤85℃	4.7	5.11	5.52	
Fast-Trip Comparator Threshold	$I_{FASTRIP}$		1.4 x I_{FAULT} +2			A
Current Monitor Output (IMON)						
Gain Factor I_{IMON}/I_{OUT}	G_{IMON}	1 A ≤ I_{OUT} ≤ 5 A		52.3		µA/A
Pass FET Output (OUT)						
OUT Leakage Current in Off-State	I_{LKG_OUT}	V_{IN} =18V, $V_{EN/UVLO}$ = 0V, V_{OUT} = 0V (Sourcing)	-2	0	2	µA
		V_{IN} =2.7V, $V_{EN/UVLO}$ =0V, V_{OUT} = 0V (Sinking)	3	13	20	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
V_{IN} -V_{OUT} Threshold for Reverse Protection Comparator, Falling	V_{REVTH}		-40	-25	-10	mV
V_{IN} -V_{OUT} Threshold for Reverse Protection Comparator, Rising	V_{FWDTH}		84	100	116	mV
Fault Flag (/FLT): Active Low						
/FLT Internal Pull-Down Resistance	$R_{/FLT}$	V_{OVP} = 2 V, $I_{/FLT}$ = 5 mA sinking	15	30	55	Ω
/FLT Input Leakage Current	$I_{/FLT}$	0V ≤ $I_{/FLT}$ ≤ 18V	-1	0	1	μA
/FLT Assertion Delay in Circuit Breaker Mode	$t_{CB(dly)}$	Delay from I_{OUT} > I_{FAULT} to FLT↓ (and internal FET turned off)		4		ms
Positive Input for Power-Good Comparator (PGTH)						
PGTH Threshold Voltage, Rising	V_{PGTHR}		0.97	0.99	1.01	V
PGTH Threshold Voltage, Falling	V_{PGTHF}		0.9	0.92	0.94	V
PGTH Input Leakage Current	I_{PGTH}	0 V ≤ V_{PGTH} ≤ 18 V	-100	0	100	nA
Power Good Comparator Output (PGOOD): Active High						
PGOOD Internal Pull-down Resistance	R_{PGOOD}	V_{PGTH} = 0V, I_{PGOOD} = 5 mA sinking	15	30	55	Ω
PGOOD Input Leakage Current	I_{PGOOD}	0 V ≤ V_{PGOOD} ≤ 18 V	-1	0	1	μA
Thermal Shut Down (TSD)						
TSD Threshold	T_{TSD}			160		℃
TSD Hysteresis	T_{TSDhys}			12		℃
Thermal Fault			Latch-off			
Over Voltage Protection Input (OVP)						
OVP Disable Delay	$t_{OVP(dly)}$	OVP↑ (100mV above V_{OVPR}) to /FLT↓		2		μs
Enable and UVLO Input						
EN Turn-On Delay	$t_{ON(dly)}$	EN/UVLO↑ (100mV above V_{ENR}) to V_{OUT} = 100 mV, C_{dVdT} < 0.8 nF		220		μs
		EN/UVLO↑ (100mV above V_{ENR}) to V_{OUT} = 100 mV, C_{dVdT} ≥ 0.8 nF	100 + 150 x C_{dVdT}			μs
EN Turn-Off Delay	$t_{OFF(dly)}$	EN/UVLO↓ (100mV below V_{ENF}) to /FLT↓		2		μs
Output Ramp Control (dV/dT)						
Output Ramp Time	t_{dVdT}	EN/UVLO ↑ to V_{OUT} = 4.5 V, with C_{dVdT} = open		0.2		ms
		EN/UVLO ↑ to V_{OUT} = 11 V, with C_{dVdT} = open	0.25	0.37	0.5	ms
		EN/UVLO ↑ to V_{OUT} = 11 V, with C_{dVdT} = 1nF		0.97		ms
Current Limit						
Fast-Trip Comparator Delay	$t_{FASTRIP(dly)}$	I_{OUT} > $I_{FASTRIP}$		200		ns
Reverse Protection Comparator						
Reverse Protection Comparator Delay	$t_{REV(dly)}$	(V_{IN} - V_{OUT})↓(1 mV overdrive below V_{REVTH}) to /FLT↓		10		μs
		(V_{IN} - V_{OUT})↓(10 mV overdrive below V_{REVTH}) to /FLT↓		1		μs
	$t_{FWD(dly)}$	(V_{IN} - V_{OUT})↑(10 mV overdrive below V_{REVTH}) to /FLT↑		3.1		μs
Power-Good Comparator Output (PGOOD): Active High						
PGOOD Delay (De-glitch) Time	t_{PGOODR}	Rising edge		0.54		ms
	t_{PGOODF}	Falling edge		0.54		ms

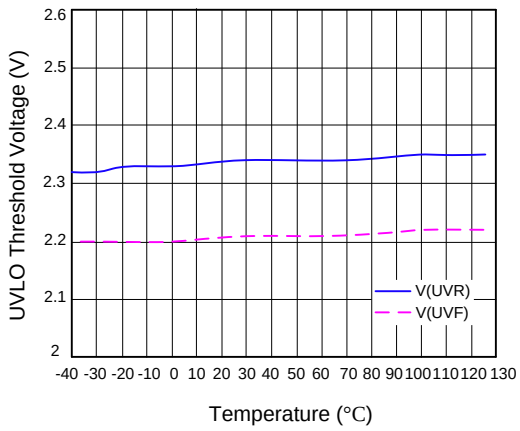
Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25℃ on a highly effective four-layer thermal conductivity test board of JESD5-2, -5, -7 thermal measurement standards.

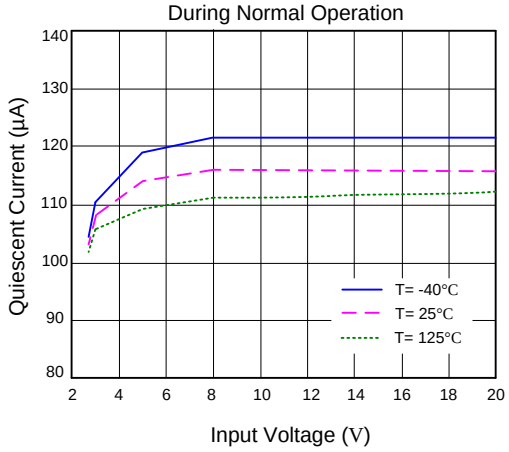
Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

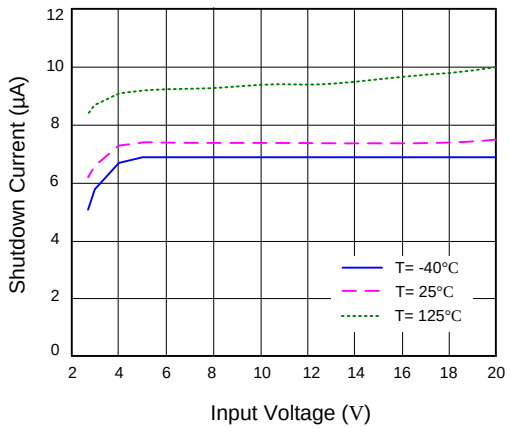
UVLO Threshold Voltage vs. Temperature



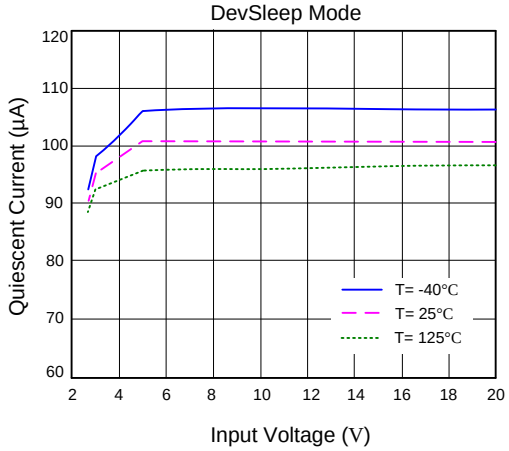
Input Supply Current vs. Supply Voltage During Normal Operation



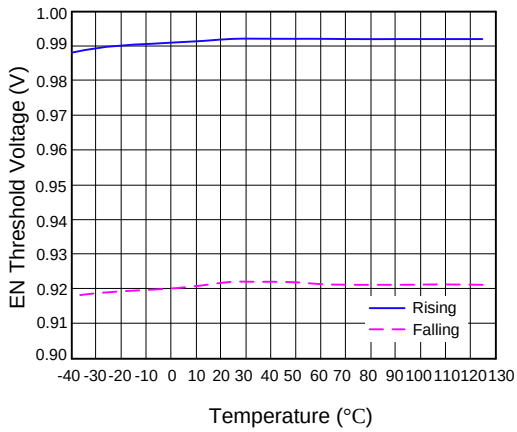
Shutdown Current vs. Input Voltage



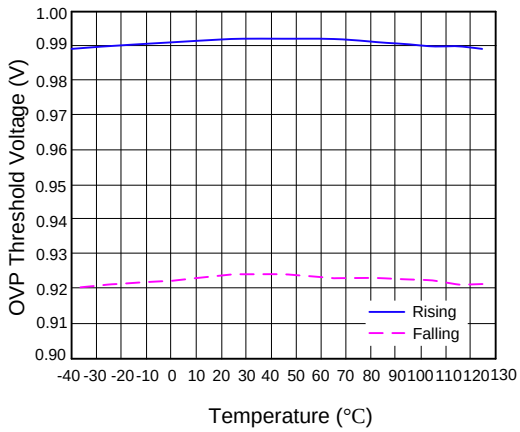
Input Supply Current vs. Supply Voltage in DevSleep Mode



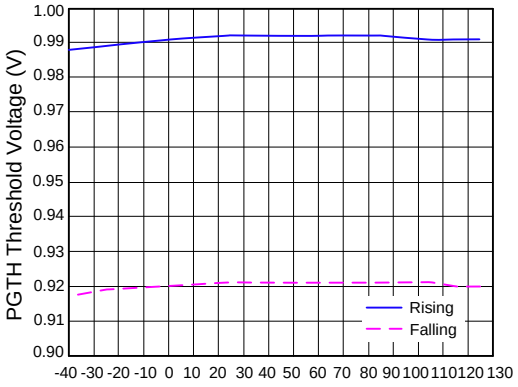
EN Threshold Voltage vs. Temperature



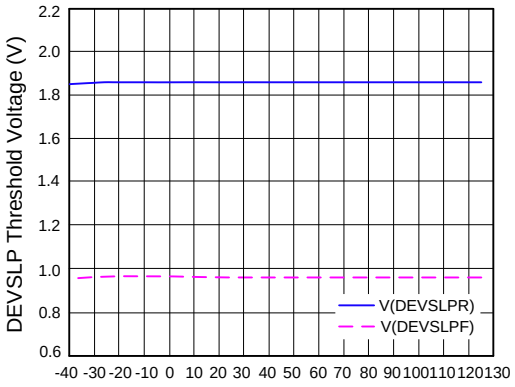
OVP Threshold Voltage vs. Temperature



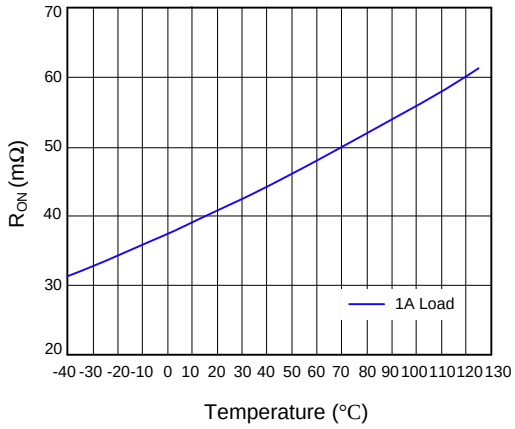
PGTH Threshold Voltage vs. Temperature



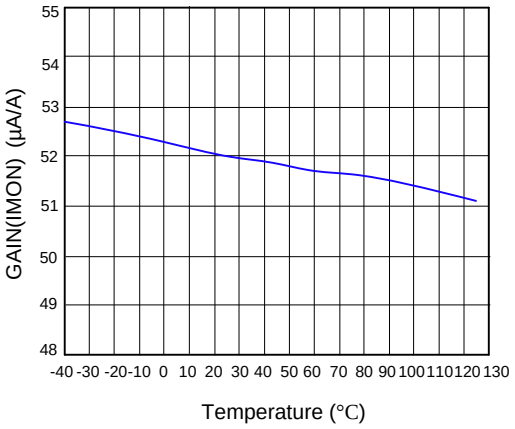
DEVSLP Threshold Voltage vs. Temperature



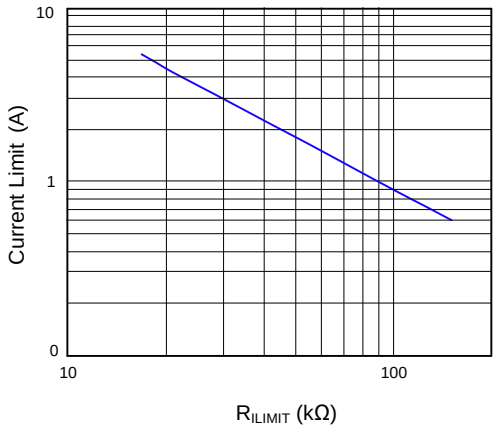
R_{ON} vs. Temperature



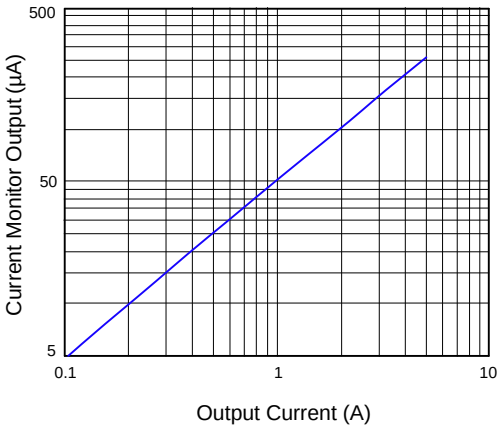
$GAIN_{(IMON)}$ vs. Temperature



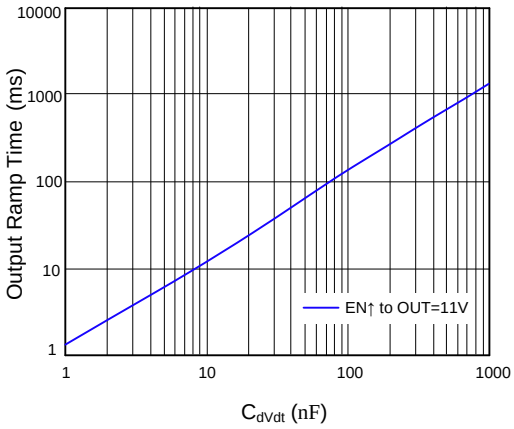
Current Limit vs. Current Limit Resistor



Current Monitor Output vs. Output Current

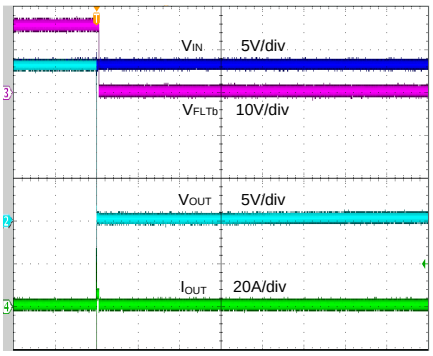


Output Ramp Time vs. C_{dVdT}



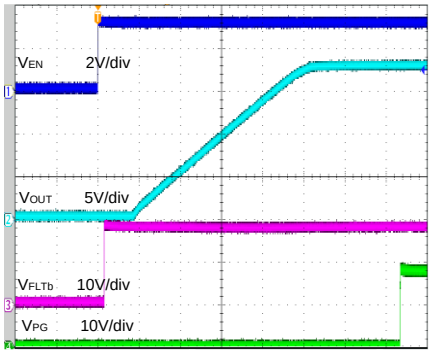
Hard-short

(V_{IN}=18V, C_{IN}=C_{OUT}=10μF, R_{ILIM}=16.9kΩ)



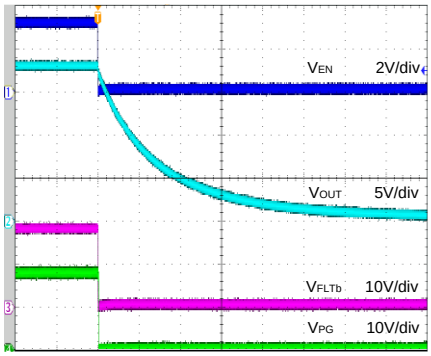
Turn ON with Enable

(V_{IN}=18V, C_{dVdT}=1nF, C_{OUT}=100μF, 6Ω Load)



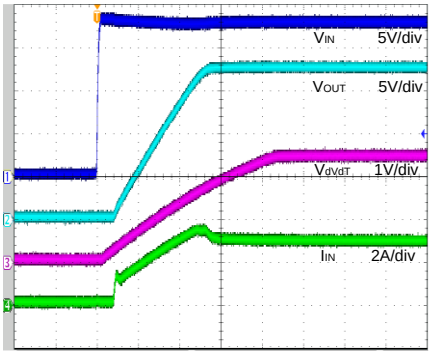
Turn OFF with Enable

(V_{IN}=18V, C_{dVdT}=1nF, C_{OUT}=100μF, 6Ω Load)



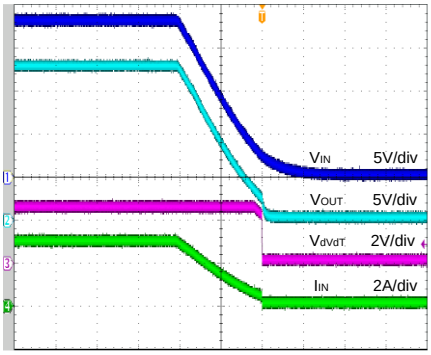
V_{IN} Startup

(V_{IN}=18V, EN ON, C_{dVdT}=1nF, C_{OUT}=100μF, 6Ω Load)



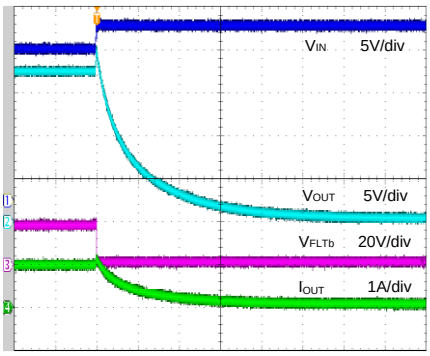
V_{IN} Shutdown

(V_{IN}=18V, EN ON, C_{dVdT}=1nF, C_{OUT}=100μF, 6Ω Load)



Over-voltage Shutdown

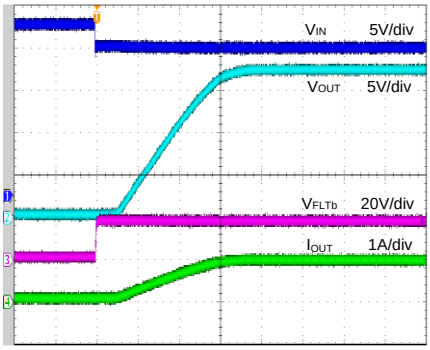
(V_{IN}=18V→20V, R_{FLTb}=100kΩ, 18Ω Load)



Time (40μs/div)

Over-voltage Recovery

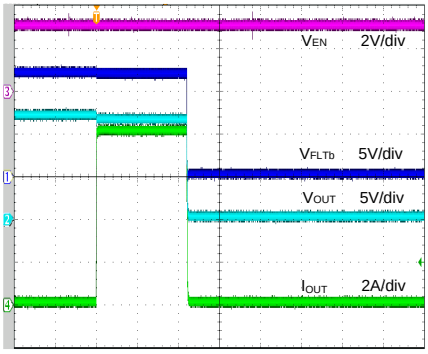
(V_{IN}=20V→18V, R_{FLTb}=100kΩ, 18Ω Load)



Time (100μs/div)

Overload Protection

(V_{IN}=12V, R_{ILIM}=16.9kΩ, Load:0Ω→1.5Ω)



Time (2ms/div)

Application Information

The SY28846B is a smart eFuse with integrated back-to-back MOSFETs and enhanced built-in protection circuitry. It is ideal for power management systems and applications powered from 2.7V to 18V.

For hot-plug applications, the device provides hot-swap power management with an in-rush current limit during a programmable soft-start. The device is equipped with a precision over-current limit used to minimize over-design of the input power supply. The device also integrates a short-circuit protection that helps protect both the part and system from a sudden high current event when a short circuit is detected. The overcurrent limit can be programmed between 0.6A and 5.3A using an external resistor.

Undervoltage Lockout and Overvoltage Set Point:

The trip points can be programmed for under-voltage and over-voltage protection using an external resistor network. Figure 3 illustrates the UVLO and OVP threshold settings. The values required are calculated by solving the following equations:

$$V_{OVPR}(V) = \frac{R_3}{R_1+R_2+R_3} \times V_{OV}$$

$$V_{ENR}(V) = \frac{R_2+R_3}{R_1+R_2+R_3} \times V_{UV}$$

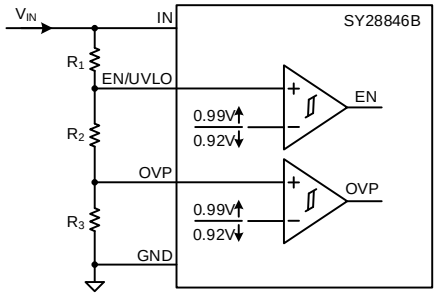


Figure 3.
UVLO and OVP Thresholds Set by R_1, R_2 and R_3

It is recommended to use larger values of resistance for R_1, R_2, and R_3 to minimize the input current drawn from the power supply.

However, this can add errors in these calculations due to leakage currents from external devices connected to the resistor string. Using a resistor string current 20× larger than the expected leakage current is recommended to improve the thresholds accuracy.

Overload Protection:

The device continuously monitors the load current and keeps it below the value programmed by R_{ILIM}. During overload events, the current limit is set to I_{LIM} (over-load current limit), as shown in the following equation:

$$I_{FAULT} = \frac{89}{R_{ILIM}}$$

Where:

- I_{FAULT} is overload current limit in Amperes.
- R_{ILIM} is the current limit resistor value, in kΩ.

The SY28846B allows the overload current to flow through the device until $I_{LOAD} < I_{FASTRIP}$. It starts the timer when $I_{FAULT} < I_{LOAD} < I_{FASTRIP}$, and once the timer exceeds $t_{CB(dly)}$, the internal FET is turned off and FLT is asserted.

If the device junction temperature reaches the thermal shutdown threshold (T_{TSD}), the internal MOSFET is turned off. Once in thermal shutdown, the SY28846B stays latched off. During thermal shutdown, the fault pin /FLT pulls low to signal a fault condition.

The SY28846B operation during overload and short circuit conditions are explained in Table 1.

Table 1. Device Operation during Overload and Short Circuit Conditions

Start-up	Inrush ramp controlled by dVdT
	Inrush limited to I_{FAULT} level as set by R_{ILIM}
	Fault Timer runs when current is limited to I_{FAULT}
	Fault timer expires after $t_{CB(dly)}$ (4ms) causing device shutoff
	Device turns off if $T_J > T_{TSD}$ before timer expires
Overcurrent response	Current is allowed through the device if $I_{LOAD} < I_{FASTRIP}$
	Fault Timer runs when current goes above I_{FAULT}
	Fault timer expires after $t_{CB(dly)}$ (4 ms) causing device shutoff
	Device turns off if $T_J > T_{TSD}$ before timer expires
Short-circuit response	Fast shut off when $I_{LOAD} > I_{FASTRIP}$
	Quick restart and current limited to I_{FAULT}, follows standard start-up

Short-Circuit Protection:

The device incorporates two distinct protection levels: a current limit (I_{LIM}) and a fast-trip threshold ($I_{FASTRIP}$). The fast trip and current limit dependence is shown in the following equation:

$$I_{FASTRIP} = 1.4 \times I_{FAULT} + 2$$

The device's current increases rapidly during a transient short circuit event. As the current-limit amplifier cannot

respond quickly to this event due to its limited bandwidth, the fast-trip circuit ensures that the device can respond to and control the current within 1 µs when detecting a short circuit event (I_{OUT} > $I_{FASTRIP}$). The fast-trip circuit holds the internal FET off for a few microseconds, after which the current limit amplifier regulates the output current to I_{LIM}. Then, the device behaves similar to an overload condition.

Current Monitoring:

The device provides a current mirror at the IMON pin proportional to the output current. A resistor R_{IMON} connected from the IMON pin to the GND is used to convert the sensed current to a voltage. The sense voltage at IMON pin is calculated from equation:

$$V_{IMON} = \left(I_{OUT} \times GAIN_{IMON} + I_{IMON_{OS}}\right) \times R_{IMON}$$

Where:

- $GAIN_{IMON}$ = Gain factor I_{IMON}/I_{OUT} = 52 µA/A
- I_{OUT} = Load current
- I_{IMON_OS} = 0.8 µA (typ)

This can be connected to a downstream ADC for system health monitoring. The R_{IMON} needs to be configured based on the maximum input voltage range of the ADC used. R_{IMON} is set using:

$$R_{IMON} = \frac{V_{IMONmax}}{I_{LIM} \times 52 \times 10^{-6}} k\Omega$$

If the IMON pin voltage is not digitized with an ADC, RIMON can be selected to produce a 1V/1A voltage at the IMON pin by selecting a resistor value of 20 kΩ (1% tolerance is recommended).

This pin should not have a bypass capacitor to avoid delay in the current monitoring information.

IN, OUT, and GND Pins:

The device has multiple input (IN) and output (OUT) pins.

All the IN pins should be connected together and to the power source. C_{IN} is a bypass capacitor that helps control transient voltages, limit emissions, and local power supply noise. Where acceptable, a value in the range of 0.1µF to 10µF is recommended for C_{IN}. The recommended operating voltage range has to be 20% higher than the maximum expected voltage.

The GND terminal is the most negative voltage in the circuit and is used as a reference unless otherwise specified.

Device Operation Modes:

The SY28846B features a dedicated DevSleep interface pin (DEVSLP) to control the device and help it enter low-power mode. The DEVSLP pin is compatible with standard hardware signals asserted from the host controller. When the DEVSLP pin is pulled high, the device starts operating in low-power DevSleep mode. During this mode, the quiescent current is decreased to less than 140µA (100µA typical), the output voltage remains active, the current limit is set to $I_{DEVSLP(LIM)}$, and the reverse blocking comparator and the current monitor are disabled. All other protections remain active to ensure the system's safety even in DevSleep mode.

Hot Plug-in and In-Rush Current Control:

The device has a controlled output slew rate, providing soft-start functionality. This limits the inrush current caused by the output capacitor(s) charging and enables these devices to be used in hot-swap applications. The slew rate can be decreased with an external capacitor added between the dVdT pin and the ground (as shown in Figure 4). With an external capacitor present, the slew rate can be determined by the following equation:

$$I_{dVdT} = \left(\frac{C_{dVdT}}{GAIN_{dVdT}}\right) \times \left(\frac{dV_{OUT}}{dt}\right)$$

Where:

- I_{dVdT} = 1µA (typ)
- $\frac{dV_{OUT}}{dt}$ Desired output slew rate
- $GAIN_{dVdT}$= dVdT to OUT gain = 12

The total ramp time (t_{dVdT}) of V_{OUT} for 0 to V_{IN} can be calculated using equation:

$$t_{dVdT} = 8.3 \times 10^{4} \times V_{IN} \times C_{dVdT}$$

The dVdT pin can be left floating if the slew rate is not decreased. When left floating, the device uses the default value of 48V/ms for the output slew rate.

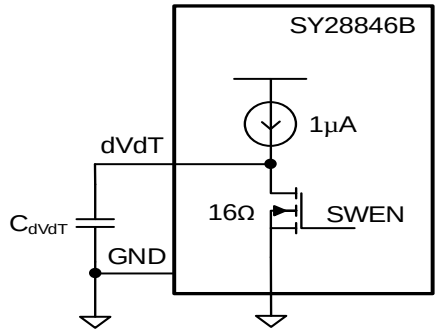


Figure 4.
Output Ramp Up Time t_{dVdT} is Set by C_{dVdT}

FAULT Response:

The /FLT pin asserts (active low) when one of the following fault conditions are detected: under-voltage, over-voltage, reverse block, and thermal shutdown. The /FLT signal remains asserted until the fault conditions are addressed and the device resumes regular operation. An internal "deglitch" circuit for under-voltage and over-voltage (2.2µs typical) filters unexpected false faults during transients on the input bus. Using this pin requires an external pull-up resistor to an external voltage rail. If the /FLT reporting feature is not used in the application, the /FLT pin may be left open or tied to the ground. VIN falling below VUVF = 2.1 V resets the /FLT pin status.

Power Good Comparator:

The power-good (PGOOD) output can indicate whether the output voltage is above a user-defined threshold and can, therefore, be considered within the acceptable range by downstream DC-DC converters or system monitoring circuits. A resistor divider connected to the PGTH pin sets an accurate power-good threshold for the output voltage. The PGOOD pin is an open-drain output that is high-impedance when the voltage at the PGTH pin is higher than 0.99 V.

The PGOOD signal has a deglitch time incorporated to ensure that internal MOSFET is fully biased before downstream converters apply heavy load. Controlling the de-glitch delay can be done by using the equation:

$t_{PGOOD(degl)}$ = Maximum {(3.5 × 10^6 × C_{dVdT}), t_{PGOODR}}

The pin requires an external pull-up resistor to the input or output voltage rails. If the PGOOD reporting feature is not used, PGOOD may be left open or tied to the ground.

Thermal Shutdown:

The device has built-in overtemperature shutdown circuitry designed to disable the internal MOSFET if the junction temperature exceeds 160°C (typical). The protection circuit latches off the internal MOSFET. During thermal shutdown, the fault pin /FLT pulls low to signal a fault condition.

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PCB Layout Guide:

1. A 0.1µF or greater ceramic decoupling capacitor is recommended for all applications between the IN terminal and the GND. For hot-plug applications, where input power path inductance is negligible, this capacitor can be eliminated or its value reduced.

2. The optimum placement of the decoupling capacitor is closest to the IN and GND terminals of the device. Care must be taken to minimize the loop area formed by the bypass-capacitor connection and the IN/GND pins of the device.

3. Place all external components: R_{ILIM}, C_{dVdT}, R_{IMON}, and resistors for UVLO and OVP, close to their connection pins. Connect the components to the SGND with the shortest trace length to reduce parasitic effects.

4. The trace routing for the R_{ILIM} and R_{IMON} components to the device should be as short as possible to reduce parasitic effects on the current limit and current monitoring accuracy. These traces should not have any coupling to switching signals on the board.

5. Connect the SGND plane to the PGND (main power ground) at a single point, near the input capacitor negative terminal.

6. Protection devices such as TVS, snubbers, capacitors, or diodes should be placed physically close to the device they intend to protect and routed with short traces to reduce the parasitic inductance. For example, a Schottky diode placed across the output can be used to absorb negative transient voltages.

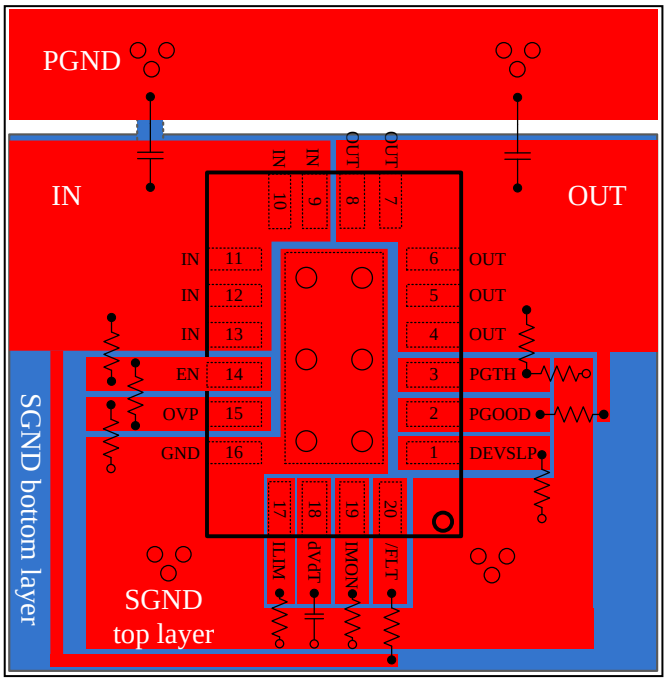
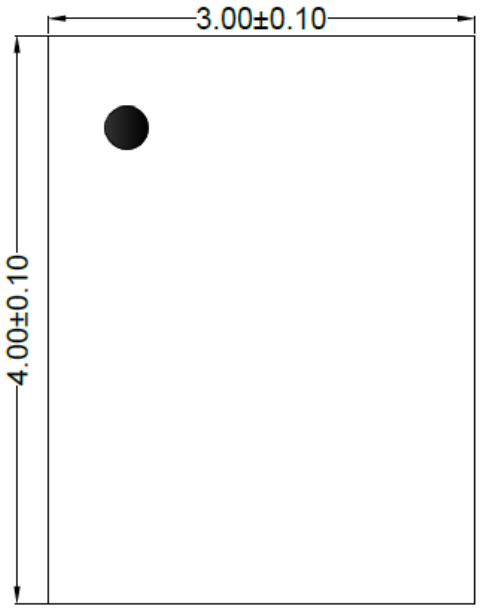
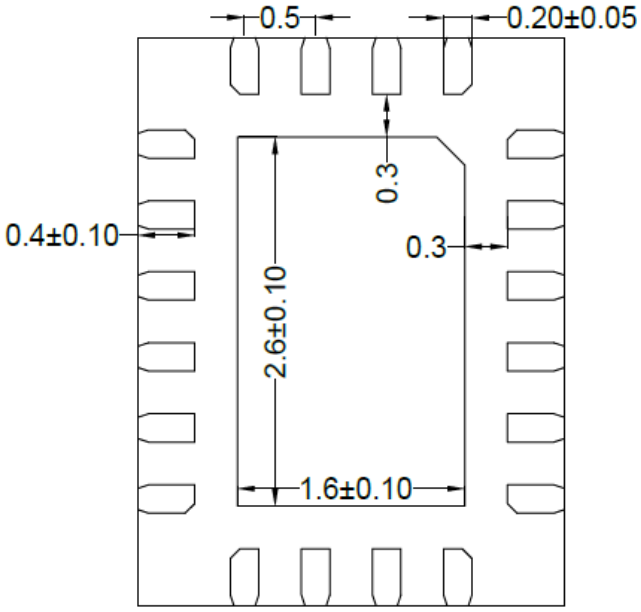


Figure 5. PCB Layout Example

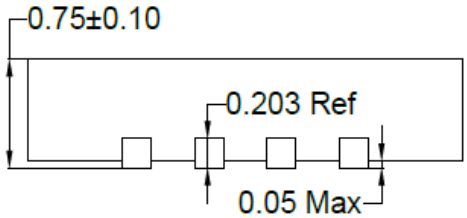
QFN3×4-20 Package Outline Drawing



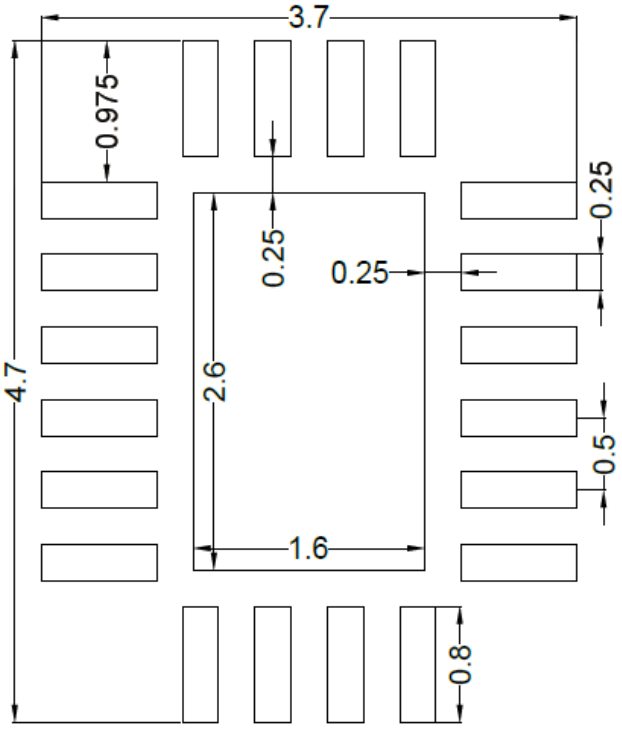
Top View



Bottom View



Side View

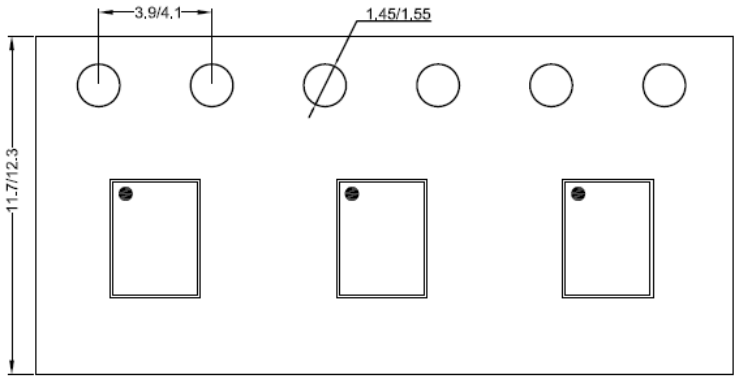


Recommended PCB Layout
(Reference Only)

Note: All dimensions are in millimeters and exclude mold flash and metal burr.

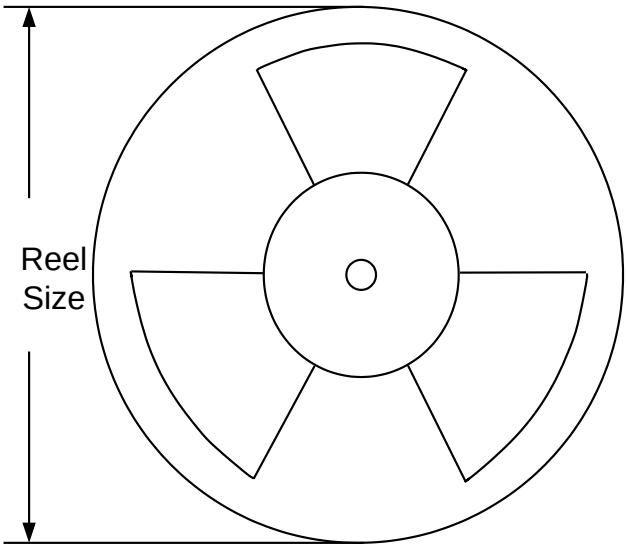
Taping & Reel Specification

1. QFN3x4 Taping Orientation



Feeding direction →

2. Carrier Tape & Reel Specification for Packages



Package types	Tape width (mm)	Pocket pitch (mm)	Reel size (Inch)	Trailer length (mm)	Leader length (mm)	Qty per reel
QFN3×4	12	8	13"	400	400	5000

3. Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Dec.07, 2023	Revision 1.0	Language improvements for clarity.
Feb.14, 2022	Revision 0.9	Initial Release

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