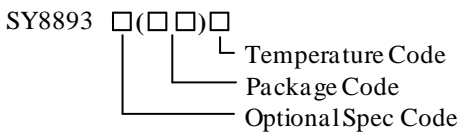


General Description

The SY8893E is a high efficiency 1.2MHz synchronous step down DC/DC regulator, which is capable of delivering up to 3A output currents. It can operate over a wide input voltage range from 2.5V to 5.5V and integrate main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

The SY8893E is in a space saving, low profile SOT563 package.

Ordering Information



Ordering Number	Package type	Note
SY8893EARC	SOT563	--

Features

- 2.5V to 5.5V Input Voltage Range
- Low $R_{DS(ON)}$ for Internal Switches (Top/Bottom) 100m Ω /60m Ω
- High Switching Frequency 1.2MHz Minimizes the External Components
- Internal Soft-start Limits the Inrush Current
- Forced PWM Operation
- 100% Dropout Operation
- Power Good Indicator
- Hic-cup for Short Circuit Protection
- Output Auto Discharge Function
- RoHS Compliant and Halogen Free
- Compact Package: SOT563

Applications

- Set Top Box
- USB Dongle
- Media Player
- Smart phone

Typical Applications

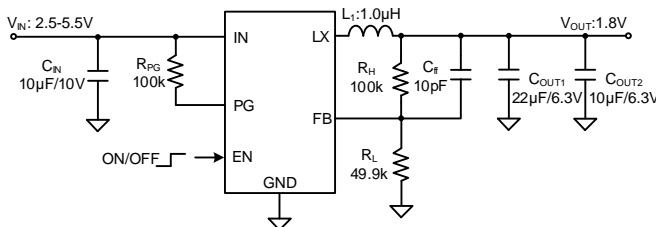


Figure1. Schematic Diagram

Inductor and C_{OUT} Selection Table

V_{OUT} [V]	L [μ H]	C_{OUT} [μ F]			
		10	22	32	44
1.2	0.47		√	☆	√
	1.0			√	√
1.8	1.0		√	☆	√
	1.5			√	√
3.3	1.0		√	☆	√
	1.5		√	√	√

Note: '☆' means recommended for most applications.

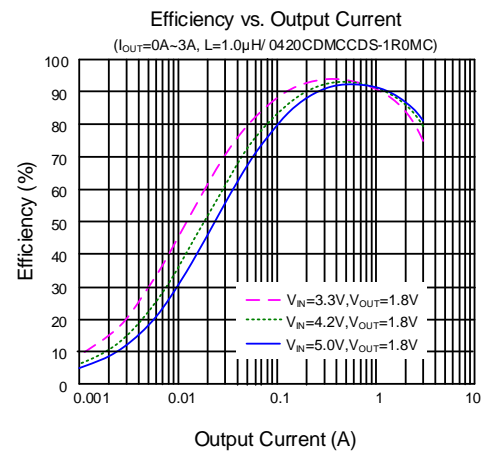
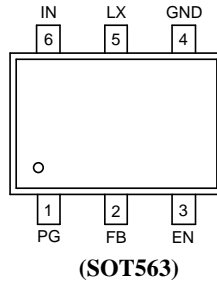


Figure2. Efficiency vs. Output Current

Pinout (Top View)



Top Mark: C4xyz (device code: C4, x=year code, y=week code, z=lot number code)

Pin Name	Pin Number	Pin Description
PG	1	Power good indicator (open drain output). Low if the output < 90% or the output >120% of regulation voltage; High otherwise. Connect a pull-up resistor to the input.
FB	2	Output Feedback Pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{OUT}=0.6 \times (1+R_H/R_L)$.
EN	3	Enable control. Pull high to turn on. Do not leave it floating.
GND	4	Ground pin.
LX	5	Inductor pin. Connect this pin to the switching node of inductor.
IN	6	Input pin. Decouple this pin to the GND pin with at least a 10μF ceramic capacitor.

Block Diagram

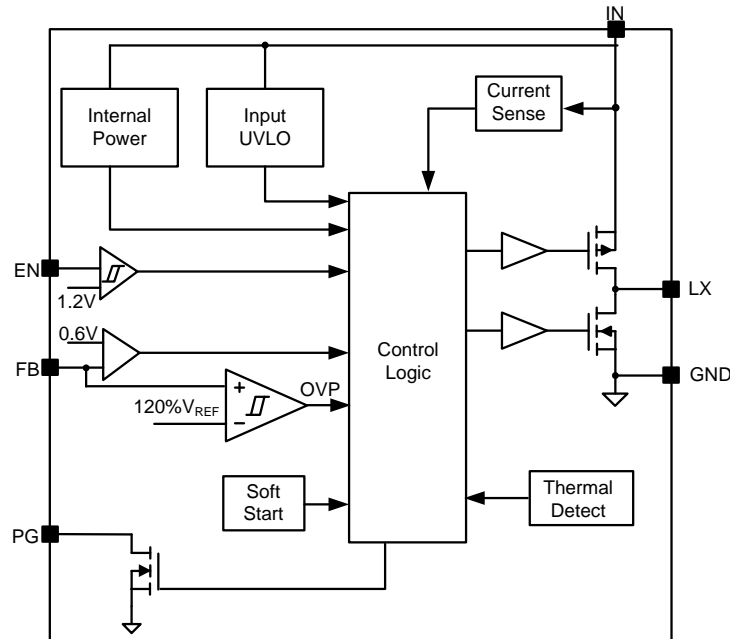


Figure3. Block Diagram



Absolute Maximum Ratings (Note 1)

Supply Input Voltage	-0.3V to 6.0V
PG, FB, EN Voltage	-0.3V to $V_{IN}+0.6V$
LX Voltage	-0.3V ^(*1) to 6.0V ^(*2) ^(*3)
Power Dissipation, P_D @ $T_A = 25^\circ C$	1.4W
Package Thermal Resistance (Note 2)	
θ_{JA}	70°C/W
θ_{JC}	8°C/W
Junction Temperature Range	-40°C to 150°C
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temperature Range	-65°C to 150°C
(*1) LX Voltage Tested Down to -3V<40ns	
(*2) LX Voltage Tested Up to +7V<40ns	
(*3) LX Voltage Tested Up to +7.8V<3ns	

Recommended Operating Conditions (Note 3)

Supply Input Voltage	2.5V to 5.5V
Junction Temperature Range	-40°C to 125°C
Ambient Temperature Range	-40°C to 85°C

Electrical Characteristics

($V_{IN} = 5V$, $V_{OUT} = 1.8V$, $L = 1.0\mu H$, $C_{OUT} = 32\mu F$, $T_A = 25^\circ C$, unless otherwise specified)

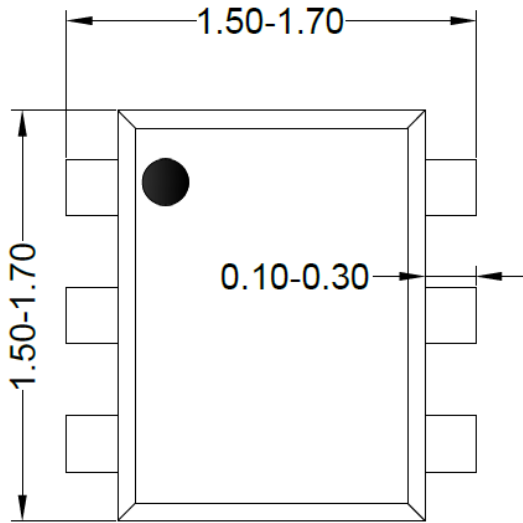
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.5		5.5	V
Input UVLO Threshold	V_{UVLO}				2.5	V
Input UVLO Hysteresis	V_{HYS}			0.15		V
Shutdown Current	I_{SHDN}	$V_{EN}=0V$		0.1	1	μA
Feedback Reference Voltage	V_{REF}	$I_{OUT}=0A$, CCM	591	600	609	mV
LX Node Discharge Resistance	R_{DIS}			50		Ω
Top FET R_{ON}	$R_{DS(ON)1}$			100		m Ω
Bottom FET R_{ON}	$R_{DS(ON)2}$			60		m Ω
EN Input Voltage High	$V_{EN,H}$		1.2			V
EN Input Voltage Low	$V_{EN,L}$				0.4	V
PG Threshold for Under Voltage Detection	$V_{PG,UVP}$			90		% V_{REF}
PG Low Delay Time for Under Voltage Detection	$t_{UVP,DLY}$			20		μs
PG Threshold for Over Voltage Detection	$V_{PG,OVP}$			120		% V_{REF}
PG Low Delay Time for Over Voltage Detection	$t_{OVP,DLY}$			20		μs
Min ON Time	$t_{ON,MIN}$			60		ns
Maximum Duty Cycle	D_{MAX}		100			%
Turn On Delay Time	$t_{ON,DLY}$	from EN high to LX start switching		300		μs
Soft-start Time	t_{SS}			700		μs
Switching Frequency	f_{SW}	$I_{OUT}=0A$, CCM		1.2		MHz
Top FET Current Limit	$I_{LMT, TOP}$		4			A
Bottom FET Reverse Current Limit	$I_{LMT, RVS}$		0.8		1.25	A
Output Under Voltage Protection Threshold	V_{UVP}			50		% V_{REF}
Output UVP Delay	$t_{UVP,DLY}$			5		μs
UVP Hic-cup ON Time	$t_{UVP, ON}$			1.25		ms
UVP Hic-cup OFF Time	$t_{UVP, OFF}$			1.25		ms
Thermal Shutdown Temperature	T_{SD}			160		$^\circ C$
Thermal Shutdown Hysteresis	T_{HYS}			20		$^\circ C$

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

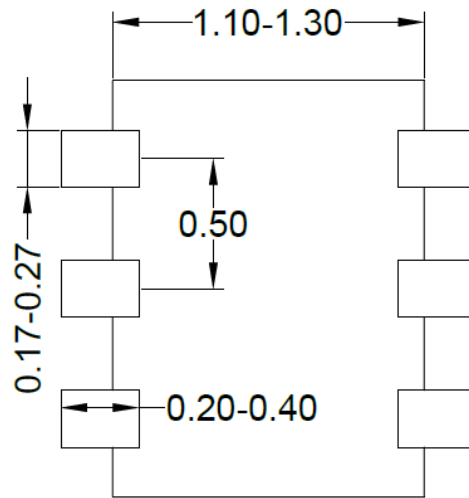
Note 2: θ_{JA} is measured in the natural convection at $T_A = 25^\circ C$ on 2OZ four-layer Silergy evaluation board. Pin 5 of case position for SY8893EARC θ_{JC} measurement.

Note 3: The device is not guaranteed to function outside its operating conditions.

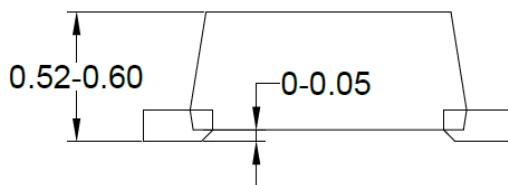
SOT563 Package Outline Drawing



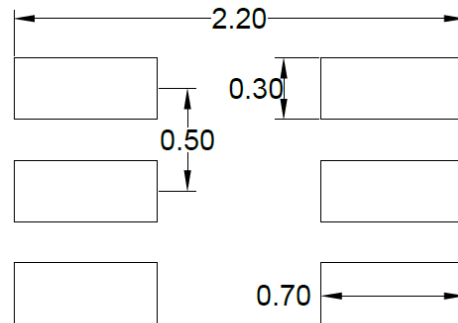
Top view



Bottom view



Side View



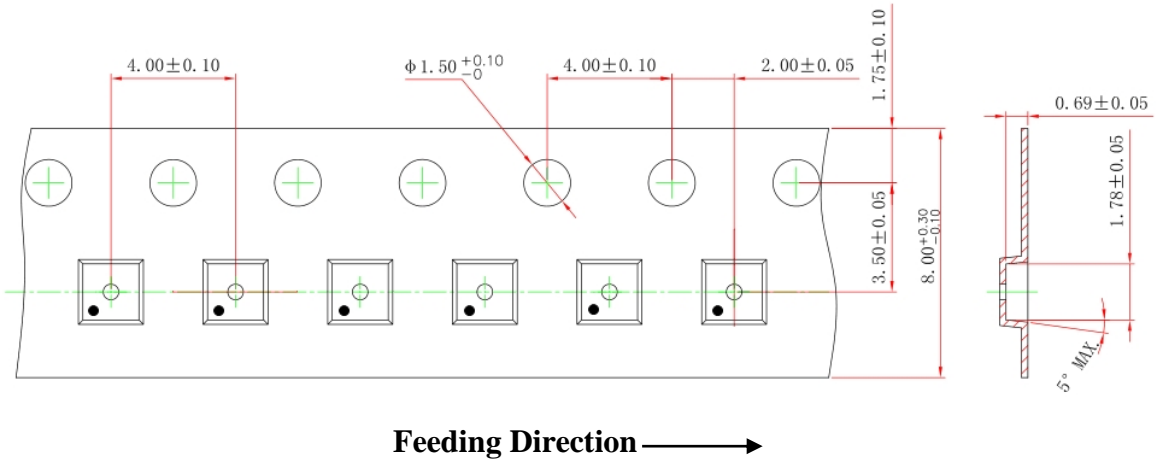
**Recommended PCB layout
(Reference only)**

Notes: All dimension in millimeter and exclude mold flash & metal burr.

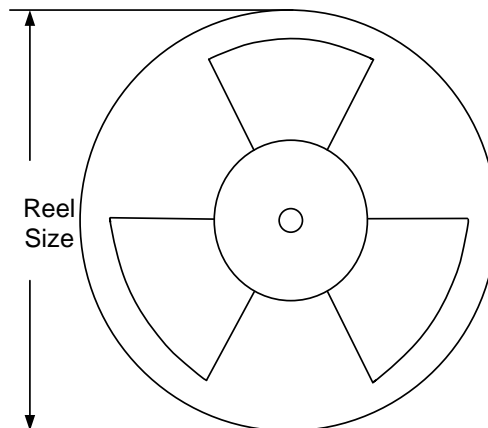
Taping & Reel Specification

1. Taping Orientation

SOT563



2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
SOT563	8	4	7"	280	160	5000

3. Others: NA