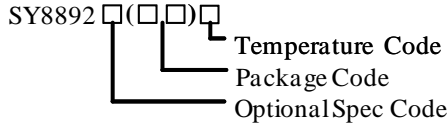


### General Description

The SY8892 is a high efficiency 1.5MHz synchronous step down DC/DC regulator, capable of delivering up to 2A output currents. It can operate over a wide input voltage range from 2.5V to 5.5V and integrates main switch and synchronous switch with very low  $R_{DS(ON)}$  to minimize the conduction loss.

The SY8892 is in a space saving, low profile SOT563 package.

### Ordering Information



Ordering Number	Package type	Note
SY8892ARC	SOT563	--

### Features

- 2.5V to 5.5V Input Voltage Range
- 55  $\mu$ A Low Quiescent Current
- Low  $R_{DS(ON)}$  for Internal Switches (Top/Bottom): 125m $\Omega$  /75m $\Omega$
- High Switching Frequency 1.5MHz Minimizes the External Components
- Internal Soft-start Limits the Inrush Current
- 100% Dropout Operation
- Power Good Indicator
- Hic-cup for Short Circuit Protection
- Output Auto Discharge Function
- RoHS Compliant and Halogen Free
- Compact Package: SOT563

### Applications

- Set Top Box
- USB Dongle
- Media Player
- Smart Phone

### Typical Application

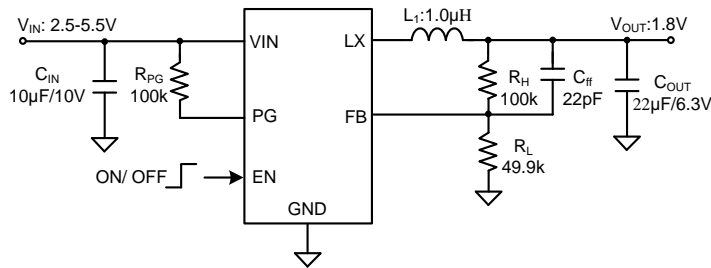


Figure1. Schematic Diagram

Inductor and  $C_{OUT}$  Selection Table

$V_{OUT}$ [V]	L [ $\mu$ H]	$C_{OUT}$ [ $\mu$ F]			
		4.7	10	22	22x2
1.2	1.0			☆	√
	1.5			√	√
	2.2			√	√
1.8/3.3	1.0		√	☆	√
	1.5		√	√	√
	2.2		√	√	√

Note: '☆' means recommended for most applications.

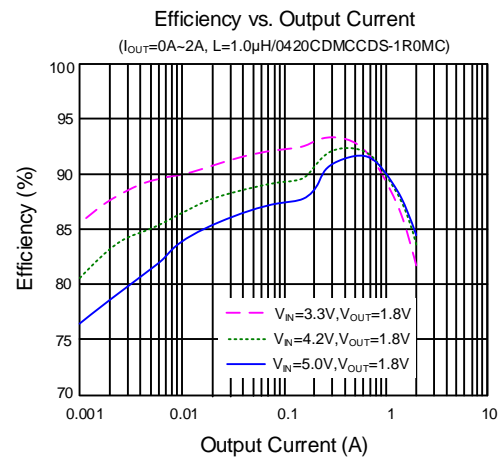
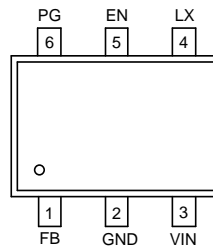


Figure2. Efficiency vs. Output Current

**Pin Out (Top View)**



**Top Mark: M4xyz** (device code: M4, x=year code, y=week code, z=lot number code)

**Pin Description**

Pin Name	Pin Number	Pin Description
FB	1	Output feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{OUT}=0.6 \times (1+R_H/R_L)$ .
GND	2	Ground pin.
VIN	3	Input pin. Decouple this pin to the GND pin with at least a 10µF ceramic capacitor.
LX	4	Inductor pin. Connect this pin to the switching node of the inductor.
EN	5	Enable control. Pull high to turn on. Do not leave it floating.
PG	6	Power good indicator. Power good indicator (open drain output). Low if the output < 90% or the output >120% of regulation voltage; High otherwise. Connect a pull-up resistor to the input.

**Function Block**

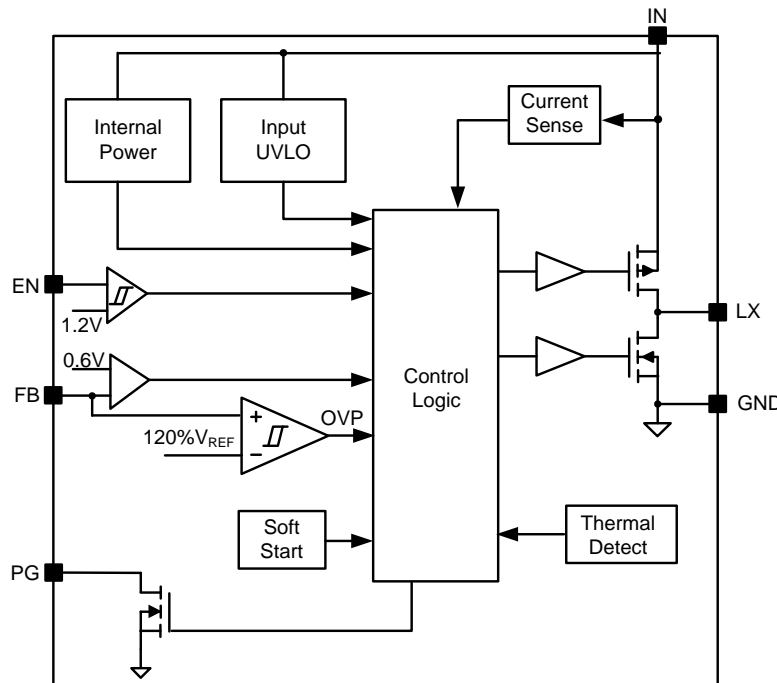


Figure3. Block Diagram



**Absolute Maximum Ratings** (Note 1)

Supply Input Voltage-----	-0.3V to 6.0V
FB, EN, PG Voltage-----	-0.3V to $V_{IN} + 0.6V$
LX Voltage-----	-0.3V <sup>(*1)</sup> to 6.0V <sup>(*2)</sup>
Power Dissipation, $P_D$ @ $T_A = 25\text{ }^\circ\text{C}$ -----	1.11W
Package Thermal Resistance (Note 2)	
$\theta_{JA}$ -----	90 $^\circ\text{C/W}$
$\theta_{JC}$ -----	20 $^\circ\text{C/W}$
Junction Temperature Range -----	-40 $^\circ\text{C}$ to 150 $^\circ\text{C}$
Lead Temperature (Soldering, 10 sec.) -----	260 $^\circ\text{C}$
Storage Temperature Range -----	-65 $^\circ\text{C}$ to 150 $^\circ\text{C}$
<sup>(*1)</sup> LX Voltage Tested Down to -3V <20ns	
<sup>(*2)</sup> LX Voltage Tested Up to +7V <20ns	

**Recommended Operating Conditions** (Note 3)

Supply Input Voltage -----	2.5V to 5.5V
Junction Temperature Range -----	-40 $^\circ\text{C}$ to 125 $^\circ\text{C}$
Ambient Temperature Range -----	-40 $^\circ\text{C}$ to 85 $^\circ\text{C}$

**Electrical Characteristics**(V<sub>IN</sub> = 5V, V<sub>OUT</sub> = 1.8V, L = 1.0μH, C<sub>OUT</sub> = 22μF, T<sub>A</sub> = 25 °C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V <sub>IN</sub>		2.5		5.5	V
Input UVLO Threshold	V <sub>UVLO</sub>			2.45	2.5	V
Input UVLO Hysteresis	V <sub>YST</sub>			150		mV
Shutdown Current	I <sub>SHDN</sub>	V <sub>EN</sub> =0V		0.1	1	μA
Quiescent Current	I <sub>Q</sub>	V <sub>FB</sub> =V <sub>REF</sub> ×105%		55		μA
Feedback Reference Voltage	V <sub>REF</sub>	I <sub>OUT</sub> =1A, CCM	0.591	0.6	0.609	V
LX Node Discharge Resistance	R <sub>DIS</sub>			50		Ω
Top FET R <sub>ON</sub>	R <sub>DS(ON)1</sub>			125		mΩ
Bottom FET R <sub>ON</sub>	R <sub>DS(ON)2</sub>			75		mΩ
EN Input Voltage High	V <sub>EN,H</sub>		1.2			V
EN Input Voltage Low	V <sub>EN,L</sub>				0.4	V
PG Threshold for Under Voltage Detection	V <sub>PG,UVP</sub>			90		%
PG Low Delay Time for Under Voltage Detection	t <sub>UVP,DLY</sub>			15		μs
PG Threshold for Over Voltage Detection	V <sub>PG,OV</sub>			120		%
PG Low Delay Time for Over Voltage Detection	t <sub>OV,DLY</sub>			15		μs
Min ON Time	t <sub>ON,MIN</sub>			50		ns
Maximum Duty Cycle	D <sub>MAX</sub>		100			%
Turn On Delay Time	t <sub>ON,DLY</sub>	from EN high to LX start switching		0.25		ms
Soft-start Time	t <sub>SS</sub>	V <sub>OUT</sub> from 0% to 100%		0.75		ms
Switching Frequency	f <sub>SW</sub>	I <sub>OUT</sub> =1A, CCM		1.5		MHz
Top FET Current Limit	I <sub>LMT, TOP</sub>		3			A
Output Under Voltage Protection Threshold	V <sub>UVP</sub>			50		% V <sub>REF</sub>
Output UVP Delay	t <sub>UVP,DLY</sub>			10		μs
UVP Hiccup ON Time	t <sub>UVP,ON</sub>			1.45		ms
UVP Hiccup OFF Time	t <sub>UVP,OFF</sub>			1.45		ms
Thermal Shutdown Temperature	T <sub>SD</sub>			160		°C
Thermal Shutdown Hysteresis	T <sub>HYS</sub>			20		°C

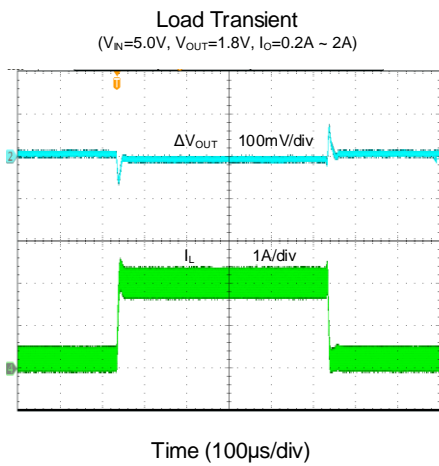
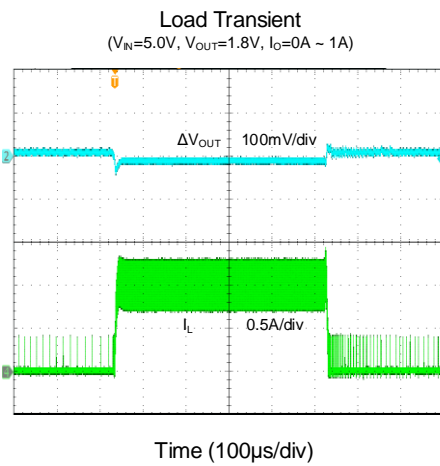
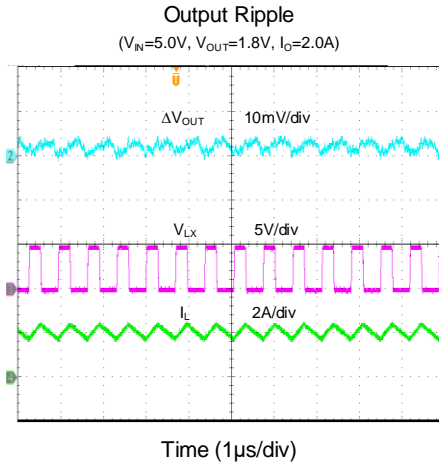
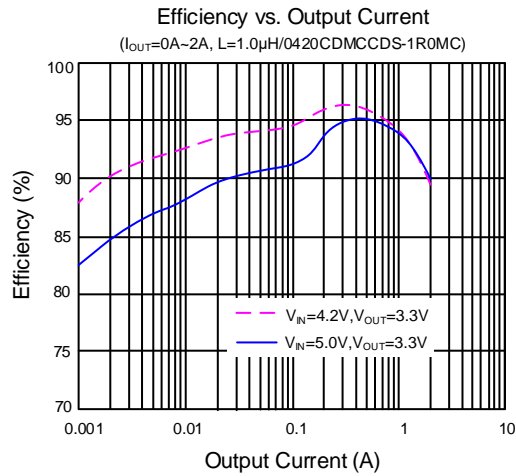
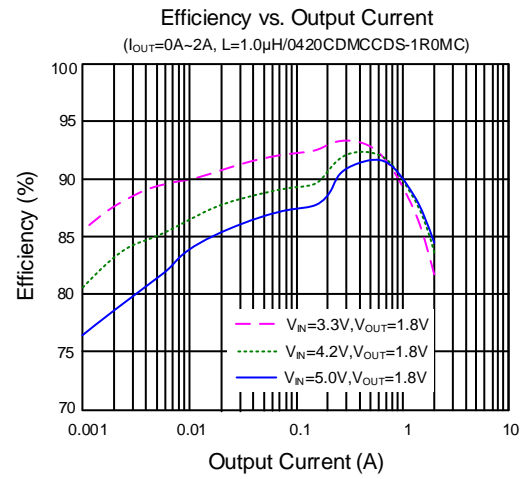
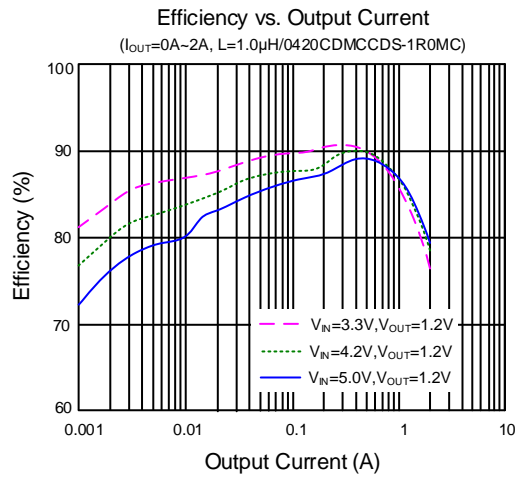
**Note 1:** Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note2:**  $\theta_{JA}$  of SY8892ARC is measured in the natural convection at T<sub>A</sub> = 25 °C on 20Z two-layer Silergy evaluation board. Pin 4 is the case position for SY8892ARC  $\theta_{JC}$  measurement.

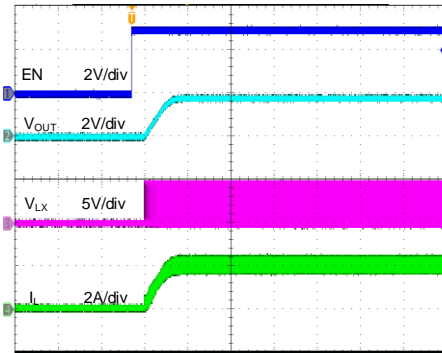
**Note 3:** The device is not guaranteed to function outside its operating conditions.

## Typical Performance Characteristics

( $T_A = 25^\circ\text{C}$ ,  $V_{IN} = 5\text{V}$ ,  $V_{OUT} = 1.8\text{V}$ ,  $L = 1.0\mu\text{H}$ ,  $C_{OUT} = 22\mu\text{F}$ , unless otherwise noted)

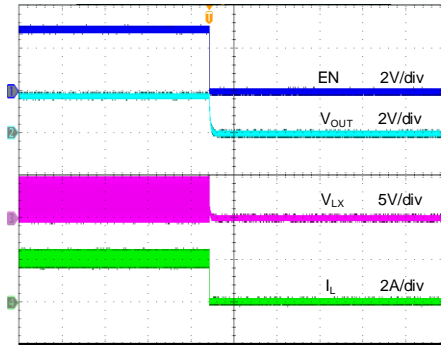


**Startup from Enable**  
 ( $V_{IN}=5.0V$ ,  $V_{OUT}=1.8V$ ,  $R_{LOAD}=0.9\Omega$ )



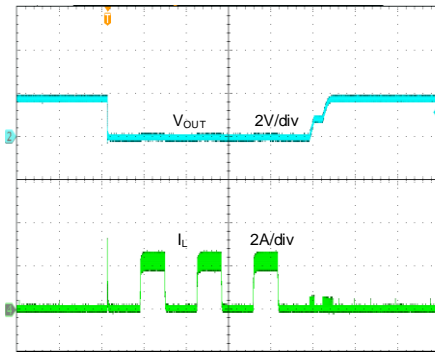
Time (800µs/div)

**Shutdown from Enable**  
 ( $V_{IN}=5.0V$ ,  $V_{OUT}=1.8V$ ,  $R_{LOAD}=0.9\Omega$ )



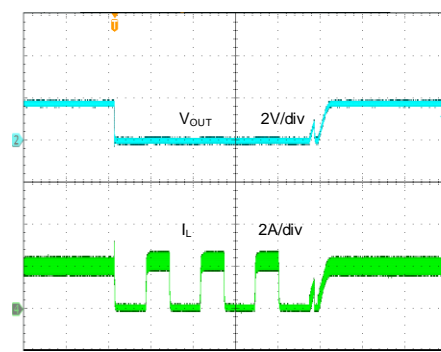
Time (800µs/div)

**Short Circuit Protection**  
 ( $V_{IN}=5.0V$ ,  $V_{OUT}=1.8V$ ,  $I_O=0A \sim$  Short)



Time (2ms/div)

**Short Circuit Protection**  
 ( $V_{IN}=5.0V$ ,  $V_{OUT}=1.8V$ ,  $I_O=2A \sim$  Short)



Time (2ms/div)

## Operation

The SY8892 is a high efficiency 1.5MHz synchronous step down DC/DC regulator, which is capable of delivering up to 2A output currents. It can operate over a wide input voltage range from 2.5V to 5.5V and integrates main switch and synchronous switch with very low  $R_{DS(ON)}$  to minimize the conduction loss.

The SY8892 is in a space saving, low profile SOT563 package.

## Applications Information

Because of the high integration in the SY8892, the application circuit based on this regulator is rather simple. Only the input capacitor  $C_{IN}$ , the output capacitor  $C_{OUT}$ , the output inductor  $L$  and the feedback resistors ( $R_H$  and  $R_L$ ) need to be selected for the targeted application specifications.

### Feedback Resistor Dividers $R_H$ and $R_L$

Choose  $R_H$  and  $R_L$  to program the proper output voltage. A value of between  $1k\Omega$  and  $1M\Omega$  is recommended for both resistors. If  $R_L = 120k\Omega$  is chosen, then  $R_H$  can be calculated to be:

$$R_H = \frac{(V_{OUT} - 0.6V) \times R_L}{0.6V}$$

### Input Capacitor $C_{IN}$

A typical X5R or better grade ceramic capacitor with 10V rating and greater than  $10\mu F$  capacitance is recommended. To minimize the potential noise problem, this ceramic capacitor should be placed really close to the IN and GND pins. Care should be taken to minimize the loop area formed by  $C_{IN}$  and the IN/GND pins.

### Output Capacitor $C_{OUT}$

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use an X5R or better grade ceramic capacitor with 6.3V rating and greater than  $22\mu F$  capacitance.

### Output Inductor $L$

There are several considerations in choosing this inductor.

- 1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple

current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{f_{SW} \times I_{OUT,MAX} \times 40\%}$$

Where  $f_{SW}$  is the switching frequency and  $I_{OUT,MAX}$  is the maximum load current.

- 2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT, MIN} > I_{OUT, MAX} + \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{2 \times f_{SW} \times L}$$

- 3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with  $DCR < 50m\Omega$  to achieve a good overall efficiency.

### Load Transient Considerations

The SY8892 regulator integrates the compensation components to achieve good stability and fast transient responses. In some applications, adding a  $22pF$  ceramic capacitor in parallel with  $R_H$  may further speed up the load transient responses and is thus recommended for applications with large load transient step requirements.

### Layout Design

The layout design of the SY8892 is relatively simple. For the best efficiency and to minimize noise problems, the following components should be placed close to the IC:  $C_{IN}$ ,  $L$ ,  $R_H$  and  $R_L$ .

- 1) It is desirable to maximize the PCB copper area connecting to the GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable. Reasonable paths are suggested to be placed underneath the ground pad to enhance the soldering quality and thermal performance.
- 2)  $C_{IN}$  must be close to pins IN and GND. The loop area formed by  $C_{IN}$  and GND must be minimized.
- 3) The PCB copper area associated with the LX pin must be minimized to avoid the potential noise problem.
- 4) The components  $R_H$  and  $R_L$  and the trace connecting to the FB pin must NOT be adjacent to the LX net on the PCB layout to avoid the noise problem.

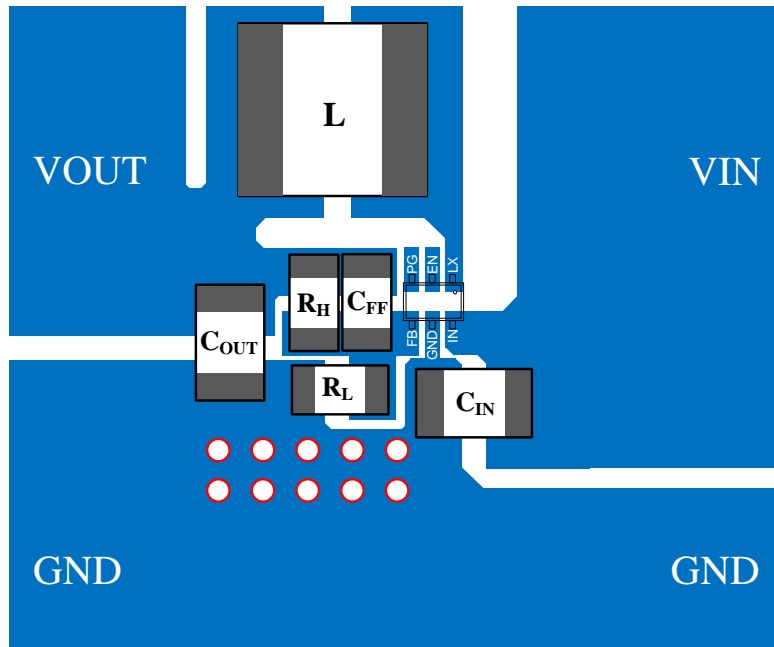
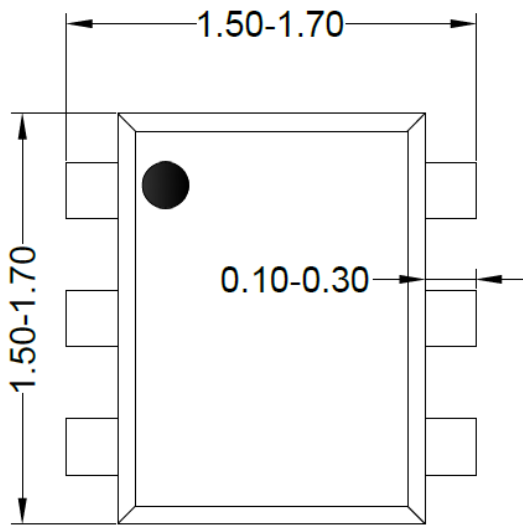


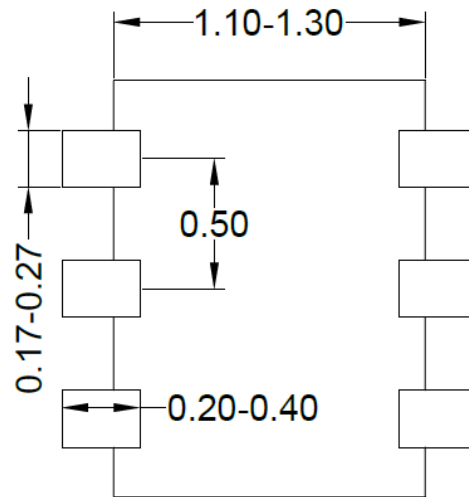
Figure4. PCB Layout Suggestion



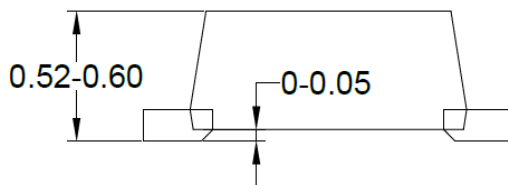
**SOT563 Package Outline Drawing**



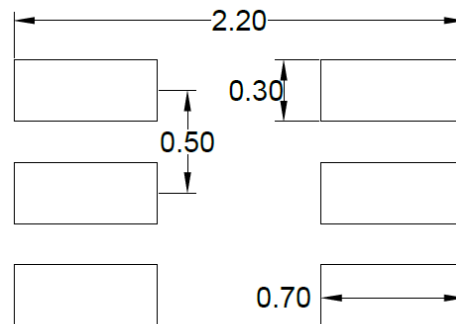
**Top view**



**Bottom view**



**Side View**



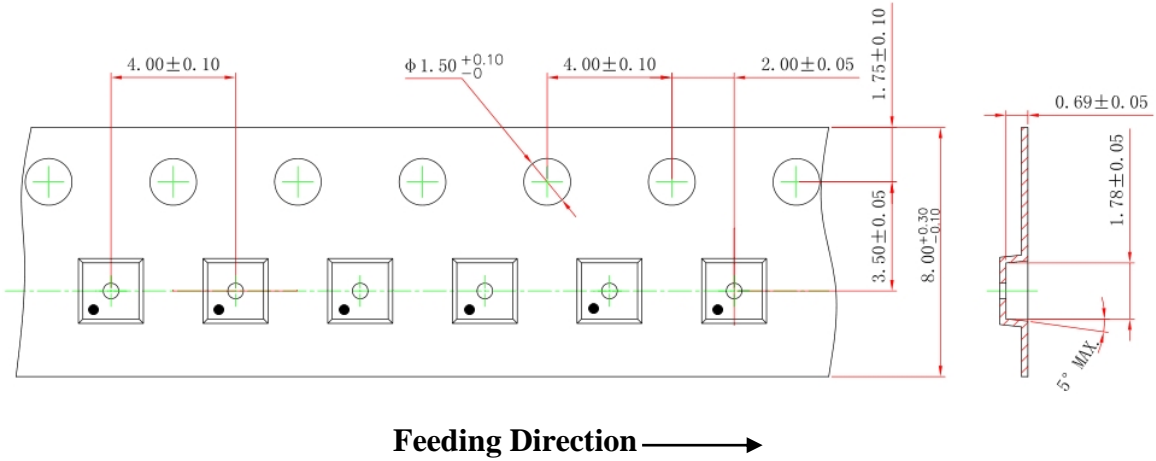
**Recommended PCB layout  
(Reference only)**

**Notes: All dimension in millimeter and exclude mold flash & metal burr.**

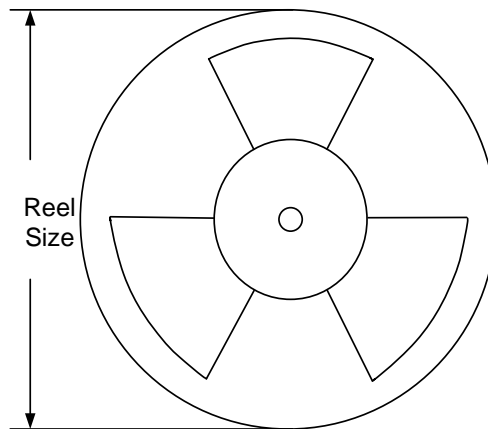
## Taping & Reel Specification

### 1. Taping Orientation

**SOT563**



### 2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
SOT563	8	4	7"	280	160	5000

### 3. Others: NA

## Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

<b>Date</b>	<b>Revision</b>	<b>Change</b>
Jun. 11, 2020	Revision 0.9	Initial Release

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