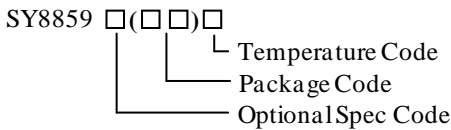


General Description

SY8859 is a high efficient 1.0MHz synchronous step down DC/DC regulator capable of delivering up to 3A output current. The SY8859 can operate over a wide input voltage range from 2.7V to 5.5V and integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

The low output voltage ripple, the small external inductor and the capacitor sizes are achieved with 1.0MHz switching frequency.

Ordering Information



Ordering Number	Package type	Note
SY8859QWC	QFN1.5×1.5-7	--

Features

- Low $R_{DS(ON)}$ for Internal Switches (Top/Bottom) 85mΩ /50mΩ
- 2.7~5.5V Input Voltage Range
- 55μA Low Quiescent Current
- Ultra Fast Load Transient Speed
- High Switching Frequency 1.0MHz Minimizes the External Components
- Internal Soft-start Limits the Inrush Current
- Reliable Short Circuit Protection
- Output Auto Discharge Function
- RoHS Compliant and Halogen Free
- Compact Package: QFN1.5×1.5-7

Applications

- Smart Phone
- LCD TV
- Set Top Box
- Mini-Notebook PC
- Access Point Router

Typical Applications

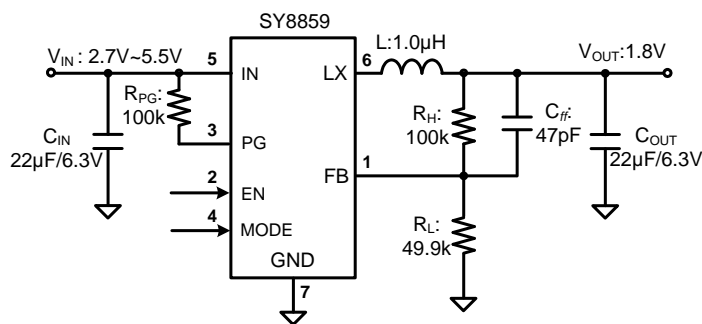


Figure1. Schematic Diagram

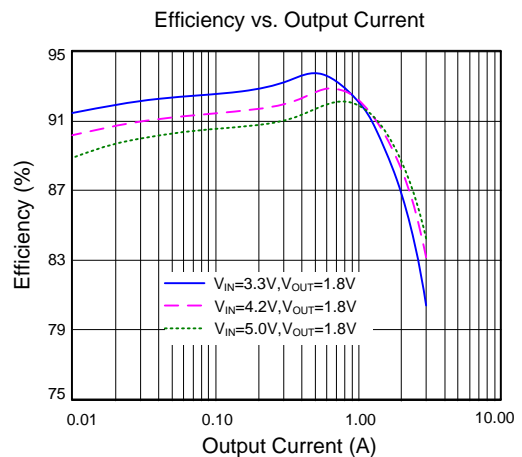
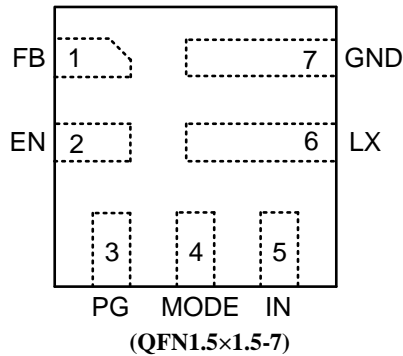


Figure2. Efficiency vs. Output Current

Pinout (Top View)



Top Mark: Prxyz (device code: Pr, x=year code, y=week code, z=lot number code)

Pin Name	Pin Number	Pin Description
FB	1	Feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{OUT}=0.6V \times (1+R_H/R_L)$
EN	2	Enable control. Pull high to turn on. Do not leave it floating.
PG	3	Power good indicator (Open drain output). Low if the output < 90% of regulation voltage or the output >120% of regulation voltage. High otherwise. Connect a pull-up resistor to the input pin.
MODE	4	Mode control pin. Do not leave it floating. MODE=high, selected Force CCM mode operation during light load. MODE=low, selected PFM mode operation during light load.
IN	5	Input pin. Decouple this pin to GND pin with at least a 22μF ceramic capacitor.
LX	6	Inductor pin. Connect this pin to the switching node of the inductor.
GND	7	Ground pin.

Block Diagram

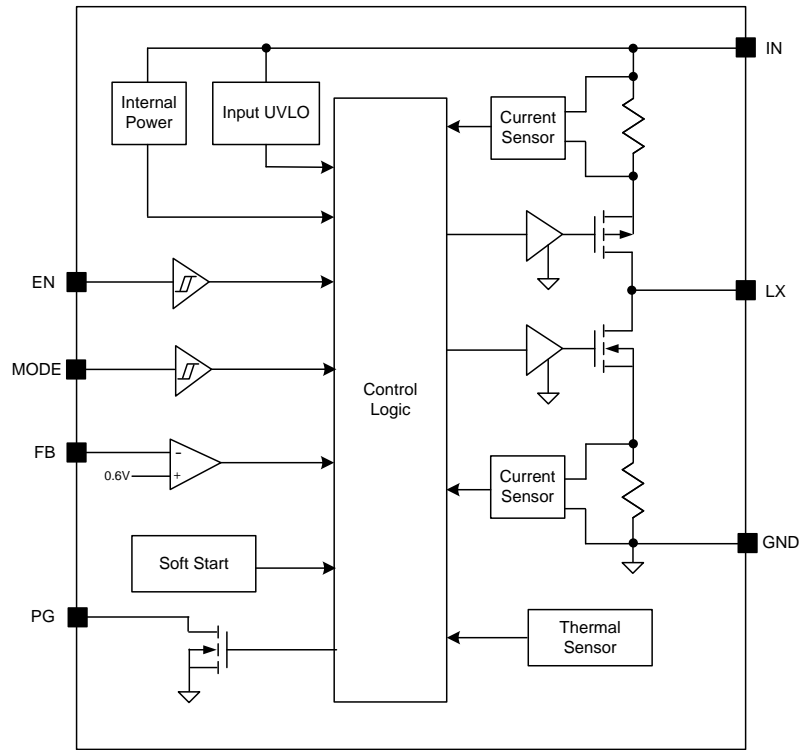


Figure3. Block Diagram

Absolute Maximum Ratings (Note 1)

Supply Input Voltage	-----	6.0V
EN, PG, MODE, FB Voltage	-----	$V_{IN} + 0.6V$
LX Voltage	-----	$-0.3V^{(*1)}$ to $6V^{(*2)}$
Power Dissipation, P_D @ $T_A = 25^\circ C$, QFN1.5x1.5-7	-----	1.5W
Package Thermal Resistance (Note 2)		
θ_{JA}	-----	$66^\circ C/W$
θ_{JC}	-----	$5^\circ C/W$
Junction Temperature Range	-----	$-40^\circ C$ to $150^\circ C$
Lead Temperature (Soldering, 10 sec)	-----	$260^\circ C$
Storage Temperature Range	-----	$-65^\circ C$ to $150^\circ C$
(*1) LX voltage tested down to $-3V < 40ns$		
(*2) LX voltage tested up to $+7V < 40ns$		

Recommended Operating Conditions (Note 3)

Supply Input Voltage	-----	2.7V to 5.5V
Junction Temperature Range	-----	$-40^\circ C$ to $125^\circ C$
Ambient Temperature Range	-----	$-40^\circ C$ to $85^\circ C$

Electrical Characteristics

($V_{IN} = 5.0V$, $V_{OUT} = 1.8V$, $L = 1.0\mu H$, $C_{OUT} = 22\mu F$, $T_A = 25^\circ C$, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.7		5.5	V
Input UVLO Threshold	V_{UVLO}				2.7	V
Input UVLO Hysteresis	V_{HYS}			0.18		V
Quiescent Current	I_Q	$V_{FB} = V_{REF} \times 105\%$		55		μA
Shutdown Current	I_{SHDN}	$EN = 0V$		0.1	1	μA
Feedback Reference Voltage	V_{REF}		594	600	606	mV
Output Discharge Resistance	R_{DIS}			75		Ω
Top FET R_{ON}	$R_{DS(ON)1}$			85		m Ω
Bottom FET R_{ON}	$R_{DS(ON)2}$			50		m Ω
EN Input Voltage High	$V_{EN,H}$		1.1			V
EN Input Voltage Low	$V_{EN,L}$				0.4	V
MODE Input Voltage High	$V_{MODE,H}$		1.1			V
MODE Input Voltage Low	$V_{MODE,L}$				0.4	V
PG Threshold for Under Voltage Detection	$V_{PG,UVP}$			90		$\% V_{REF}$
PG Low Delay Time for Under Voltage Detection	$t_{UVP,DLY}$			15		μs
PG Threshold for Over Voltage Detection	$V_{PG,OVP}$			120		$\% V_{REF}$
PG Low Delay Time for Over Voltage Detection	$t_{OVP,DLY}$			10		μs
Min ON Time	$t_{ON,MIN}$			80		ns
Maximum Duty Cycle	D_{MAX}		60			$\%$
Turn On Delay	$t_{ON,DLY}$	from EN high to LX start switching		90		μs
Soft-start Time	t_{SS}			0.35		ms
Switching Frequency	F_{SW}	CCM		1.0		MHz
Top FET Current Limit	$I_{LMT, TOP}$		4			A
Bottom FET Current Limit	$I_{LMT, BOT}$		3			A
Output Under Voltage Protection Threshold	V_{UVP}			40		$\% V_{REF}$
Output UVP Delay	$t_{UVP,DLY}$			15		μs
Thermal Shutdown Temperature	T_{SD}			150		$^\circ C$
Thermal Shutdown Hysteresis	T_{HYS}			15		$^\circ C$

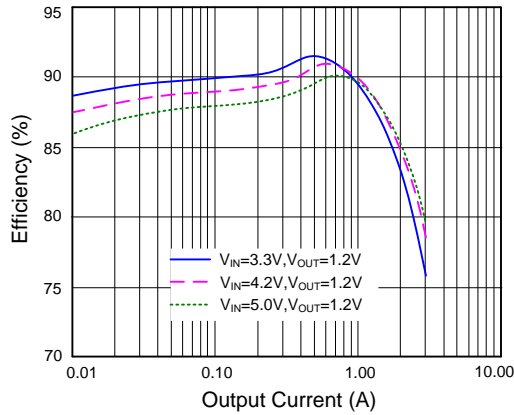
Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} of SY8859QWC is measured in the natural convection at $T_A = 25^\circ C$ on a 20Z two-layer Silergy evaluation board. Paddle of QFN1.5 \times 1.5-7 package is the case position for SY8859QWC θ_{JC} measurement.

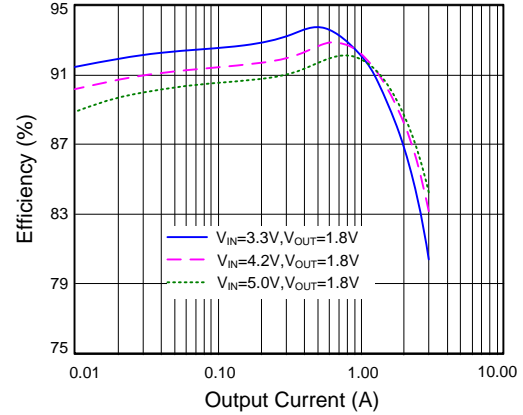
Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

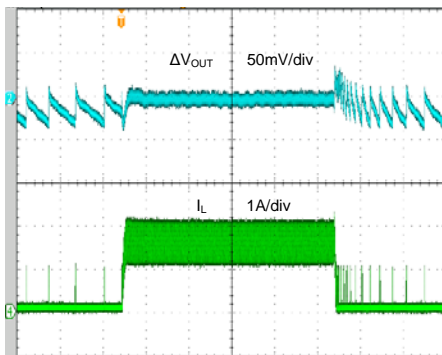
Efficiency vs. Output Current



Efficiency vs. Output Current

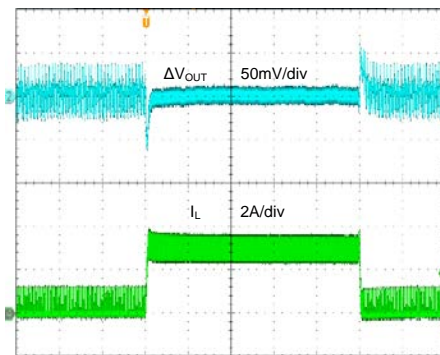


Load Transient
($V_{IN}=5.0V, V_{OUT}=1.8V, I_O=0 \sim 1.5A$)



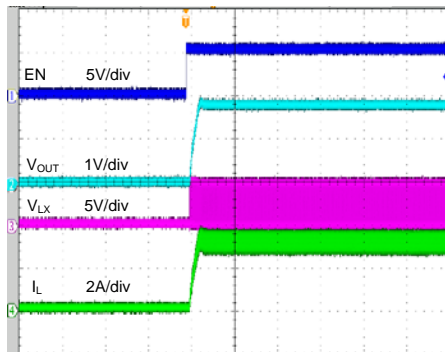
Time (100 μ s/div)

Load Transient
($V_{IN}=5.0V, V_{OUT}=1.8V, I_O=0.3 \sim 3.0A$)



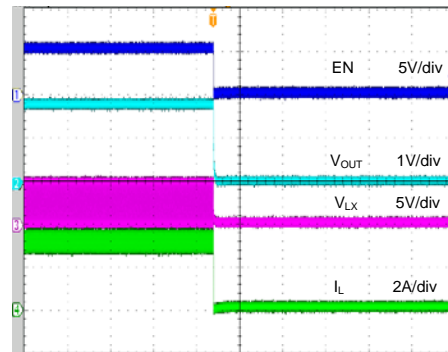
Time (100 μ s/div)

Startup from Enable
($V_{IN}=5.0V, V_{OUT}=1.8V, I_O=3.0A$)



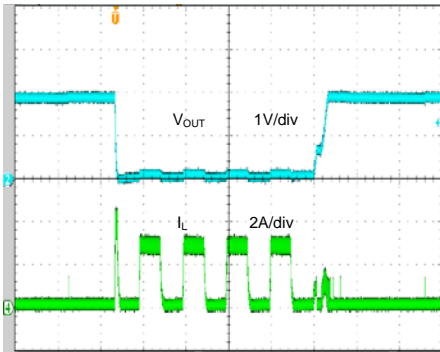
Time (800 μ s/div)

Shutdown from Enable
($V_{IN}=5.0V, V_{OUT}=1.8V, I_O=3.0A$)



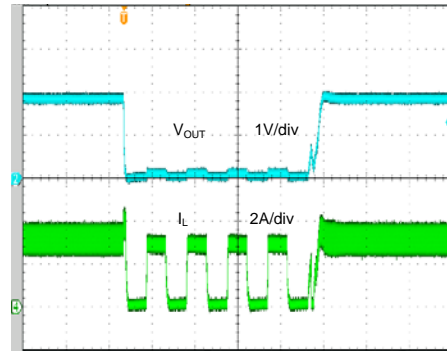
Time (800 μ s/div)

Short Circuit Protection
 ($V_{IN}=5.0V$, $V_{OUT}=1.8V$, $I_O=0A \sim$ short)



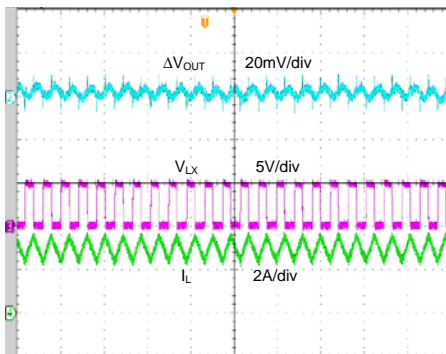
Time (400 μ s/div)

Short Circuit Protection
 ($V_{IN}=5.0V$, $V_{OUT}=1.8V$, $I_O=3.0A \sim$ short)



Time (400 μ s/div)

Output Ripple
 ($V_{IN}=5.0V$, $V_{OUT}=1.8V$, $I_O=3.0A$)



Time (2 μ s/div)

Operation

SY8859 is a high efficient 1.0MHz synchronous step down DC/DC regulator capable of delivering up to 3A output current. The SY8859 can operate over a wide input voltage range from 2.7V to 5.5V and integrate main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

The low output voltage ripple, the small external inductor and the capacitor sizes are achieved with 1.0MHz switching frequency.

Applications Information

Because of the high integration of SY8859, the application circuit based on this regulator IC is rather simple. Only input capacitor C_{IN} , output capacitor C_{OUT} , output inductor L and feedback resistors (R_H and R_L) need to be selected for the target application specifications.

Feedback Resistor Dividers R_H and R_L :

Choose R_H and R_L to program the proper output voltage. To minimize the power consumption under light load, it is desirable to choose large resistance values for both R_H and R_L . A value of between 100k Ω and 1M Ω is highly recommended for both resistors. If $R_L = 120k\Omega$ is chosen, then R_H can be calculated to be:

$$R_H = \frac{(V_{OUT} - 0.6V) \cdot R_L}{0.6V}$$

Input Capacitor C_{IN} :

A typical X5R or better grade ceramic capacitor with 6.3V rating and greater than 22 μ F capacitance is recommended. To minimize the potential noise problem, we should place this ceramic capacitor

really close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN} , and IN/GND pins.

Output Inductor L:

There are several considerations in choosing this inductor.

- 1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{F_{SW} \times I_{OUT,MAX} \times 40\%}$$

Where F_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

- 2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT, MIN} > I_{OUT, MAX} + \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{2 \times F_{SW} \times L}$$

- 3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with $DCR < 25m\Omega$ to achieve good overall efficiency.

Inductor vs. Output Capacitor:

The ripple base control strategy need very small C_{OUT} to confirm stability. Too large the inductor and C_{OUT} will lead to instability. The recommend inductance and the output capacitor are shown as below.

Table1. Inductance vs. Output Capacitor Selection Table

L	C_{OUT}					
	10 μ F	22 μ F	22 μ F \times 2	22 μ F \times 4	22 μ F \times 6	22 μ F \times 8
1.0 μ H	×	√	√	√	√	√
1.5 μ H	×	√	√	√	×	×
2.2 μ H	×	√	√	×	×	×

OCP and SCP Protection Method:

With load current increasing, the low side FET current will get higher than valley current limit threshold. The low side FET will keep turning on until low side FET current decreases below the valley current limit threshold, so that valley current is limited. If the load current continues to increase, the output voltage will drop. When the output voltage falls below 40% of the regulation level, the output short is detected and the IC will operate in hip-cup mode. The hip-cup frequency is 600Hz, the hip-cup duty is 50%. If the hard short is removed, the IC will return to normal operation.

Layout Design:

The layout design of SY8859 regulator is relatively simple. For the best efficiency and to minimum noise problems, we should place the following components close to the IC: C_{IN} , L, R_H and R_L .

1) It is desirable to maximize the PCB copper area adjacent to GND pin to achieve the best thermal performance and noise performance. If the board space allowed, a ground plane is highly desirable. Reasonable vias are suggested to be placed underneath the ground pad to enhance the soldering quality and thermal performance.

2) C_{IN} must be close to pins IN and GND. The loop area formed by C_{IN} and GND must be minimized.

3) The PCB copper area adjacent to LX pin must be minimized to avoid the potential noise problem.

4) The components R_H , R_L , and the trace connected to the FB pin must NOT be adjacent to the LX pin net on the PCB layout to avoid the noise problem.

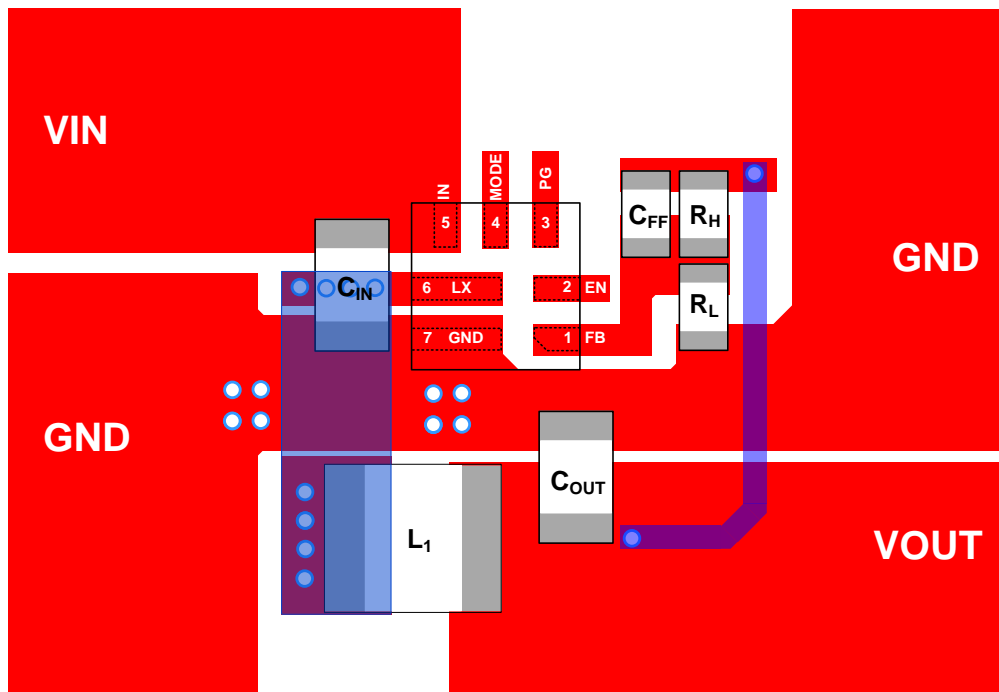
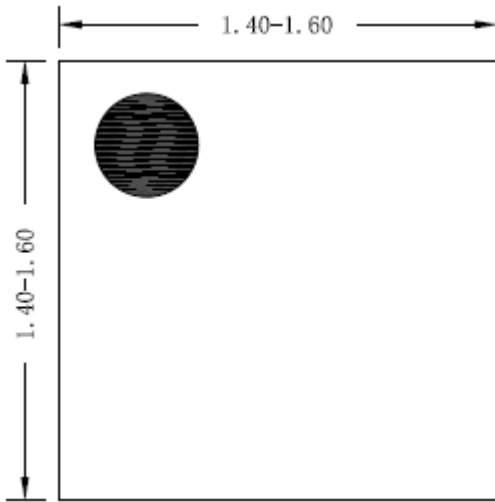
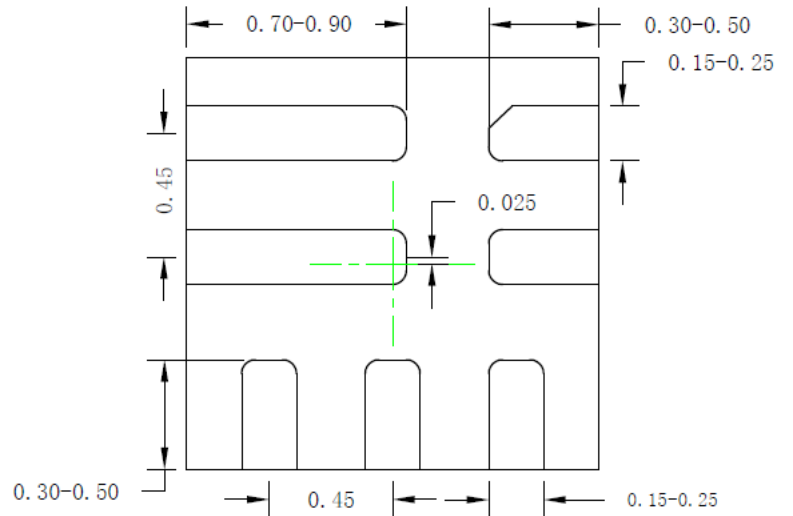


Figure4. PCB Layout Suggestion

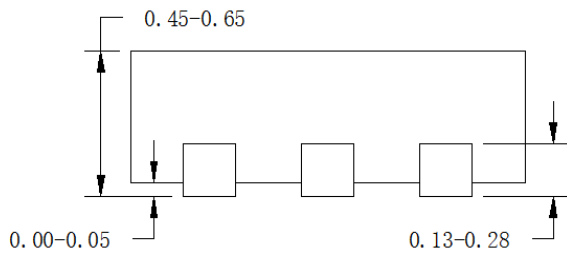
QFN1.5×1.5-7 Package Outline Drawing



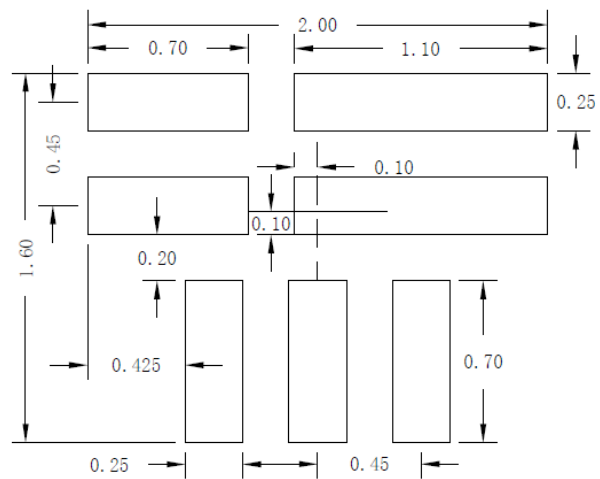
Top View



Bottom View



Side View

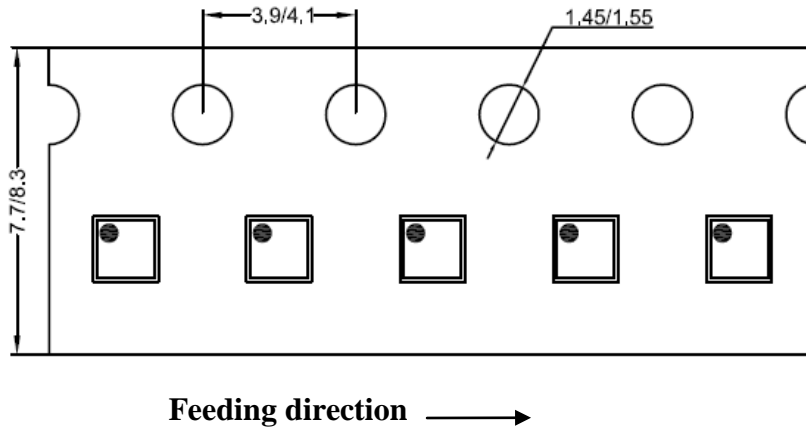


Recommended PCB Layout

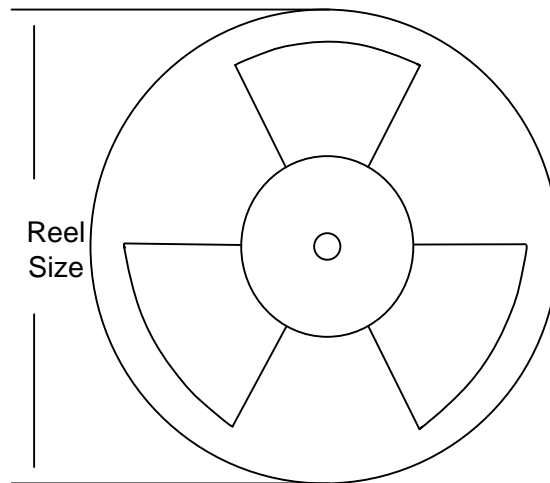
Notes: All dimension in millimeter and exclude mold flash & metal burr

Taping & Reel Specification

1. QFN1.5×1.5 taping orientation



2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN1.5×1.5	8	4	7"	400	160	3000

3. Others: NA



Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Sep. 09, 2022	Revision 0.9C	Update the dimensions in the Bottom View of the Package outline drawing. (page9)
Jan.21, 2021	Revision 0.9B	Update the package outline drawing (page 9)
Jan.10, 2018	Revision 0.9A	Update the Block diagram (page3)
Jun.20, 2017	Revision 0.9	Initial Release



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