SYS14L02DHC

Low Capacitance ESD/Surge Protection for Gigabit Ethernet Interfaces

General Description

SYS14L02DHC is a low-capacitance Transient Voltage Suppressor (TVS) array designed to provide electrostatic discharge (ESD) protection for high-speed data interfaces. With typical capacitance of 3.0pF only, SYS14L02DHC is designed to protect parasitic-sensitive systems against over-voltage and over-current transient events. It complies with IEC 61000-4-2 (ESD) (±30kV air, ±30kV contact discharge), IEC 61000-4-4 (electrical fast transient - EFT) (40A, 5/50 ns), IEC 61000-4-5 (Surge) (40A, 8/20μs), very fast charged device model (CDM) ESD and cable discharge event (CDE), etc.

SYS14L02DHC is in a DFN3.0×2.0-10L package. Each SYS14L02DHC device can protect two high-speed line pairs. The "flow-thru" design minimizes trace inductance and reduces voltage overshoot associated with ESD events. The combined features of low capacitance and high ESD robustness make SYS14L02DHC ideal for high-speed data port and high-frequency line (e.g., Gigabit Ethernet Ports) applications. The low clamping voltage of the SYS14L02DHC guarantees a minimum stress on the protected IC.

Ordering Information

Part Number	Working Voltage	Quantity Per Reel	Reel Size
SYS14L02DHC	2.5V	3,000	7 Inch

Features

- Transient protection for high-speed data lines
  - IEC 61000-4-2 (ESD) ±30kV (Air)
    ±30kV (Contact)
  - IEC 61000-4-4 (EFT) 40A (5/50 ns)
  - IEC 61000-4-5 (Surge) 40A (8/20μs)
- Package optimized for high-speed lines
- Provides protection for two line pairs
- Low capacitance: 3.0pF @ 0V (Typical)
- Low leakage current: 0.1μA @ V_{RWM} (Typical)
- Low operating and clamping voltage
- Each I/O pin can withstand over 1000 ESD strikes for ±8kV contact discharge

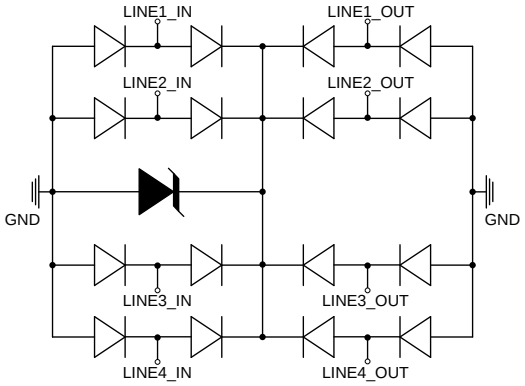
Mechanical Characteristics

- DFN3.0×2.0-10L package
- Flammability Rating: UL 94V-0
- Marking: Part number, Date
- Packaging: Tape and Reel

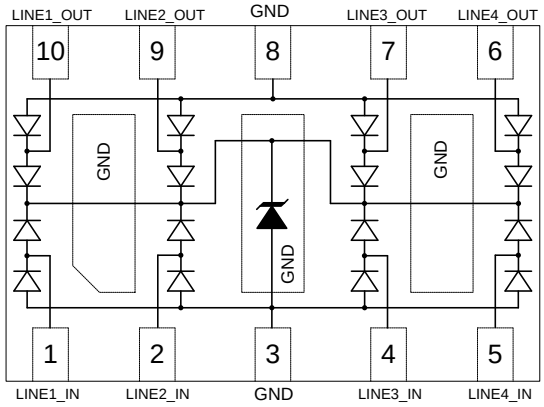
Applications

- 10/100/1000M Ethernet Ports
- WAN/LAN Equipment
- Desktops, Servers and Notebooks
- Cellular Phones
- Switching Systems
- Audio/Video Inputs

Circuit Diagram



Pin Configuration (Top View)



(DFN3.0×2.0-10)

Absolute Maximum Rating

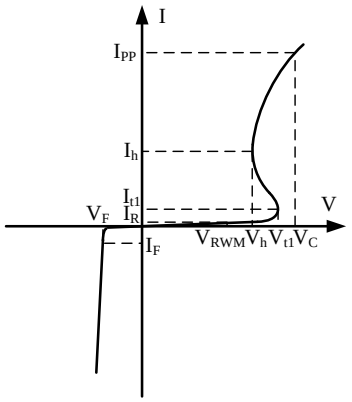
Symbol	Parameter	Value	Units
I_{PP}	Peak Pulse Current (8/20μs)[1]	40	A
P_{PK}	Peak Pulse Power (8/20μs)[1]	1000	Watts
V_{ESD}	ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	±30 ±30	kV
T_{OPT}	Operating Temperature	-55 to +125	°C
T_{STG}	Storage Temperature	-55 to +150	°C

Notes:

1) Ratings with 2 pins connected together per the recommended configuration (ie pin 1 connected to pin 10, pin 2 connected to pin 9, pin 4 connected to pin 7, and pin 5 connected to pin 6).

Electrical Characteristics (T = 25°C)

Symbol	Parameter
V_{RWM}	Nominal Reverse Working Voltage
I_R	Reverse Leakage Current @ V_{RWM}
V_{t1}	Trigger Voltage
I_{t1}	Trigger Current @ V_{t1}
V_h	Holding Voltage
I_h	Holding Current @ V_h
V_C	Clamping Voltage @ I_{PP}
I_{PP}	Maximum Peak Pulse Current
C_{ESD}	Parasitic Capacitance

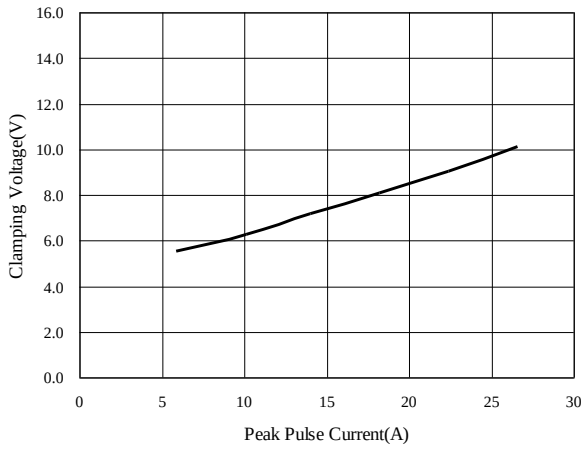


Uni-Directional TVS

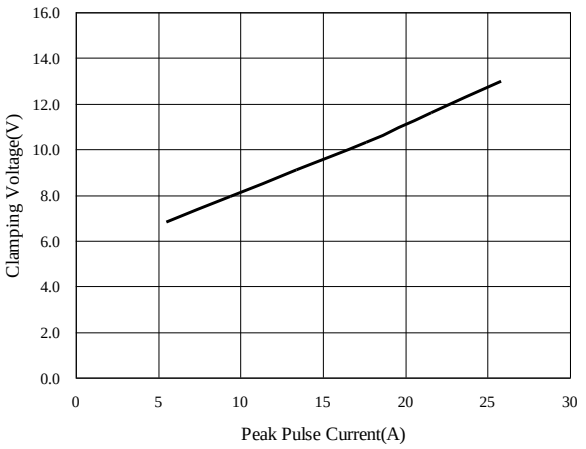
Symbol	Test Condition	Minimum	Typical	Maximum	Units
V_{RWM}				2.5	V
I_R	V_{RWM} = 2.5V, T = 25°C		0.1	1.0	μA
V_{t1}	I_{t1} = 1μA	3.0	3.7	4.5	V
V_h	I_h = 1mA	3.0		4.0	V
V_C	Any I/O to Ground I_{PP} = 1A, t_p = 8/20μs			4.5	V
V_C	Any I/O to Ground I_{PP} = 10A, t_p = 8/20μs			7.5	V
V_C	Any I/O to Ground I_{PP} = 25A, t_p = 8/20μs			12.0	V
V_C	Line-to-Line / Line-to-GND, two I/O Pins connected together on each line I_{PP} = 40A, t_p = 8/20μs			20.0	V
C_{ESD}	Between I/O Pins and Ground V_R = 0V, f = 1MHz		3.0	4.0	pF
C_{ESD}	Between I/O Pins V_R = 0V, f = 1MHz		1.5	2.0	pF

Typical Performance Characteristics

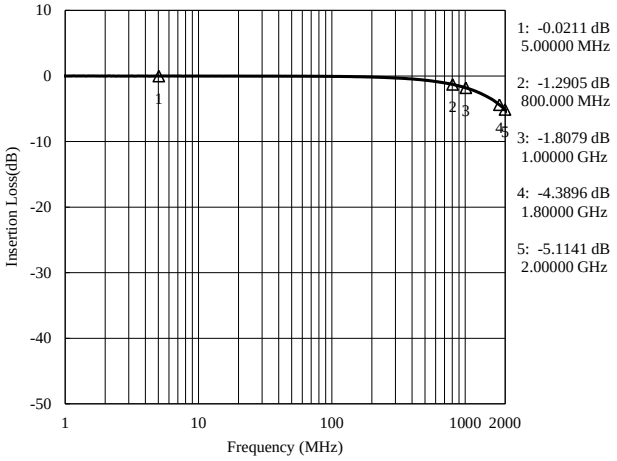
Clamping Voltage V_C vs. Current I_{PP}
Any I/O to GND



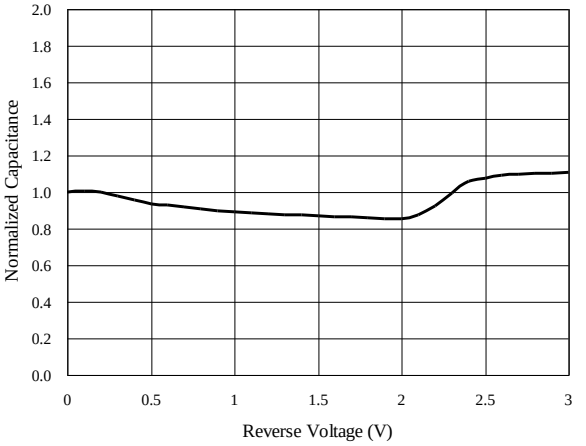
Clamping Voltage V_C vs. Current I_{PP}
Line-to-Line, Two I/O Pins Connected Together



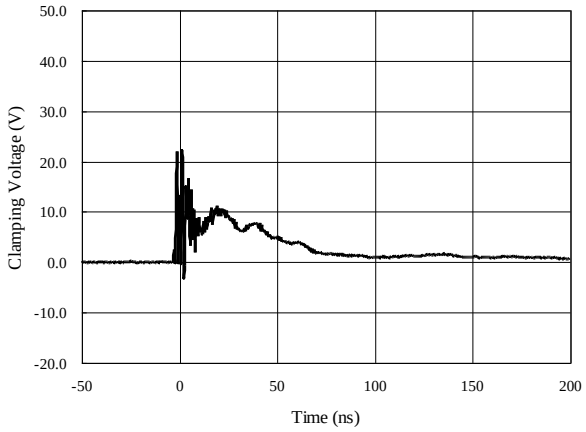
Insertion Loss S21 (I/O to GND)



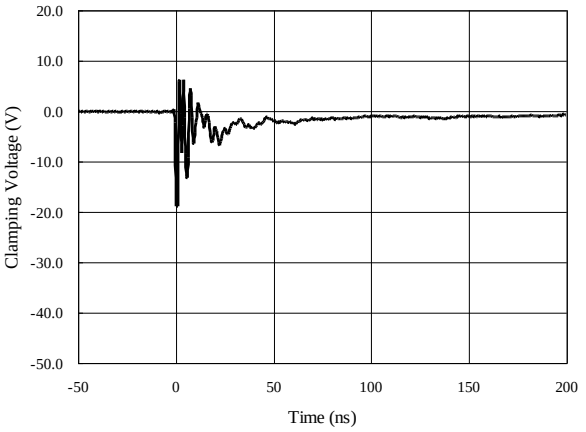
Normalized Capacitance vs. Voltage



ESD Clamping of I/O to GND
(+8kV Contact per IEC 61000-4-2)



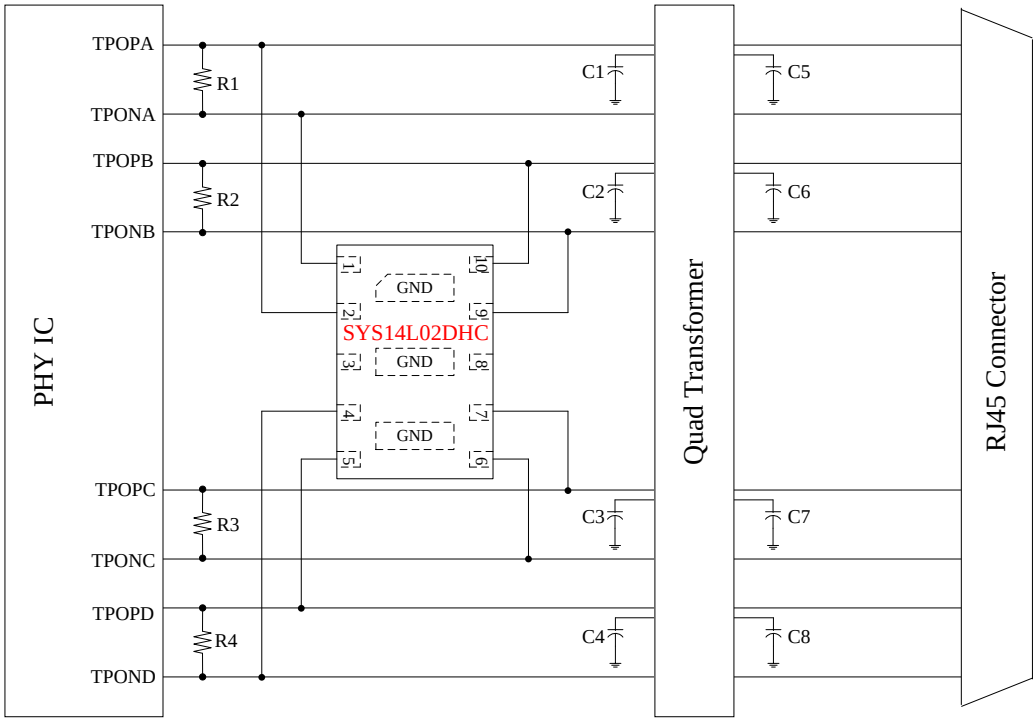
ESD Clamping of I/O to GND
(-8kV Contact per IEC 61000-4-2)



Application Information

Electronic equipment is susceptible to damage caused by a variety of sources, including Electrostatic Discharge (ESD), Electrical Fast Transients (EFT) and Lightning strikes. The SYS14L02DHC was designed to protect the sensitive equipment from damage which may be induced by such transient events. This product can be configured in different connections to meet the requirement of common-mode and differential-mode as follows:

Gigabit Ethernet Protection

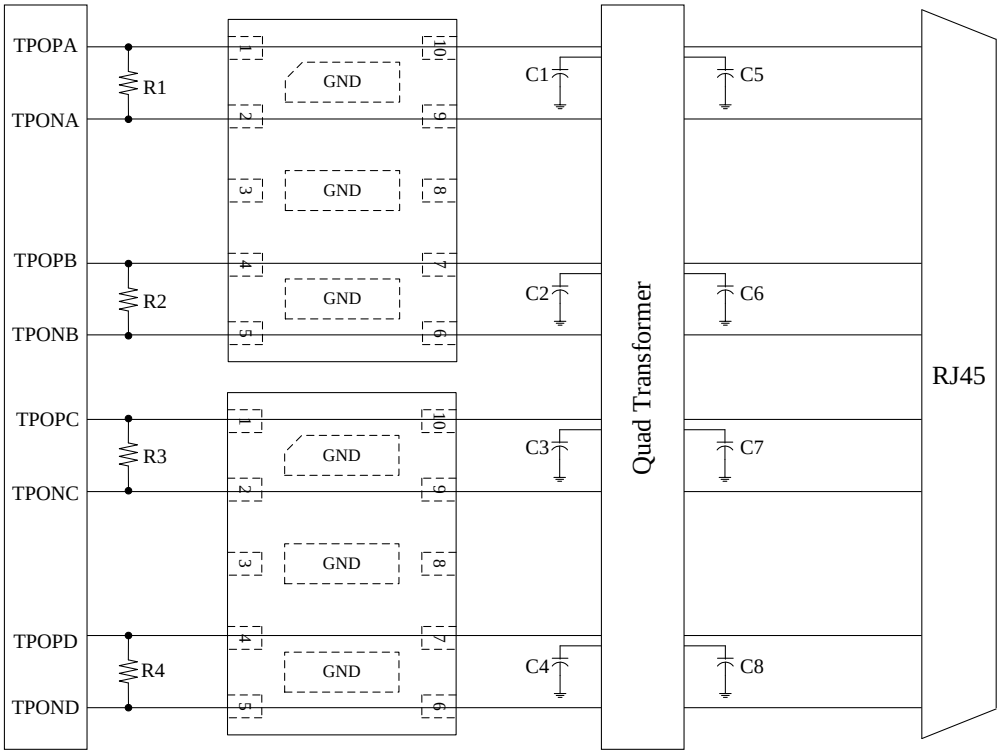


Schematic Diagram for Gigabit Ethernet ESD/Surge Protection using SYS14L02DHC

NOTE:

Please connect pin3, Pin8 and all GND Tabs of SYS14L02DHC to the ground plane of the systems.

Gigabit Ethernet Protection (Cont.)



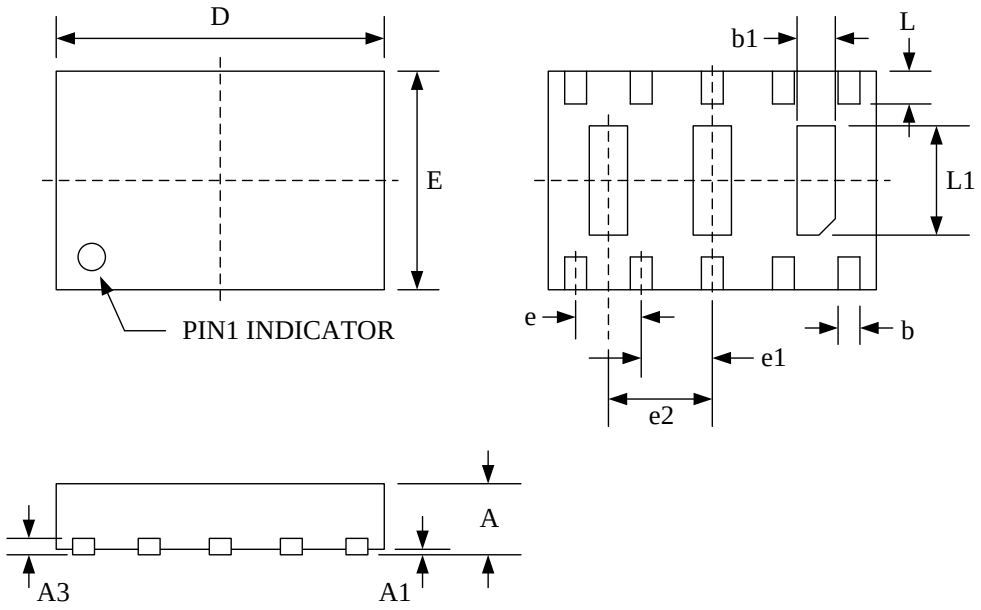
Schematic Diagram for Gigabit Ethernet ESD/Surge Protection using SYS14L02DHC

NOTE:

Please connect pin3, Pin8 and all GND Tabs of SYS14L02DHC to the ground plane of the systems.

Package Outline

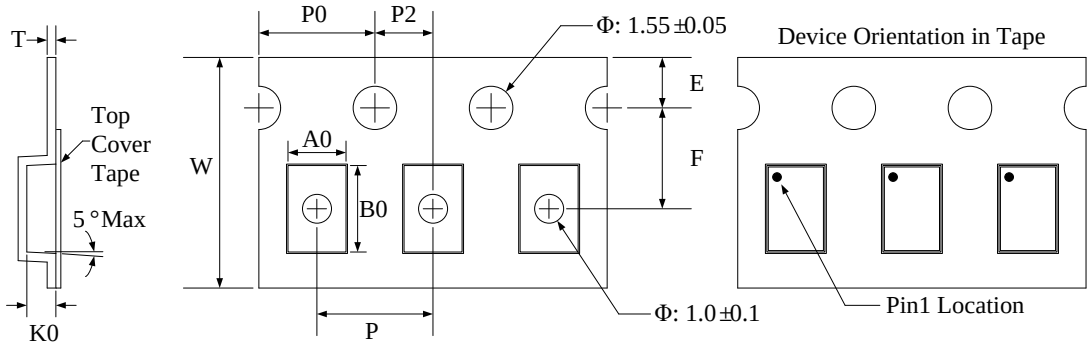
- DFN3.0×2.0-10L package



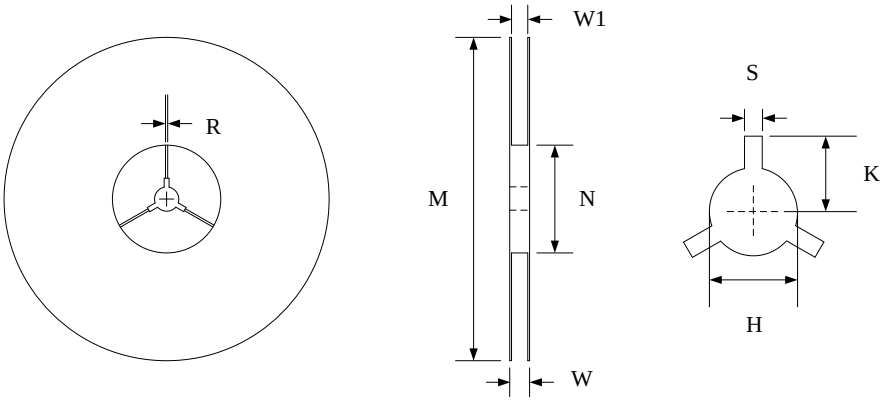
Package Dimensions (Controlling dimensions are in millimeters)

Symbol	Dimensions (mm)			Dimensions (Inches)		
	Minimum	Typical	Maximum	Minimum	Typical	Maximum
A	0.500	0.600	0.650	0.020	0.024	0.026
A1	0.000	0.030	0.050	0.000	0.001	0.002
A3	0.15 REF			0.006 REF		
b	0.150	0.200	0.250	0.006	0.008	0.010
b1	0.250	0.350	0.450	0.010	0.014	0.018
D	2.900	3.000	3.100	0.114	0.118	0.122
E	1.900	2.000	2.100	0.075	0.079	0.083
e	0.600 BSC			0.024 BSC		
e1	0.650 BSC			0.026 BSC		
e2	0.950 BSC			0.037		
L	0.250	0.300	0.350	0.010	0.012	0.014
L1	0.950	1.000	1.050	0.037	0.039	0.041

Tape and Reel Specification

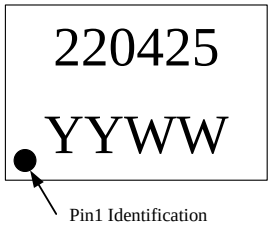


Symbol	W	A0	B0	K0	E	F	P	P0	P2	T
Dimensions (mm)	8.00+0.3 -0.1	2.3 ±0.1	3.2 ±0.1	1.0 ±0.1	1.75 ±0.1	3.5 ±0.05	4.0 ±0.1	4.0 ±0.1	2.0 ±0.1	0.3 ±0.05



Symbol	Reel Size	M	N	W	W1	H	S	K	R
Dimensions (mm)	Φ178	178.0 ±1.0	60.0 ±1.0	11.5 ±0.5	9.0 ±0.5	13.0 ±0.5	2.0 ±0.1	11.0 ±0.2	1.0 ±0.05

Marking Codes

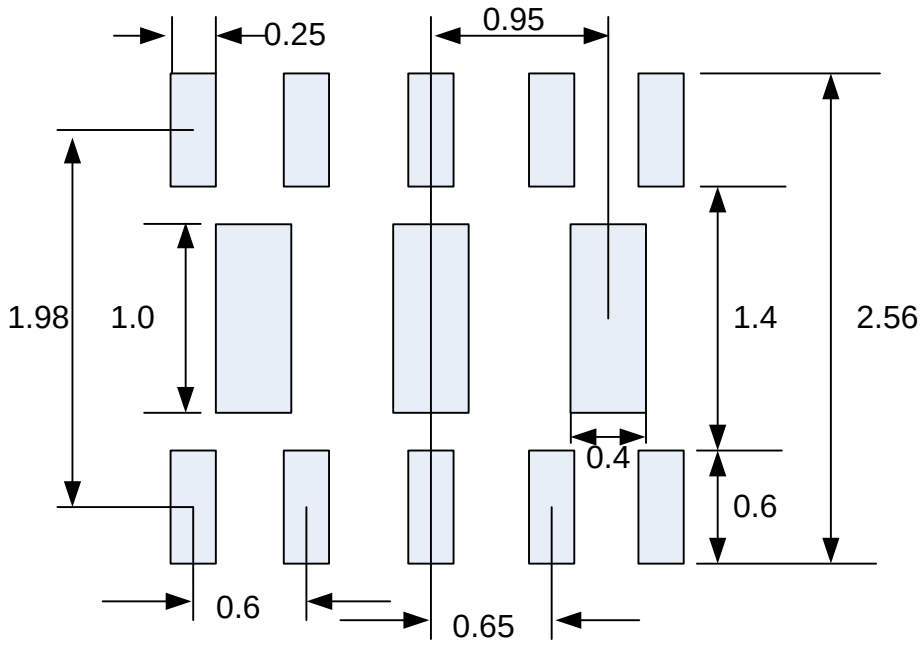


Note:

(1) "220425" is the part number, fixed.

(2) "YYWW" is date code. "YY" is year (2012 is "12"); while "WW" is the assembly week in a year.

Suggested PCB Layout



SYS14L02DHC